GOMACTech-05

Government Microcircuit Applications
and
Critical Technology Conference

FINAL PROGRAM

"Intelligent Technologies"

April 4 - 7, 2005

The Riviera Hotel
Las Vegas, Nevada

GOMACTech-05
ADVANCE PROGRAM
CONTENTS

WELCOME

The GOMACTech-05 Program Committee is pleased to welcome you to this year's conference in Las Vegas, Nevada. GOMACTech strives to be the Government's pre-eminent conference for the review of developments in microcircuit applications for government systems and has been utilized to announce major government microelectronics initiatives such as VHSIC, MIMIC, and others. GOMACTech was established in 1968 and is an Unclassified, Export-Controlled event that requires all participants to be U.S. Citizens or legal U.S. Permanent Residents.

This year's conference theme, "Intelligent Technologies," recognizes that systems which can gather and analyze data as well as make decisions autonomously in harsh unfriendly environments require a marriage of high-performance information-processing technologies with highly capable sensor technologies.

This year's conference will follow a format that has proven very successful in recent years in which both technical and topical sessions will be included. The technical sessions will consist of papers that are both contributed and solicited while the topical sessions will consist of presentations that are focused on the work being performed within selected ongoing government-sponsored programs. Topical session themes this year include Array Technologies, Technology for Frequency Agile Digitally Synthesized Transmitters (TFAST), Vertically Integrated Sensor Arrays (VISA), Sensors and Urban Warfare, The New Millennium Program, and Electronics for Extreme Environments.

On Tuesday morning the conference will formally begin with an excellent Plenary Session. Mr. Pete Theisinger, Project Manager of the Mars Science Laboratory and the Mars Exploration Rovers, Jet Propulsion Laboratory (JPL), will present the Keynote Address "Rovers on Mars – The Technical Underpinnings". In keeping with the conference theme, the Jack Kilby Lecture Series will feature Dr. James Hutchby of the Semiconductor Research Corporation discussing "Beyond Silicon," Dr. Matthew Goodman of Telcordia presenting insight into "FPGAs in DoD Systems – Benefits and Challenges," and Prof. Linda Katehi of Purdue University will conclude the series with "Three-Dimensional Circuits for Compact, Reconfigurable, and Multifunctional Systems."

Prior to the formal opening of the conference, two tutorials will be offered on Monday afternoon for which the cost is included as part of the conference registration fee. In the first tutorial, "Nanoelectronics," four leaders in their respective areas will provide overviews of recent progress in Nanotubes/Nanowires, Nano-magnetoelectronics, Nano-photonics, and Nanofabrication. The second tutorial, "Sensor Networks and Applications," will review the evolution of sensor-network research and address new opportunities resulting from advances in sensor computing, communication technologies, and challenges that must be met to implement sensor networks.

The Plenary and Technical Paper Sessions are the major sources of formal information exchange that will occur at the conference. Other sources are provided through the Exhibition, which includes major IC manufacturers and commercial vendors of devices, equipment, systems, and services for nearly all facets of the electronics business. The exhibition opens on Tuesday at noon and

runs through Wednesday at 4:00 pm. On Tuesday, following the last technical paper session, representatives from various IC manufacturers will present posters on efforts that support the Radiation-Hardened Technology Roadmaps. In addition, representatives from the Government will present posters on their respective capabilities in microelectronics technology development. Following the Poster Session, there will be an Exhibitors' Reception, sponsored by Northrop Grumman, where attendees can mix in a relaxing atmosphere of food and good spirits. On Thursday, a Government Applications and Vision Session will be held during lunch in which current and future directions of government-sponsored programs will be presented.

This strong technical program reflects the hard work of the GOMACTech-05 Technical Program Committee. The committee aggressively sought out particular topics and areas for presentations, and we think the quality of the conference this year will positively reflect this effort. We appreciate your support and believe that GOMACTech-05 will be a rewarding experience.

Ingham A. Mack
Conference Chair
Office of Naval Research

Sammy A. Kayali
Technical Program Chair
Jet Propulsion Laboratory

REGISTRATION

All sessions of GOMACTech-05 are being held here at the Riviera Hotel in Las Vegas, Nevada. Both check-in and on-site registration will take place in the hotel's Convention Center Foyer.

Conference check-in and on-site registration hours:

Monday, 4 April – 10:00 am – 5:00 pm
Tuesday, 5 April – 7:00 am – 5:00 pm
Wednesday, 6 April – 7:00 am – 5:00 pm
Thursday, 7 April – 7:00 am – 5:00 pm

SECURITY PROCEDURES

The GOMACTech Conference is an Unclassified, Export-Controlled event that requires participants to be U.S. Citizens or legal U.S. Permanent Residents. All registrants must provide proof of U.S. Citizenship or Permanent Resident status prior to being permitted entry into the conference. Additionally, a signed **Non-Disclosure Statement** will be required.

You may prove U.S. citizenship with any one of the following:
U.S. Passport
Birth Certificate **AND** valid government-issued photo ID
Naturalization Certificate **AND** valid government-issued photo ID

The following are NOT proof of citizenship:
Voter registration card
Driver's license

GOMACTech TUTORIALS

Two 4-hour tutorials of interest to the GOMACTech community are a special feature of the conference. The tutorials are both being held on Monday, 4 April, 1:00 – 5:00 pm. There is no additional fee for the tutorials, but registrants must indicate their intention to attend on the registration form.

Tutorial 1: Nanotechnology

Capri Room 101

Moderators: **Chagaan Battar,** *IDA, Alexandria, VA*
Cliff Lau, *IDA, Alexandria, VA*

Nanotubes and Nanowires: An Overview in System Development
M. Meyyappan, NASA Ames Research Center, Moffett Field, CA

Carbon nanotubes (CNTs) with their unique electronic properties and extraordinary mechanical properties have been the subject of intensive research for logic, memory, actuator, and sensor devices. Recently, inorganic nanowires of silicon, germanium, and high-temperature oxides and nitrides have shown interesting characteristics to warrant consideration for the same applications. An overview of the growth, characterization, and application development in both mechanical systems will be given.

Nanoimprint Lithography: An Enabling Engine for Nanotechnology and Next-Generation ICs

Stephen Y. Chou, Michael Austin, Neil Li, and Rich Yu,
Princeton University, Princeton, NJ

Nanoimprint lithography (NIL) is a revolutionary method of nanopatterning that offers ultra-high resolution (sub 5 nm), high throughput, and low cost – unmatchable by other existing lithography. NIL is regarded as one of 10 emerging technologies that can significantly change the world (*MIT Technology Review*) and has been put on the International Roadmap for Semiconductor Industry's ITRS roadmap as one of the next generation of lithographies for IC manufacturing.

Spin-Transfer-Induced Excitations in Magnetic Nanostructures

W. H. Rippard, M. R. Pufall, S. Kaka, and T. J. Silva
NIST, Boulder, CO

Recent developments in spin-transfer-induced phenomena in magnetic nanostructures will be discussed. More specifically, this will include an overview of high-speed-current-induced switching and high-frequency (GHz) oscillations in magnetic "nanopillars" and "nanocontacts".

Nanophotonics: New Opportunities for Integration of Lasers, Modulators, Filters, and Detectors for Data Communications and Microfluidic Sensors

Axel Scherer
Caltech, Pasadena, CA

The emergence of silicon on insulator substrates, advanced crystal growth, and high-resolution fabrication techniques offers new opportunities for dense integration of optical devices. These opportunities, with a focus on filters, waveguides, resonators, and surface plasmon devices, will be discussed.

Tutorial 2: Sensor Networks and Applications

Capri Room 102

Moderator: Sri Kumar, *DARPA/IPTO, Arlington, VA*

Dr. Sri Kumar
DARPA/IPTO, Arlington, VA

Advances in semiconductor and microelectromechanical (MEMS) technology have enabled a convergence of sensors, processing, and communications. This trend in hardware miniaturization and integration of sensing, computing, and communication chips has enabled a number of militarily-important applications. There is a desire to closely couple design of the network with the application, but the methods and tools to do this still remain a challenge. This tutorial will review the evolution of sensor-network research and address new opportunities, resulting from advances in sensor, computing, and communication technologies, and challenges that must be met to implement sensor networks.

EXHIBITION

An exhibition comprised of commercial vendors exhibiting products of interest to the GOMACTech community is an integral part of the conference. All attendees are reminded to visit the exhibitors when they have some free time. The Exhibit Hall is located in the hotel's Grand Ballroom E. Coffee breaks will be held in the exhibit area when they coincide with the exhibition's hours of operation. On Tuesday evening an Exhibitors' Reception, sponsored by the Northrop Grumman, where attendees can mix in a relaxing atmosphere of food and good spirits. Exhibition hours are as follows:

Tuesday, 5 April 12:00 pm – 8:00 pm
Wednesday, 6 April 9:00 am – 4:00 pm

Exhibitors

Air Force Research Laboratory
Amkor Test Services
APIC Corp.
ATK Mission Research
Atmel Corp.
BAE Systems
Boeing Phantom Works
CPU Technology, Inc.
Discovery Semiconductors, Inc.
Diversified Technologies
DPA Components International
EDAptive Computing, Inc.
Honeywell
IBM Corp.
JSI Microelectronics
LSI Logic Corp.
M/A – COM
National Reconnaissance Office
Northrop Grumman
NxGen/US-Semi
Peregrine Semiconductor
Sandia National Laboratories
Silvaco InternationalSynopsys, Inc.

WEDNESDAY EVENING SOCIAL

The Top of the Riv Ballroom on the 24th floor of the hotel's Monaco Tower will be the site of this year's Wednesday evening dinner event. The Top of the Riv offers a spectacular view of the night lights of Las Vegas. Dinner will be served at 7:00 pm followed by a top-flight Las Vegas entertainer. Tickets should be purchased in advance along with your conference registration. Adults $ 25.

HOTEL ACCOMMODATIONS

The Riviera Hotel and Casino enjoys a legendary past as one of the first top-notch Las Vegas hotels in Nevada, known for its big name entertainment and friendly hospitality, as well as its world-wide name recognition. Preparing for its Golden Anniversary in 2005, the historic Riviera is one of the state's premier destination spots, offering the passion and excitement of nostalgic Las Vegas, combined with a modern-day, multi-million-dollar remodeling of rooms and convention facilities, bringing the property up to par with today's mega-resort competition.

Over 2000 refurbished oversized rooms offer maximum comfort and breathtaking views of the glittering Las Vegas Strip with its western scenic panoramas. Each accommodation has been attractively decorated.

GOMACTech has reserved a block of rooms at the special conference rates of $104 single, $109 double. These rates are exclusive of Clark County tax (currently 9%) and an energy surcharge of $3.50/night.

Reservations may be made by calling the hotel reservations department at 1-800-634-6753.

Not currently available, but anticipated before the time of GOMACTech, all rooms will have wireless Internet capability at an additional daily charge (expected to be $10/day).

CONFERENCE CONTACT

Anyone requiring additional information about GOMACTech should contact the Conference Coordinator, Ralph Nadell, GOMACTech, 411 Lafayette Street, Suite 201, New York, NY 10003 (212/460-8090 x203), Rnadell@pcm411.com.

GOMACTech '04 PAPER AWARDS

Paper awards based on audience evaluations from GOMACTech-04 will include the George Abraham Outstanding Paper Award and a Meritorious Paper Award to the runner-up. Presentation of these well-deserved awards will be made at the Plenary Session on Tuesday morning in Grande Ballroom C/D. The GOMACTech-04 winners are:

The George Abraham Outstanding Paper Award (7.1)

J. W. Ward, M. Meinhold, T. R. Bengston, and G. F. Carleton
Nantero, Inc., Woburn, MA

"*Large-Scale Integration of Single-Walled Carbon-Nanotube (CNT) Nonvolatile RAM*"

Meritorious Paper Award (18.7)

F. Ayazi
Georgia Institute of Technology, Atlanta, GA

"*Nano-Precision Integrated Electromechanical Filters for UHF Communications*"

AGED SERVICE RECOGNITION

The following individuals will be recognized for their contributions to the DoD through their service on the Advisory Group on Electron Devices:

Peter Asbeck
John Brock
Jon Christensen
James Clary
Barry Dunbridge
Barry Gilbert
May Hibbs-Brenner
William Howard
Conilee Kirkpatrick
Charles Krumm
David Myers
Joseph Saloom
William Tennant
Richard Williamson
Debbie Wilson
Andrew Yang

RATING FORM / QUESTIONNAIRE

Do not forget to vote for your favorite presentation this year before you leave the conference. A rating form/questionnaire is being handed out at conference check-in. To encourage the submission of forms, all attendees who hand in a completed form at the registration desk will be given a USB laptop-computer light.

SPEAKERS' PREP ROOM

Capri Room 109 is designated as a speakers' preparation room and will be available during the hours the conference registration desk is open. Speakers are encouraged to use the Capri 109 facilities to ensure compatibility with the meeting's A/V equipment. Speakers having difficulties should request at the conference registration desk to see an A/V operator. Speakers are also asked to be at their assigned presentation room 30 minutes before the sessions begins to meet with their session chair. An A/V operator will be assigned to each technical session room.

CD-ROM PROCEEDINGS

The first volume of the GOMACTech CD-ROM Proceedings, containing searchable, condensed versions of submitted papers presented at the conference will be distributed to all registrants. Additional copies of the CD-ROM can be purchased at the conference at a cost of $40.00 per CD.

Previously published as the GOMAC Digest of Technical Papers, Volumes I – XXVIII, this publication is the only record of the conference. Previous GOMAC digests will, upon request, be made available to qualified Defense Technical Information Center (DTIC) users. Please call 1-800-225-3842 for bound or microfiche copies. Past Digests can be ordered by calling the above number and identifying the following accession numbers (please note that GOMAC was not held in the calendar year of 1995):

GOMAC-84 B113271	-86 B107186	-87 B119187
-88 B129239	-89 B138550	-90 B150254
-91 B160081	-92 B169396	-93 B177761
-94 B195015	-96 B212362	-97 B222171
-98 B235088	-99 B242763	-00 B254138
-01 B264749	-02 B275146	-03 M201604
-04 M201663		

INFORMATION / MESSAGE CENTER

The Information/Message Center will be located adjacent to the GOMACTech Registration Desk located in the Conference Center Foyer. The message center telephone number for incoming calls is 702/734-5110. Callers should ask to be transferred to the GOMACTech Registration Desk.

PARTICIPATING GOVERNMENT ORGANIZATIONS

Participating Government Organizations of GOMACTech-05 include: Department of Defense (Army, Navy, Air Force) ... National Aeronautics and Space Administration ... Department of Commerce (National Institute of Standards and Technology) ... National Security Agency ... Department of Energy (Sandia National Laboratories) ... Defense Logistics Agency ... Department of Health and Human Services ... Defense Threat Reduction Agency ... Defense Advanced Research Projects Agency ... Central Intelligence Agency ... National Reconnaissance Office

GOMAC WEB SITE

Information on GOMACTech may be obtained through its Web site at www.gomactech.net.

TUESDAY, 5 APRIL

PLENARY SESSION

Tuesday, April 5 / 8:30 am – 12:00 pm / Grande Ballroom C/D

Opening Remarks **(8:30–8:45)**

Ingham Mack, GOMACTech-05 General Chair
Office of Naval Research, Arlington, VA

GOMACTech Awards and AGED Service Recognition **(8:45–9:00)**

Keynote Address **(9:00–10:00)**

Mr. Peter Theisinger
Manager, Mars Science Laboratory Project
Jet Propulsion Laboratory, Pasadena, CA

"Rovers on Mars – The Technical Underpinnings"

BREAK **(10:00–10:30)**

Jack S. Kilby Lecture Series **(10:30–12:00)**

Dr. James Hutchby
SRC, Research Triangle Park, NC

"***Beyond Silicon***"

Dr. Matthew S. Goodman
Chief Scientist and Telcordia Fellow
Telcordia Technologies, Red Bank, NJ

"***FPGAs in DoD Systems – Benefits and Challenges***"

Prof. Linda Katehi
Dean of Engineering
Purdue University, West Lafayette, IN

"***Three-Dimensional Circuits for Compact, Reconfigurable, and Multifunctional Systems***"

LUNCH **(12:00–1:30)**

Session 1

RAD-HARD ELECTRONICS AND SYSTEMS

Tuesday, April 5 / 1:30 – 3:30 pm / Grande Ballroom C

Chair: **Lew Cohn**
DTRA, Fort Belvoir, MD
Co-Chair: **Ken Label**
NASA–GSPC, Greenbelt, MD

1.1: Silicon-Carbide Rad-Hard Power Semiconductors (1:30)

C. Severt
AFRL/PRPE, Wright-Patterson AFB, OH

This presentation will define silicon carbide power devices that have been subjected to radiation tests and present characterization data prior to and subsequent to various levels and types of radiation. Conclusions concerning the general radiation tolerance and specific device capabilities while operating in a radiation environment will be made.

1.2: A Rad-Hard 128K × 36 SRAM for Space Applications (1:50)

S. Doyle, T. Hoang, E. Maher, J. Gilliam
BAE SYSTEMS, Manassas, VA

A new high-performance 128K × 36 SRAM is being developed in 0.15-µm RH15 technology for use in space and other strategic rad-hard applications. For the first time, a synchronous architecture has been selected, allowing users greater flexibility and compatibility with commercial pipelined synchronous, late write, and burst SRAMs. By using advanced RHBD techniques, 200-MHz operation will support 1x cycle time when used as L2 Cache with the RAD750 microprocessor.

1.3: 150-nm Rad-Hard SOI-Structured ASIC Family (2:10)

D. Kagey, J. Hobbs, J. Culp
Honeywell SSEC, Minneapolis, MN

D. Holt
Lightspeed, Santa Clara, CA

Honeywell is leveraging its 150-nm assured rad-hard SOI technology to develop a structured ASIC solution to the Hi-Rel Space requirements for TID and SEU hardened flight units. The structured ASIC approach will cut traditional NRE costs by a factor of 5, while keeping delivery cycles for ASICs with more than a million gates to 12–15 weeks.

1.4: A Rad-Hard 0.25-µm Mixed-Signal CMOS Technology for Read-Out ICs and Extreme Temperature Applications (2:30)

M. S. Polavarapu, J. Ishii, M. Girmay, E. Chan
BAE SYSTEMS, Manassas, VA

A rad-hard 0.25-µm mixed-signal CMOS technology, featuring shallow trench isolation (STI), dual-work-function gate electrodes, capacitors, and resistors, will be described. The results demonstrate suitability for read-out integrated circuits (ROICs) and other extreme temperature applications.

1.5: A 0.15-µm Rad-Hard Anti-Fuse Field-Programmable Gate-Array Technology (2:50)

D. Patel, L. Rockett, S. Danziger, B. Sujlana
BAE SYSTEMS, Manassas, VA

There is a growing need for high-density rad-hard field-programmable gate arrays (FPGAs) that meet the needs of military and space applications. BAE SYSTEMS, in partnership with the DoD community, is currently modernizing its process facility located in Manassas, Virginia, to support a strategically rad-hard 0.15-µm bulk CMOS process technology. This paper describes the features and data of a 0.15-µm rad-hard anti-fuse FPGA.

1.6: Implementing Next-Generation Rad-Hard ASICs (3:10)

J. Avery
Honeywell, Plymouth, MN

Honeywell is introducing a 150-nm design and manufacturing capability to produce radiation-tolerant and rad-hard ASICs with nearly 15 million gates. The initial challenge in developing rad-hard ICs is in the front-end design. A very deep submicron multimillion-gate ASIC requires a fundamentally different approach than traditional methods. This paper will address a design flow and infrastructure model Honeywell has developed to manage VDSM design complexity.

BREAK (3:30–3:40)

Session 2

SENSOR URBAN WARFARE

Tuesday, April 5 / 1:30 – 3:10 pm / Grande Ballroom D

Chair: Kathleen A. Griggs
Puritan Research Corp., Vienna, VA

2.1: The Promise and Challenge of Vision-Based Obstacle Avoidance for Unmanned Flight in Urban Environments (1:30)

J. E. Corban
Guided Systems Technologies, Inc., McDonough, GA

A. R. Tannenbaum, A. J. Calise, E. N. Johnson
Georgia Institute of Technology, Atlanta, GA

Autonomous operation of unmanned flight systems in urban environments is precluded by the immature state of obstacle avoidance technology. Recent advances in image processing hint at the potential for image-based obstacle avoidance, but will require integration with advanced micro-electronics to achieve practical real-time implementation. The promise and challenge will be discussed, and collaboration in implementation sought.

2.2: Ground-Attack Warning System (1:50)

I. Agurok, T. Jannson, G. Savant
Physical Optics Corp., Torrance, CA

J. McCalmont
AFRL, Wright-Patterson AFB, OH

Physical Optics Corporation will present its development of the Ground Attack Warning System (GAWS). The GAWS will be mounted on armored vehicles and operates in urban battlefield environments to detect the launch of RPG and TOW missiles and track them in flight.

2.3: Sentient Environments Using Video-Based Wide-Area Tracking and Immersive Visualizations (2:10)

M. Aggarwal, T. Germano, A. Arpa, S. Samarasekera
Sarnoff Corp., Princeton, NJ

A sentient system that combines comprehensive detection and tracking of all moving objects and immersive visualization of a cluttered and crowded environment using a network of stereo cameras will be presented. Smart processing is used to analyze stereo video streams to detect and track all moving objects in cluttered urban environments. The system is designed specifically to monitor moving people within a localized environment such as an office building, terminal, or other enclosed site.

2.4: Intelligent Photonic Sensors for Urban Warfare (2:30)

R. Dutt, J. Chan
APIC Corp., Culver City, CA

APIC has been pursuing SOI system-on-a-chip technology because of its capability of incorporating both photonics and electronics circuits on one chip. The result of a very-low-loss SOI waveguide and an intelligent SOI sensor that can be used for chemical, biological, or simply as a pressure sensor will be presented. Finally, an intelligent dual-band imager for urban warfare will be described. These miniaturized sensor systems with on-chip processing and communication capability could be key components for distributed intrusion alert systems.

2.5: Real-Time Stereo-Based Obstacle Detection for UAV Threat Avoidance (2:50)

J. Byrne, M. Cosgrove, R. Mehra
Scientific Systems Company, Inc., Woburn, MA

A system for UAV obstacle detection based on Sarnoff Corp's Acadia I vision processor for 23-Hz 640 x 480 binocular stereo and 10-Hz mincut-based recursive bipartition of an affinity graph on embedded hardware will be described. Simulation, indoor, outdoor, and flight-experiment results will be given.

BREAK (3:10–3:40)

Session 3

RF POWER

Tuesday, April 5 / 1:30 – 3:10 pm / Grande Ballroom G

Chair: Denis C. Webb
Naval Research Laboratory, Washington, DC

3.1: High-Frequency Power Metamorphic HEMT (1:30)

C. S. Whelan, K. Herrick, J. Laroche, K. W. Brown
Raytheon, Andover, MA

By tailoring the devices material, geometry, and processing, device designers have fabricated a state-of-the-art high-frequency metamorphic HEMT device with a G_{max} of 12 dB, a power density of 360 mW/mm, and PAEs exceeding 30% at 95 GHz. This device had been utilized to create a range of W-band amplifiers with excellent performance, including a 266-mW PA operating at 90 GHz.

3.2: 56-W SiC MESFET Transistors with a PAE > 50% for L-Band Applications (1:50)

B. Luo, P. Chen, A. Higgins, H. Finlay
Rockwell Scientific, Thousand Oaks, CA

A large gate periphery SiC MESFET has been designed and fabricated. A peak output power of 56 W and a PAE of 53% was measured from 30-mm single-die packaged transistors. The device dc characterization, frequency response, and statistical analysis will be presented.

3.3: The Design of Low-Cost 4- and 6-W MMIC High-Power Amplifiers for Ka-Band Modules (2:10)

M. R. Lyons, C. D. Grondahl, S. M. Daoud
U.S. Monolithics, Chandler, AZ

Two Ka-band power-amplifier MMICs, 4 and 6 W, with high power density and gain will be presented. Each amplifier was designed by using a five-stage topology to demonstrate over 30 dB of gain. The 4-W design exhibited a peak saturated output power of 37.2 dBm and a chip output power density of 532 mW/mm^2. This is the highest recorded power density for a Ka-band power-amplifier design to date. The high gain and power density of these designs make them ideal for low-cost Ka-band transmit systems.

3.4: A V-Band GaAs PHEMT Power Amplifier for Crosslink Applications (2:30)

K-L. Ngo Wah, Y. C. Chou, J. Goel, R. Grundbacher
Northrop Grumman, Redondo Beach, CA

A GaAs PHEMT MMIC power amplifier for crosslink satellite applications from 59 to 63 GHz will be presented. This MMIC demonstrates an output power performance of greater than 30.7 dBm on a full MMIC (greater than 28.5 dBm on half MMIC) and leads to the demonstration of a solid-state power amplifier (SSPA) module with a output power of 12.8 W at V-band using a low-loss combining technique.

3.5: High-Voltage MESFET Technology for MMIC Applications (2:50)

T. A. Winslow, D. Conway
Tycoelectronics, Roanoke, VA

High-voltage MESFET technology has been developed to address the needs of military radar system integrators, who require low-cost high-yield high-power-density power amplifiers. The high-voltage MESFET process is an extension of an existing and very mature MSAG MESFET process. 24-V high-power MMICs have been developed and have demonstrated excellent performance.

BREAK (3:10–3:40)

Session 4

RAD-HARD TECHNOLOGY ROADMAPS

Tuesday, April 5 / 3:40–5:10 pm / Grande Ballroom C

(Note: These papers are also included in the Poster Session)

Chair: **Lew Cohn**
DTRA, Fort Belvoir, MD
Co-Chair: **Ken Label**
NASA–GSPC, Greenbelt, MD

4.1: BAE SYSTEMS Rad-Hard Microelectronics Technology Roadmap (3:40)

L. Rockett, N. Haddad, M. Polavarapu, T. Bach
BAE SYSTEMS, Manassas, VA

BAE SYSTEMS, in partnership with the DoD, is completing foundry modernization to be rad-hard 150-nm CMOS technology production ready by 2Q '05. The rad-hard technology roadmap identifies the technology extensions being pursued to advance their rad-hard technology capabilities beyond the 150-nm technology node to closely track the technology capabilities offered by commercial foundries.

4.2: Peregrine Semiconductor Technology Roadmap (3:50)

C. Tabbert
Peregrine Semiconductor, Albuquerque, NM

Peregrine Semiconductor will present technology and product roadmaps supporting highly integrated RF and photonic products for space applications. Highlighted during this presentation will be recent advances in integrated GPS receiver technology and transmit-receiver module integration for phased-array antenna applications along with new RF products extending RF CMOS into Ku-Band RF applications.

4.3: Roadmap to 150-nm Rad-Hard Semiconductor Products (4:00)

G. Kirchner and J. Hobbs
Honeywell Defense & Space Electronics Systems

Honeywell has developed radiation-tolerant 150-nm semiconductor technology and rad-hard capability before the end of 2005. Near-future products based on 150-nm technology include 15-million-gate ASICs, 16MB SRAMs, 1MB MRAMS, and high-speed SerDes.

4.4: Title III Microelectronics Programs (4:10)

E. Pohlenz and B. Hagerty
AFRL (Title III), Wright-Patterson AFB, OH

P. Hastings
Northrop Grumman Information Technology, Fairborn, OH

All of the Title III programs that are pertinent to military microelectronics, including programs such as CAPEX and Space Microprocessors as well as other Title III programs focused on space, will be discussed.

4.5: Northrop Grumman Rad-Hard Technology Overview (4:20)

D. Adams, M. Fitzpatrick
Northrop Grumman Corp., Linthicum, MD

A broad range of mixed-signal, power, and nonvolatile memory products for space and avionics applications that are produced at the Northrop Grumman Corporation (NGC) Advanced Technology Center in Baltimore, Maryland, will be described.

4.6: The Continued Evolution of Re-Configurable FPGAs for Military and Space Strategic Applications

WITHDRAWN

H. Bogrow, J. Fabula, J. Moore
Xilinx, Albuquerque, NM

Present and future military and space applications continue to demand ever increasing performance, density, and above all flexibility from FPGAs. The Virtex families of re-configurable FPGAs provide the technology to meet these demands. This paper will focus mainly on Xilinx's currently available Virtex solutions, while possibly also discussing Xilinx's future development efforts.

4.7: Aeroflex's Roadmap for the Development of Rad-Hard ICs Using Commercial Foundries (4:30)

D. Wilkin
Aeroflex, Inc., Colorado Springs, CO

Aeroflex Colorado Springs will present their roadmap for the continued development of rad-hard integrated circuits using commercial wafer foundries. Products built on 0.6-, 0.25-, and 0.18-μm CMOS commercial silicon using a combination of design hardness and/or co-processing techniques will be summarized.

4.8: Rad-Hard Technology Roadmap for Microelectronics and Space Computers (4:40)

D. R. Czajkowski, D. J. Strobel
Space Micro, Inc., San Diego, CA

The ability to leverage advanced commercial COTS microelectronics is critical to providing warfighters capability. Space Micro's technology roadmap, products, and techniques, which enable use of COTS in a radiation environment, will be described.

4.9: Actel Corp.'s Technology Roadmap (4:50)

B. Cronquist, C Clardy, K. Oneill, T. Farinaro
Actel Corp., Mountain View, CA

Actel Corporation's product roadmap for high-reliability applications will be presented. Both the non-volatile one-time programmable (OTP) FPGA and the non-volatile re-programmable FPGA roadmap will be discussed. Commercial, MIL-TEMP, rad-tolerant, and rad-hard efforts will be described. Special mention will be given to the definition, content, and schedule for the radiation-tolerant non-volatile re-programmable field-programmable gate-array (RTNVRFPGA) product family. The Actel packaging roadmap for high-reliability applications will also be presented.

Session 5

DISTRIBUTED AUTONOMOUS SENSOR SYSTEMS

Tuesday, April 5 / 3:40 – 5:20 pm / Grande Ballroom D

Chair: **Jill P. Dahlburg**
Naval Research Laboratory, Washington, DC
Co-Chair: **Kathleen A. Griggs**
Puritan Research Corp., Vienna, VA

5.1: Physicomimetics Positioning Methodology for Distributed Autonomous Systems (3:40)

M. W. M. Spears, D. F. Spears
University of Wyoming, Laramie, WO

A framework called “physicomimetics” that provides distributed control of large collections of mobile vehicles will be described. This framework allows hundreds of vehicles to self-organize into sensor networks. The practicality of this approach on the “chemical-plume tracing” task, which traces a toxic plume to its source emitter, will be discussed.

5.2: Visualization for Volumetric Control in a Mobile Environment (4:00)

D. P. Schissel
General Atomics, San Diego, CA

A mobile sensor suite with advanced volumetric visualization and display technology can provide rapidly deployable surveillance and security for high-value assets or at suspected areas of enemy activity. This presentation will discuss the technical state of the art as well as give results from the demonstration of a first prototype.

5.3: Efficient Broadband RF Energy Harvesting for Wireless Sensors (4:20)

R. Zane, Z. Popovic
University of Colorado, Boulder, CO

A solution for high-efficiency broadband RF power delivery to miniature wireless sensors, thus alleviating distributed sensor networks from power wires or periodic battery replacement, will be demonstrated. The approach is based on broadband rectenna design and high-efficiency power-processing circuitry.

5.4: Embedded-Gas-Sensor System-on-Chip Characterization System (4:40)

Y. Afridi, A. Hefner, C. Ellenwood, R. Cavicchi
NIST, Gaithersburg, MD

A characterization system for evaluating critical functions of a micro-hotplate-based embedded gas sensor for system-on-a-chip applications will be presented. The system uses a virtual instrument interface to control parts-per-billion (ppb) gas-concentration levels and microhotplate temperature-controlled registers and acquires temperature- and gas-sensor data through an on-chip analog-to-digital converter.

5.5: Robust Fiber-Optic Chemical/Gas-Sensing Systems (5:00)

H. Xia, K-Li Deng
GE Global Research, Niskayuna, NY

This paper demonstrates that chemical sensing can be implemented based on bared FBGs and LPGs without etching, cladding, or chemical-active coating. The results, for the first time, have disclosed that the chemical sensing based on FBG is a one-step process due to chemical atom diffusion effect. The developed sensing systems are robust and compatible to existing fiber-optic devices.

Session 6

ADAPTIVE RF I

Tuesday, April 5 / 3:40 – 5:20 pm / Grande Ballroom G

Chair: **Eric D. Adler**
Army Research Laboratory, Adelphi, MD
Co-Chair: **William D. Palmer**
Army Research Laboratory, Adelphi, MD

6.1: Miniature Tunable Combline Filters (3:40)

S. Mehta, P. Petre, J. Foschaar
HRL Labs, Malibu, CA

HRL Laboratories' progress in developing state-of-the-art extremely miniature, tunable combline filters for the C, X, and Ku-bands will be reported. These filters are essential components for ONR's Advanced Multifunction RF System Concept (AMRF-C). The salient filter features are small size, low insertion loss, high tunability, and fast response time.

6.2: RF on Flex Panel for X-Band Phased Arrays (4:00)

A. Jacomb-Hood, R. Melcher, E. Lier, E. Talley
LM CSS, Newtown, PA

T. Destefano, P. Kraft, N. Fardella, V. Ozuna
LM MS2, Moorestown, NJ

A passive X-band phased-array panel using RF-on-flex interconnect to minimize mass and cost has been fabricated and tested. The panel was assembled using an industry-standard automated assembly line. State-of-the-art panel mass was demonstrated. The measured antenna performance is in reasonable agreement with the predicted performance.

6.3: Packaging and Transitions for Intelligent RF Microsystems (4:20)

K. Herrick
Raytheon, Andover, MA

A. Margomenos
EMAG Technologies, Ann Arbor, MI

R. Lahiji
Purdue University, West Lafayette, IN

Y. Lee
EMAG Technologies, Ann Arbor, MI

By integrating a university RF MEMS packaging process with an industry III-V standard, a manufacturable process has been developed which integrates FETs, RF MEMS, vertical RF transitions, and thermocompression bonded packaging on GaAs substrates. Significant benchmarks in this development include individual transition and wafer bonding results.

6.4: Low-Temperature Wafer-Level Packaging for RF MEMS Switches (4:40)

P. Chang-Chien, K. Tornquist, M. Truong, C. Geiger
Northrop Grumman Space Technology, Redondo Beach, CA

A low-temperature high-yield wafer-level-packaging (WLP) technique has been developed and demonstrated. Data obtained from packaged MEMS switches shows this WLP technique produces close to 100% cavity bonding yield and a very high packaged device yield. The encapsulated switch is accessed through low-loss RF vias from the backside of the package, which is only 100-μm thick. Furthermore, this technology is compatible with NGSTs standard 100-mm MMIC fabrication processes, making packaging MMIC-integrated MEMS devices with this WLP technology possible.

6.5: High-Efficiency RF Class E Power Amplifiers for Unattended Ground Sensor Applications (5:00)

J. D. Popp, J. F. Rowland, A. H. Yang
SPAWAR System Center San Diego, San Diego, CA

D. Y. C. Lie
SYS Technologies, San Diego, CA

This paper investigates high-efficiency RF Class E power-amplifier technology for unattended ground sensor systems. Results of designs using COTS technology and IBM SiGe 7HP technology operating in the 300-MHz and 2.4-GHz bands will be presented. These designs demonstrate 3x improvements in power efficiency over available technology.

Interactive Session

POSTER SESSION

Tuesday, April 6 / 5:20 – 6:30 pm / Grande Ballroom H

Chair: Lew Cohen
DTRA, Ft. Belvoir, MD

Government Laboratories

P.1: AFRL Mixed-Signal Design Center

V. J. Patel, H. S. Axtell, C. L. A. Cerny
AFRL/SND, Wright-Patterson AFB, OH

For many years, receivers have taken advantage of the III-V technologies for performance. However, these technologies and system packaging have proven to be expensive and challenging to integrate. Also, the difficulty of achieving first-pass fabrication success in III-V and in silicon technologies compounds the problem of cost. Therefore, AFRL and DARPA initiated efforts to reduce the cost of these receiver systems by evaluating and demonstrating advanced silicon processes. In the attempt to achieve first-pass success, DARPA funded the NeoCAD effort that allowed both industry and universities to put forth ideas and develop new electronic-design-automation tools for RF and analog.

P.2: Defense Microelectronics Activity Capabilities

D. Pentrack
Defense Microelectronics Activity, McClellan, CA

DMEA provides the DoD with a variety of microelectronics design, fabrication, and test services. Digital, analog, mixed-signal, RF, and EEPROM devices are fabricated in a true flexible foundry using a variety of licensed processes. DMEA thereby assures a continued source of supply for 5 V and rad-hard technologies.

P.3: Radiation-Tolerant Microelectronics Developments at NAVSEA Crane

WITHDRAWN

J. McKamey, D. Platteter, J. Clark
NAVSEA Crane, Crane, IN

Current work includes nuclear hardening and design of guidance system electronics for the Navy's Trident II missile system along with radiation effects research and development for the Defense Threat Reduction Agency.

P.4: Air Force Research Laboratory

C. Gordon
AFRL/VSSE, Kirtland AFB, NM

Advances in microelectronics are revolutionizing defense capabilities, with space-based surveillance, communications, and navigation as prime examples. In search of transformational military space capabilities, the Air Force Research Laboratory's Space Vehicles Directorate is focusing on reconfigurability, very high performance, and design hardening as a foundation for affordable, sustainable spacecraft electronics.

P.5: NRL Electronics S&T Program

A. Campbell, G. M. Borsuk
NRL, Washington, DC

NRL conducts an in-house multi-disciplinary research program that addresses six thrust areas: solid-state electronics, nanoelectronics, plasma science and technology, power electronics, vacuum electronics, and electro-optics science and technology. A brief overview of the key research opportunities being addressed in each of these thrusts will be presented.

P.6: The NASA Electronic Parts and Packaging (NEPP) Program: Roadmap for NASA's Radiation Effects on and Reliability of Electronics Efforts

K. A. LaBel, M. J. Sampson
NASA/GSFC, Greenbelt, MD

C. E. Barnes
Jet Propulsion Laboratory, Pasadena, CA

The NEPP Program is responsible for developing the plans for and leading the research on reliability and radiation response in the space and aeronautics environments. Presented herein are the current NASA tasks as well as a consideration of future research areas.

P.7: The Sandia National Laboratories Microelectronics Program

K. K. Ma, F. W Sexton, P. E. Dodd
Sandia National Laboratories, Albuquerque, New Mexico

The current status of the Sandia National Laboratories Radiation-Hardened Microelectronics Program wii be described. The influence of many factors on the program's direction, including the acceptance of using commercial field-programmable gate arrays, single-event transient effects on ultra-deep-submicron silicon technologies, hardened-by-design methodology, and trends in commercial microelectronic industry, will be discussed.

P.8: The NIST Workshop on Reliability Issues in Nano-Materials

R. R. Keller, D.T. Read
NIST, Boulder, CO

The introduction of nanomaterials into current and future technologies opens up an entirely new suite of both materials science and measurement science challenges. Effects of dimensional scaling play a stronger role in the reliability of nanomaterials than in any other materials known to date. Surfaces and interfaces can easily dominate and change behavior and properties known to develop in bulk materials of the same chemical composition. As such, one cannot simply extrapolate what is now known about bulk material behavior to the nanoscale and expect to predict the structure or properties accurately. In order to address many of these concerns, NIST hosted a workshop entitled "Reliability Issues in Nanomaterials," held 17–19 August, 2004 in Boulder, Colorado, to discuss research issues and measurement-related barriers that affect the reliability of extremely fine-scale materials.

P.9: Reliability Construction Analysis Anticipating the Next DMS Train Wreck: How to Evaluate Ultra-Submicron-Feature-Size IC Reliability

G. Gaugler
DMEA, Sacramento, CA

This new work uses EBSD as a key analysis method for predicting lifetime expectations of COTS integrated circuits when used in a military environment. This work focuses on electromigration effects as significant over other effects that are receiving different attention.

Industry Roadmaps

P.10: (4.1) BAE SYSTEMS's Rad-Hard Microelectronics Technology Roadmap

L. Rockett, N. Haddad, M. Polavarapu, T. Bach
BAE SYSTEMS, Manassas, VA

BAE SYSTEMS, in partnership with the DoD, is completing foundry modernization to be rad-hard 150-nm CMOS technology production ready by 2Q '05. The rad-hard technology roadmap identifies the technology extensions being pursued to advance their rad-hard technology capabilities beyond the 150-nm technology node to closely track the technology capabilities offered by commercial foundries.

P.11: (4.2) Peregrine Semiconductor's Technology Roadmap

C. Tabbert
Peregrine Semiconductor, Albuquerque, NM

Peregrine Semiconductor will present technology and product roadmaps supporting highly integrated RF and photonic products for space applications. Highlighted during this presentation will be recent advances in integrated GPS receiver technology and transmit-receiver module integration for phased-array antenna applications along with new RF products extending RF CMOS into Ku-Band RF applications.

P.12: (4.3) Roadmap to 150-nm Rad-Hard Semiconductor Products

G. Kirchner and J. Hobbs
Honeywell Defense & Space Electronics Systems

Honeywell has developed radiation-tolerant 150-nm semiconductor technology and rad-hard capability before the end of 2005. Near-future products based on 150-nm technology include 15-million-gate ASICs, 16MB SRAMs, 1MB MRAMS, and high-speed SerDes.

P.13: (4.4) Title III Microelectronics Programs

P. Hastings
Northrop Grumman Information Technology, Fairborn, OH

All of the Title III programs that are pertinent to military microelectronics, including programs such as CAPEX and Space Microprocessors as well as other Title III programs focused on space, will be discussed.

P.14: (4.5) Northrop Grumman's Rad-Hard Technology Overview

D. Adams, M. Fitzpatrick
Northrop Grumman Corp., Linthicum, MD

A broad range of mixed-signal, power, and nonvolatile memory products for space and avionics applications that are produced at the Northrop Grumman Corporation (NGC) Advanced Technology Center in Baltimore, Maryland, will be described.

P.15: (4.6) The Continued Evolution of Re-Configurable FPGAs for Military and Space Strategic Applications

H. Bogrow, J. Fabula, J. Moore
Xilinx, Albuquerque, NM

Present and future military and space applications continue to demand ever increasing performance, density, and above all flexibility from FPGAs. The Virtex families of re-configurable FPGAs provide the technology to meet these demands. This paper will focus mainly on Xilinx's currently available Virtex solutions, while possibly also discussing Xilinx's future development efforts.

P.16: (4.7) Aeroflex's Roadmap for the Development of Rad-Hard ICs Using Commercial Foundries

D. Wilkin
Aeroflex, Inc., Colorado Springs, CO

Aeroflex Colorado Springs will present their roadmap for the continued development of rad-hard integrated circuits using commercial wafer foundries. Products built on 0.6-, 0.25-, and 0.18-μm CMOS commercial silicon using a combination of design hardness and/or co-processing techniques will be summarized.

P.17: (4.8) Rad-Hard Technology Roadmap for Microelectronics and Space Computers

D. R. Czajkowski, D. J. Strobel
*Space Micro, Inc., San Diego, C**A***

The ability to leverage advanced commercial COTS microelectronics is critical to providing warfighters capability. Space Micro's technology roadmap, products, and techniques, which enable use of COTS in a radiation environment, will be described.

P.18: (4.9) Actel Corp.'s Technology Roadmap

B. Cronquist, C Clardy, K. Oneill, T. Farinaro
Actel Corp., Mountain View, CA

Actel Corporation's product roadmap for high-reliability applications will be presented. Both the non-volatile one-time programmable (OTP) FPGA and the non-volatile re-programmable FPGA roadmap will be discussed. Commercial, MIL-TEMP, rad-tolerant, and rad-hard efforts will be described. Special mention will be given to the definition, content, and schedule for the radiation-tolerant non-volatile re-programmable field-programmable gate-array (RTNVRFPGA) product family. The Actel packaging roadmap for high-reliability applications will also be presented.

WEDNESDAY, 6 APRIL

Session 7

ARRAY TECHNOLOGIES

Wednesday, April 6 / 8:30 – 10:10 am / Grande Ballroom C

Chair: **Christopher D. Lesniak**
AFRL, Wright Patterson AFB, OH

7.1: Converting Ceramic Phased-Array Modules to Plastic Phased-Array Modules (8:30)

D. Helms, R. Anderson, J-P. T. Lanteri
M/A-COM, Lowell, MA

A 9-W T/R L-band plastic packaged module achieves comparable performance with a traditional LTCC module. A plastic package lead frame and matching IC have been designed to compliment an existing TR module IC. Package NRE and reocurring cost are dramatically lower. Package volume as well as weight has been reduced.

7.2: Highly Integrated L-band T/R Module RF Performance (8:50)

M. Walker, R. Thornton, P. Schurr, S. R. Nelson
REMEC, Richardson, TX

The RF performance of highly integrated, high-efficiency (>40% PAE transmit path) L-band T/R modules will be described. These modules were designed for AFRL to support future space-based-radar low-cost lightweight arrays. Each module contains five MMICs in a 0.8-square-inch 10-layer LTCC package. A demonstration of a white-cell true-time-delay device (a quartic cell), providing 81 delays from 3 psec to 19 nsec, will be reported. Delays were accurate to within a fraction of a picosecond.

7.3: Wideband Random Phased Arrays: Cost-Effective Multifunction Performance (9:10)

J. T. Bernhard, G. Cung, K. C. Kerby, P. E. Mayes
The University of Illinois, Urbana, IL

The development of a random array design based on a low-profile canted antenna that delivers instantaneous wideband operation will be described. Design approaches for the random arrays that provide good sidelobe performance over frequency while remaining practical and cost effective to fabricate and operate will be discussed.

7.4: Multilayered Liquid-Crystal Polymer (LCP) AESA with Intregal MEMS Phase Shifters (9:30)

L.G. Chorosinski, J. D. Hartman, E. A. Capelle, D. W. Bever
Northrop Grumman ES, Baltimore, MD

Liquid-crystal polymer (LCP) substrates offer significant cost, weight, and performance benefits compared to conventional substrates, not only for circuit cards but for micro-machined and microelectromechanical system (MEMS) devices too. Direct fabrication of MEMS RF switches on multilayered substrates can enable production of more-affordable high-performance electronically steered arrays. The development of suitable processes for manufacturing MEMS RF switches on LCP substrates will be demonstrated.

7.5: X- and Ku-Band T/R, TTD, and PA MMICS (9:50)

J. Dishong, G. Clark, D. White, S. Yok,
REMEC, Richardson, TX

Highly integrated small-area X- and Ku-Band transmit/receive (T/R), true-time delay (TTD), and high-power high-efficiency amplifier MMICs have been designed for AFRL by REMEC to support future radar low-cost light-weight arrays.

BREAK (10:10–10:40)

Session 8

TECHNOLOGY FOR FREQUENCY AGILE DIGITALLY SYNTHESIZED TRANSMITTERS (TFAST)

Wednesday, April 6 / 8:30 – 10:10 am / Grande Ballroom D

Chair: **John Zolper**
DARPA/MTO, Arlington, VA

8.1: **High-Speed Direct Digital Synthesis Using Next-Generation InP HBT Technology** **(8:30)**

F. Stroili, R. B. Elder
BAE SYSTEMS, Nashua, NH

M. Feng
The University of Illinois, Champaign, IL

M. Le
Vitesse Semiconductor, Camarillo, CA

The development progress of a next-generation high-density InP HBT device and interconnect technology, as well as the implementation of a high-speed direct digital synthesizer, will be reported. This work is being performed under the DARPA TFAST (Technology for Frequency Agile Digitally Synthesized Transmitters) program.

8.2: **Super-Scaled InP DHBT Technology for High-Speed Direct Digital Synthesis** **(8:50)**

T. Hussain, D. Hitko, Y. Toyter, R Rajavel
HRL, Laboratories, LLC, Malibu, CA

A super-scaled InP DHBT technology with state-of-the-art performance will be described. A DHBT record-high f_t of ~420 GHz was measured for 0.4-mm emitter-width devices, while f_t and f_{max} simultaneously above 400 GHz were measured for 0.25-mm emitter-width devices. Static CML flip-flop toggling at 150 GHz will be reported.

8.3: **LSI-Compatible Submicron InP DHBT Technology for Frequency-Agile Digitally Synthesized Transmitters** **(9:10)**

B. Brar
Rockwell Scientific Co., Thousand Oaks, CA

M. Rodwell
University of California at Santa Barbara, Santa Barbara, CA

C. Nguyen
GCS, Torrrance, CA

InP DHBTs offer the highest speed-breakdown product of any transistor technology that offers suitable threshold control required for LSI circuits. Progress towards the fabrication of 20-GHz direct digital synthesizers chips will be reported.

8.4: Planarized InP/InGaAs Heterojunction Bipolar Transistors for Next-Generation Communication Systems **(9:30)**

D. Sawdai, P. C. Chang, V. Gambin, X. Zeng
Northrop Grumman Space Technology, Redondo Beach, CA

An advanced InP HBT technology has been developed, which enables a new class of high-speed mixed-signal applications for next-generation communication systems. This work demonstrates a novel HBT with reduced base-collector capacitance and submicron scaling for excellent RF performance.

8.5: InP DHBT High-Speed Direct Digital Synthesizer with Phase and Amplitude Modulation **(9:50)**

J. Matsui, A. Gutierrez-Aitken, B. Chan, E. Kaneshiro
Northrop Grumman, Redondo Beach, CA

Direct digital synthesizers (DDS) offer advantages over RF approaches in integrated radar, electronic warfare, and communications systems. A high-speed InP HBT-based DDS chip with phase and amplitude modulation, along with return-to-zero DAC and phase reset capabilities, will be presented.

BREAK **(10:10–10:40)**

Session 9

MICROWAVE CMOS

Wednesday, April 6 / 8:30 – 10:30 am / Grande Ballroom G

Chair: **Daniel J Radack**
DARPA/MTO, Arlington, VA

9.1: Super-Scaled CMOS for MMIC and Data Converter Applications (8:30)

M. F. Chang, J. Woo, K. Yang
UCLA, Los Angeles, CA

Recent advances in super-scaled CMOS makes it a viable candidate for implementation of MMIC and high-speed data converters. Issues involved in CMOS MMIC and data-converter design will be investigated. Innovative circuit techniques that may mitigate technology imperfections will be investigated. Examples that manifest the potential of CMOS circuits for system insertion will be described.

9.2: A 60-GHz Adaptive Beamforming Array in CMOS (8:50)

S. Alalusi, R. Brodersen
University of Califoirnia at Berkeley, Berkeley, CA

A 60-Hz adaptive beamforming array was implemented in standard 130-nm CMOS. The design is based on a vector-modulator phase shifter which operates at the full carrier frequency. The high-integration and digital computation of CMOS were utilized to overcome the shortcomings of CMOS circuits at these frequencies.

9.3: Digitally Assisted Analog Circuit Design for Communication SoCs (9:10)

T. H. Meng
Stanford University, Palo Alto, CA

The availability of high-speed network infrastructure and low-cost CMOS technology has dramatically changed the landscape of broadband communication in the past few years. To accommodate the ever increasing data rates, communication SoC design is no longer merely a circuit integration problem. The implementation of high-throughput communication SoCs with a power constraint requires a new design strategy for the embedded analog components.

9.4: Metal-Mask Configurable RF ICs (9:30)

L. T. Pileggi, Y. Xu
Carnegie Mellon University, Pittsburgh, PA

S. P. Boyd
Stanford University, Stanford, CA

Metal-mask configurable RF circuits using a base circuit fabric that can be robustly configured for various wireless applications to meet tight time-to-mission requirements will be described. A framework for optimization with recourse (ORACLE) for such configurable circuits demonstrates that a performance comparable to leading-edge full-custom designs can be achieved.

9.5: RF Subsystem for µNode SoC **(9:50)**

K. K. O, J. E. Brewer
University of Florida, Gainesville, FL

F. Martin
Motorola, Plantation, FL

Research enabling physically small single-chip all-CMOS short-range communication nodes (micro-nodes) is progressing. The viability of 24-GHz CMOS implementation of RF circuitry in 130-nm CMOS, practicality of on-chip antennas at 5-m distances, avoidance of the need for an off-chip crystal, and adequate noise isolation have been confirmed.

9.6 Fully Depleted SOI CMOS RF AMPLIFIERS **(10:10)**

C. L. Chen, R. Chang, P. W. Wyatt, C. K. Chen
MIT Lincoln Laboratory, Lexington, MA

Process modules have been added to the standard low-power fully depleted SOI CMOS technology to improve the performance of rf circuits. Several rf amplifiers at X- and Ku-bands will be reported, and no floating-body effects were observed. An amplifier with an adaptive bias control circuit demonstrated the integration of rf and digital circuits.

BREAK **(10:30–10:40)**

Session 10

ADVANCED PACKAGING

Wednesday, April 6 / 10:40 – 11:40 am / Grande Ballroom C

Chair: James C. Lyke
AFRL, Kirtland AFB, NM

10.1: A Self-Configuring Point-to-Point Backplane Architecture (10:40)

S. Cannon, J. Willis
Space Software Lab, Utah State University, Logan, UT

A self-contained space avionics communications architecture will be presented. This architecture offers a self-configuring reusable inter-payload communications system for a space avionics network. This platform provides point-to-point deterministically latent communications among payloads.

10.2: Progress on Reconfigurable Interconnections for Enhancing Plug-and-Play Avionics Flexibility (11:00)

G. Forman, J. Iannotti, C. Kapusta, W. Hinrichs
General Electric Co., Niskayuna, NY

The most-recent project progress and traction in driving emerging technology for faster integration efficiency and greater transparency of the data-transport physical layer for enabling plug-and-play avionics-based systems will be described.

10.3: Self-Aligned Polymeric Waveguide Interconnections for Efficient Chip-to-Chip Optical Coupling (11:20)

H. Xia, R. Guida, T. Gorczyca, K- L. Deng
General Electric Co., Niskayuna, NY

Optical coupling using self-written waveguides based on fiber connections has been investigated. This work has demonstrated that the self-written waveguide can greatly improve the light-coupling efficiency. Loss less than 1 dB can be obtained from SM to MM and SM to SM fiber interconnections, respectively.

LUNCH (11:40–1:30)

Session 11

RF PHOTONICS

Wednesday, April 6 / 10:40 am – 12:00 pm / Grande Ballroom D

Chair: Keith Williams
Naval Research Laboratory, Washington, DC

11.1: High-Performance Surface-Normal Modulators Based on Stepped Quantum Wells (10:40)

H. Mohseni, W. Chan, H. An, A. Ulmer
Sarnoff Corp., Princeton, NJ

Surface-normal modulators based on stepped quantum wells at / ~ 1.55 mm were demonstrated. These devices have nearly two times better efficiency and 7-dB higher extinction ratio compared to devices with rectangular and coupled-quantum-well active regions. Moreover, they show a 60-nm optical bandwidth, which should enable them to operate over an ~100°C temperature range.

11.2 Adaptive Post-Distortion for Photodetector Linearization (11:00)

J. Basak, B. Jalali
University of California at Los Angeles, Los Angeles, CA

Nonlinearities due to photodetector saturation limit the maximum dynamic range achievable in short fiber-optic links. An adaptive method for photodetector linearization using a monolithic CMOS polynomial generator has been demonstrated. Improvements of 16 and 5.1 dB were achieved in the second- and third-order limited dynamic ranges, respectively.

11.3: Wideband Frequency-Agile High-SFDR Receiver Front-End (11:20)

G. Silverman, J. SooHoo
Lockheed Martin, Newtown, PA

P. Yu, I. Schubin
University of California at San Diego, San Diego, CA

RF sensing and remoting of microwave receiver front-ends using photonics are essential to EW and ISR applications. Results of a hardware and applications development for microwave photonic components and systems will be presented. The technical objective is very high SFDR in a receiver system. Selected applications were demonstrated in brassboard hardware.

11.4: Quartic White-Cell-Based Optical True-Time Delays for Phased-Array Antennas (11:40)

B. L. Anderson, C. M. Warnky, R. Mital, S. A. Collins, Jr.
The Ohio State University, Columbus, OH

A demonstration of a white-cell true-time-delay device (a quartic cell) providing 81 delays from 3 to 19 nsec will be reported . Delays were accurate to within a fraction of a picosecond.

LUNCH (12:00–1:30)

Session 12

HIGH-PERFORMANCE SILICON

Wednesday, April 6 / 10:40 am – 12:00 pm / Grande Ballroom G

Chair: **Daniel J. Radack**
DARPA/MTO, Arlington, VA

12.1: SiGe HBT Technology Performance above 340 GHz (10:40)

D. C. Ahlgren, M. Khater, J.-S. Rieh, T. Adam
IBM Corp., Hopewell Junction, NY

Results from IBMs most recent generation of SiGe HBT device technology resulting in an f_{max} performance of 340 GHz with an f_t of 300 GHz and CML ring oscillators with gate delays of less than 3.3 psec per stage will be described.

12.2: Electronic-Warfare SoC Development Using IBM SiGe Technology (11:00)

F. Stroili, R. Elder, D. Jansen
BAE SYSTEMS, Nashua, NH

D. Rowe
Sierra Monolithics, Redondo Beach, CA

Electronic-warfare SoC development using IBM SiGe technology will be described. The progress on the development of a 30 MHz to 18 GHz electronic-warfare receiver-on-a-chip with 2 GHz of instantaneous bandwidth will be discussed. This work is being performed under the DARPA TEAM program. By utilizing IBM SiGe 8HP BiCMOS technology, a dramatic impact on the implementation of future DoD RF systems is expected.

12.3: Multi-Band Adaptable Microwave Mixed-Signal SiGe System-on-a-Chip (11:20)

M. Lucas, A. Turley, C. Marcelli, W. Hall
Northrop Grumman, Baltimore, MD

Technology which provides S-, X-, and Ku-band capability including integrated filtering, adaptive dynamic range, and bandwidth control will be described. Northrop Grumman's DARPA-sponsored TEAM Program is developing LNAs, mixers, delta-sigma modulators, decimation filters, and digital beamformers using the Jazz 200-GHz SiGe process to develop a complete receiver on a chip.

12.4: SiGe BiCMOS Technology for Receiver RF ICs (11:40)

P. Orlando, H. Axtell, C. Cerny, G. Creech
AFRL, Wright-Patterson AFB, OH

The development of RFICs using the 0.18-µm SiGe BiCMOS technology for next-generation DoD radar systems will be described. With the recent advancements in silicon technology for microwave applications, AFRL has been using SiGe BiCMOS technology for receiver-on-a-chip (ROC) technology demonstration. SiGe technology has been gaining wide acceptance for RF applications, especially in the commercial wireless market. Circuit results will be presented and the design of receiver RF front-end components suitable for future DoD radar systems will be described.

LUNCH **(12:00–1:30)**

Session 13

NANOTECHNOLOGY I

Wednesday, April 6 / 1:30 – 3:10 pm / Grande Ballroom C

Chair: **Joe E. Brewer**
University of Florida, Palm Coast, FL
Co-Chair: **Meyya Meyyappan**
NASA–AMES Research Center, Moffett Field, CA

13.1: The Search for Alternative, Energy Efficient, Scalable, Room Temperature, and Manufacturable Logic Technologies Beyond CMOS **(1:30)**

G. Bourianoff
Intel Corp., Austin, Texas

Intel believes that the FET device and CMOS implementation is a very robust and sophisticated structure that operates at close to optimum efficiency and can be scaled for at least another 15 years. The status of several alternative logic technologies, fabrication methods, and energy transport mechanisms that appear to have potential merits in the 2020 timeframe will be discussed.

13.2: Emerging Devices Beyond Scaleable CMOS: Mission of the Center on Functional Engineered Nano-Architectonics (FENA) **(2:10)**

K. Wang, K. Galatsis
UCLA, Los Angeles, CA

Y. Botros
Intel Corp., Los Angeles, CA

The Center on Functional Engineered Nano Architectonics (FENA) aims to create and investigate new nano-engineered functional materials, devices, and architectures for new information-processing systems beyond the limits of conventional CMOS technology. An overview of the FENA center will be given, and the latest achievements and research results will be presented.

13.3: A Non-Volatile Molecular Microswitch for Space-Based Memory Applications **(2:50)**

D. K. Brock, J. W. Ward, B. M. Segal, T. Reuckes
Nantero, Inc., Wobrun, MA

A CMOS-compatable thin-film manufacturing process is presented in which a “fabric” of single-walled carbon nanotubes can be freely suspended between metal electrodes to create a non-volatile mechanical switch. Electrostatic forces are used to modulate the state of the device, while molecular van der Walls forces allows the device to retain its state when power is removed.

LUNCH **(3:10–3:40)**

Session 14

POWER ELECTRONICS

Wednesday, April 6 / 1:30 – 3:10 pm / Grande Ballroom D

Chair: Fritz Kub
Naval Research Laboratory, Washington, DC

14.1: Development of SiC High-Power Electronics for CVN (1:30)

J. C. Zolper, S. Beerman-Curtin
DARPA/MTO, Arlington, VA

The HPE program is developing 10-kV components to address the power-conversion stations in the next generation of Naval Aircraft Carriers (CVN). SiC MOSFETs, IGBTs, and PIN diodes will be developed to support the demonstration of a prototype solid-state power substation that will replace the 10-m^3 6-ton transformers currently being planned for converting the 13.8-kV power bus down to the 460 V required to service loads.

14.2: A Road Map of Silicon-Carbide Power Devices (1:50)

J. Palmour
Cree, Inc., Durham, NC

Cree is engaged in the development of SiC power devices. With the commercialization of SiC Schottky diodes, a new era has been launched in power electronics. The next step will be the introduction of a SiC switch which, along with the SiC Schottky diode, will provide MHz switching capability in many DoD applications requiring a reduction in size, weight, and volume. A roadmap of these devices will be discussed.

14.3: Advanced Silicon Carbide Power Device Applications to the Air Force More-Electric Aircraft (2:10)

J. Scofield
AFRL, Wright-Patterson AFB, OH

Some of the critical device fabrication and performance issues that remain to be addressed and the results of converter, motor drive, and power supply application demonstrations achieved using current state-of-the-art device technology will be described in detail. Comparisons to comparable silicon device performance in the same component circuitry highlights the advantages of utilizing silicon carbide devices and underscores the tremendous potential of this emerging technology to revolutionize the military and commercial power electronics industry.

14.4: Metrology for High-Voltage High-Speed Silicon-Carbide Power Devices (2:30)

A. Hefner, D. Berning, C. Ellenwood
NIST, Gaithersburg, MD

Performance metrics and test instrumentation needs for emerging high-voltage high-speed SiC power devices will be described. Unique power device and thermal measurement test systems and parameter extraction methods were introduced and applied to assess performance of recently developed 10-kV SiC MOSFETs and PiN diodes.

14.5: Design and Fabrication of 10-kV Power Devices on 4H-SiC **(2:50)**

Q. Zhang, E. Hanna, B. Pierce, M. Gomez
Rockwell Scientific Co., Thousand Oaks, CA

10-kV 4H-SiC power devices developed at RSC will be reviewed: (1) PiN diodes with V_f of 3.94 V at 100 A/cm^2; (2) IGTO with R_{on} of 35.4 mΩ/cm^2 and 3.75-V turn-on voltage; (3) JFET with R_{on} of 168 mΩ/cm^2; and (4) a novel termination technique, simultaneous JTE (SJTE) for >10 kV with one time implantation.

BREAK **(3:10–3:40)**

GOMACTech–05 CONFERENCE SCHEDULE

THE RIVIERA HOTEL, LAS VEGAS, NEVADA

	GOMACTech Timetable	Ballroom Foyer	Grande Ballroom E	Grande Ballroom C	Grande Ballroom D	Grande Ballroom G	Capri 101	Capri 102	GOMACTech Timetable	
Monday, 4 April	10:00–5:00 pm	Registration	.....	.....	.....	.....	.....	.....	10:00–5:00 pm	Monday, 4 April
	1:00–3:00 pm	.....	.....	.....	.....	.....	**Tutorial 1** Nanotechnology	**Tutorial 2** Sensor Networks & Applications	1:00–3:00 pm	
	BREAK 3:00–3:30 pm								BREAK 3:00–3:30 pm	
	3:30–5:00 pm								3:30–5:00 pm	
Tuesday, 5 April	7:00–5:00 pm	Registration	.....	.....	.....	.....	.....	.....	7:00–5:00 pm	Tuesday, 5 April
	8:30–10:10 am	.....	.....	**PLENARY SESSION**		.....	.....	.....	8:30–10:10 am	
	BREAK 10:10–10:40 am	.....	.....	**BREAK**		.....	.....	.....	BREAK 10:10–10:40 am	
	10:40–12:00 pm	.....	.....	**PLENARY SESSION**		.....	.....	.....	10:40–12:00 pm	
	LUNCH 12:00–1:30 pm	.....	Exhibits (12:00–8:00 pm)	**LUNCH**					LUNCH 12:00–1:30 pm	
	1:30–3:10 pm	.....	.....	**Session 1** Rad-Hard Electronics and Systems	**Session 2** Sensor Urban Warfare	**Session 3** RF Power	.....	.....	1:30–3:10 pm	
	BREAK 3:10–3:40 pm	.....	.....	**BREAK**			.....	.....	BREAK 3:10–3:40 pm	
	3:40–5:20 pm	.....	.....	**Session 4** Rad-Hard Technology Roadmaps	**Session 5** DASS	**Session 6** Adaptive RF I	.....	.....	3:40–5:20 pm	
	5:20–6:30 pm	.....	**POSTER SESSION (Grande Ballroom H)**			**POSTER SESSION (Grande Ballroom H)**			5:20–6:30 pm	
	6:30–8:30 pm	.....	**RECEPTION (Exhibit Hall)**			**RECEPTION (Exhibit Hall)**			6:30–8:30 pm	
Wednesday, 6 April	7:00–5:00 pm	Registration	.....	.....	.....	.....	.....	.....	7:00–5:00 pm	Wednesday, 6 April
	8:30–10:10 am	.....	Exhibits (9:00–4:00 pm)	**Session 7** Array Technologies	**Session 8** TFAST	**Session 9** Microwave CMOS	.....	.....	8:30–10:10 am	
	BREAK 10:10–10:40 am	.....	.....	**BREAK**			.....	.....	BREAK 10:10–10:40 am	
	10:40–12:00 pm	.....	.....	**Session 10** Advanced Packaging	**Session 11** RF Photonics	**Session 12** High-Performance Silicon	.....	.....	10:40–12:00 pm	
	LUNCH 12:00–1:30 pm	.....	.....	**LUNCH**			.....	.....	LUNCH 12:00–1:30 pm	
	1:30–3:10 pm	.....	.....	**Session 13** Nanotechnology I	**Session 14** Power Electronics	**Session 15** MEMS Circuits & Packaging I	.....	.....	1:30–3:10 pm	
	BREAK 3:10–3:40 pm	.....	.....	**BREAK**			.....	.....	BREAK 3:10–3:40 pm	
	3:40–5:20 pm	.....	.....	**Session 16** Nanotechnology II	**Session 17** New-Millennium Program	**Session 18** MEMS Circuits & Packaging II	.....	.....	3:40–5:20 pm	
	6:30–10:00 pm	.....	**BANQUET**				**BANQUET**		6:30–10:00 pm	
Thursday, 7 April	7:00–5:00 pm	Registration	.....	.....	.....	.....	.....	.....	7:00–5:00 pm	Thursday, 7 April
	8:30–10:10 am	.....	.....	**Session 19** High-Performance Computing	**Session 20** VISA I	**Session 21** Photonics I	.....	.....	8:30–10:10 am	
	BREAK 10:10–10:40 am	.....	.....	**BREAK**			.....	.....	BREAK 10:10–10:40 am	
	10:40–12:00 pm	.....	.....	**Session 22** Adaptive RF II	**Session 23** VISA II	**Session 24** Photonics II	.....	.....	10:40–12:00 pm	
	LUNCH 12:00–1:30 pm	.....		**GOVERNMENT APPLICATIONS AND VISIONS LUNCH**			.....	.....	LUNCH 12:00–1:30 pm	
	1:30–3:10 pm	.....	.....	**Session 25** Electronics for Extreme Environments I	**Session 26** Wide-Bandgap Semiconductors I	**Session 27** Rad-Hard by Design I	.....	.....	1:30–3:10 pm	
	BREAK 3:10–3:40 pm	.....	.....	**BREAK**			.....	.....	BREAK 3:10–3:40 pm	
	3:40–5:20 pm	.....	.....	**Session 28** Electronics for Extreme Environments II	**Session 29** Wide-Bandgap Semiconductors II	**Session 30** Rad-Hard by Design II	.....	.....	3:40–5:20 pm	

Session 15

MEMS CIRCUITS AND PACKAGING I

Wednesday, April 6 / 1:30 – 3:10 pm / Grande Ballroom G

Chair: **Chuck Goldsmith**
MEMtronics Corp., Plano, TX

15.1: Reconfigurable MEMS-Enabled RF Circuits for Spectrum Sensing (1:30)

T. Mukherjee, G. K. Fedder, H. Akyol, U. Arslan
Carnegie Mellon University, Pittsburgh, PA

Micromachining in RF foundry processes enhances inductor and capacitor quality factors, increases varactor tuning range, and supports creation of electromechanical mixer filters that downconvert from GHz to MHz with built-in frequency selectivity. An on-chip parallel receiver architecture and circuit blocks incorporating these devices for low-power operation will be introduced.

15.2: Wideband and Multi-Octave MEMS-Reconfigurable RF Power Amplifiers (1:50)

S. Lardizabal
Raytheon RF Components, Andover, MA

B. Pillans, A. Malczewski
Raytheon Company APC, Dallas, TX

R. Molfino
Raytheon Integrated Defense Systems, Tewksbury, MA

Two adaptable microwave power amplifiers demonstrate frequency-agile tuning for the first time over wideband and multi-octave frequency ranges. Adaptable half-watt power amplifiers cover 8–12-GHz and 2–18-GHz frequency bands. Integrating and packaging MEM switching technology into a GaAs PHEMT process is a key enabler.

15.3: Reliability Improvements in RF Capacitive MEMS Switches (2:10)

C. F. Kirby, R. M. Young, G. E. Dix, C. A. Capelle
Northrop Grumman Corp., Linthicum, MD

Two failure mechanisms in RF MEMS capacitive switches have been identified: debris generation that causes the switch not to fully close and charge trapping which prevents the switch from fully opening. Mitigation/elimination of these mechanisms has led to improved switch reliabilities of 20 billion cycles (N50).

15.4: 20-GHz Distributed MEMS Phase Shifter Using Lateral Deflection MEMS Switches (2:30)

P. Chang-Chien, R. Stokes, D. Duan, K. Tornquist
Northrop Grumman Space Technology, Redondo Beach, CA

Four-bit 20-GHz distributed MEMS transmission line (DMTL) phase shifters have been demonstrated at NGST using lateral deflection RF MEMS switches. These DMTLs have RMS phase errors of ~1 with power- handling capability of >1 W. Excellent switch uniformity and device yield making these lateral deflection MEMS switches suitable for large-array applications.

15.5: Packaging Technology for RF MEMS Switches (2:50)

D. Peroulis, L. P. B. Katehi
Purdue University, West Lafayette, IN

Y. Lu
University of Michigan, Ann Arbor, MI

RF MEMS switches impose very challenging performance and cost requirements that are not met by todays packaging technology. Two alternatives to overcome this challenge will be presented. The first analyzes advanced packaging schemes, while the second focuses on novel contact-less RF MEMS architectures with significantly more-forgiving packaging needs.

BREAK (3:10–3:40)

Session 16

NANOTECHNOLOGY II

Wednesday, April 6 / 3:40 – 5:20 pm / Grande Ballroom C

Chair: **Joe E. Brewer**
University of Florida, Palm Coast, FL
Co-Chair: **Meyya Meyyappan**
NASA–AMES Research Center, Moffett Field, CA

16.1: Post-CMOS: Biologically Inspired Computing (3:40)

D. Hammerstrom
Portland State University, Portland, OR

Computational models inspired by biology, in particular, computational neuroscience, have much promise as an alternative to traditional computing models. This is especially true for molecular scale implementation. The state of the art in neurobiological modeling and how such models might map to nano/molecular scale devices will be discussed.

16.2: Using Time and Redundancy for Nanocomputation (4:20)

J. Fortes, V. Ravinuthula, J. Harris, R. Figueiredo
University of Florida, Gainesville, FL

Based on previous work on time-based analog computation and new ideas on how to quantize time, this paper proposes principles and building blocks for digital time-based computation. Both nanoscaled CMOS and single-electronics device technologies were considered in strawman designs for the needed blocks. Where nanosystems, including memories and FPGA-like systems, are implemented as addressable arrays of nanocells, hierarchical redundancy schemes using spares and error codes were proposed for fault-tolerance purposes.

16.3: Carbon-Nanotube Mid-Infrared Detectors Overlaid on Long-Infrared Focal-Plane Array (5:00)

N. Xi
Michigan State University, East Lansing, MI

H. Szu, J. Buss
ONR, Arlington, VA

To reduce the noise-equivalent temperature in infrared sensors, carbon nanotubes (CNTs) were used as sensing materials because of its one-dimensional ballistic electronic-transport property. By simply modifying the shape of the CNT using a nano-robotic assembly system, the band gap of a CNT can be tuned to 3–5-μm wavelengths of infrared radiation. The new architecture of an optical co-axial pixel plane was designed such that the 3–5-μm wavelengths detectors are overlaid above the 8–12-μm-wavelength focal-plane array (FPA). The co-axial pixel plane is fabricated through the nano-robotic assembly system.

Session 17

NEW MILLENNIUM PROGRAM

Wednesday, April 6 / 3:40 – 5:20 pm / Grande Ballroom D

Chair: Raphael Some
Jet Propulsion Laboratory, Pasadena, CA

17.1: DS2 Follow-on Experiment: Validation of DS2-Mars-Microprobe Impact-Surviving Technology (3:40)

B. Blaes, S. D'Agostino
Jet Propulsion Laboratory, Pasadena, CA

An instrumented probe designed to impact the ground at ~180 m/sec has been developed and field tested using an air gun. The probe design and impact tests were successful at validating the impact-surviving design principles used in the building of NASA's New Millennium Deep Space-2 (DS2) Mars microprobe.

17.2: The Space Technology 5 Microsatellite Technology and Constellation Science Validation Mission (4:00)

E. Webb, C. Carlisle, J. Slavin
NASA-GSFC, Greenbelt, MD

The Space Technology 5 (ST-5) Project is part of NASA's New Millennium Program that consists of a constellation of three 25-kg-class micro-satellites. The goals are to demonstrate the research-quality science capability of the ST-5 spacecraft, to operate the three spacecraft as a constellation, and to design and flight-validate three microsatellites with new technologies. A 3-month flight-demonstration phase, beginning in March 2006, will validate the ability to perform science measurements, as well as the technologies and constellation operations.

17.3: Flexible Architecture for Advanced System Thermal Management (4:20)

D. Bugby, E. Kroliczek, J. Yun, J. Garzon
Swales Aerospace, Beltsville, MD

A flexible two-phase-loop-based architecture for advanced system thermal management will be described. The architecture, denoted as the multi-evaporator hybrid loop heat pipe (ME-HLHP), combines capillary pumped loop (CPL) expandability and temperature controllability with loop-heat-pipe (LHP) operational robustness. Six specific implementations of ME-HLHP technology will be described.

17.4: Miniature-Loop Heat Pipe with Multiple Evaporators for Thermal Control of Small Spacecraft (4:40)

J. Ku, L. Ottenstein, D. Douglas
NASA/GSFC, Greenbelt, MD

M. Pauken
Jet Propulsion Laboratory, Pasadena, CA

A miniature loop heat pipe having multiple evaporators and deployable radiators with variable emittance coatings on the radiators has been designed, fabricated, and tested. It combines the functions of variable conductance heat pipes, thermal switches, thermal diodes, and the state-of-the-art LHPs into a single integrated thermal system. Experimental results showed excellent performance and correlated well with theoretical predictions.

17.5: The Space Technology 7 Disturbance Reduction System (5:00)

W. Folkner
Jet Propulsion Laboratory, Pasadena, CA

The Space Technology 7 project will validate system-level technologies for future gravity and formation-flying missions. ST7 will control the spacecraft position relative to freely floating test mass to within 10 nm using colloidal micro-thrusters. The ST7 components will be flown as part of the European Space Agency LISA in mid-2008.

17.6: New Millennium Program ST6: Autonomous Technologies for Future NASA Spacecraft (5:20)

A. B. Chmielewski, S. Chien, and R. Sherwood
Jet Propulsion Laboratory, Pasadena, CA

W. Wyman, T. Brady, S. Buckley, and C. Tillier
Charles Stark Draper Laboratory, Inc., Cambridge, MA

The purpose of NASA's New Millennium Program (NMP) is to validate advanced technologies in space and thus lower the risk for the first mission user. The focus of the NMP is only on those technologies which need space environment for proper validation. The ST6 project has developed two advanced, experimental technologies for use on spacecraft of the future. These technologies are the Autonomous Sciencecraft Experiment and the Inertial Stellar Compass. These technologies will improve the spacecraft's ability to make decisions on what information to gather and send back to the ground and to determine its own attitude and adjust its pointing.

Session 18

MEMS CIRCUITS AND PACKAGING II

Wednesday, April 6 / 3:40 – 4:40 pm / Grande Ballroom G

Chair: **Chuck Goldsmith**
MEMtronics Corp., Plano, TX

18.1: High-Performance Packaging of RF MEMS Switches and Circuits (3:40)

C. D. Nordquist, C. W. Dyck, B. Jokiel
Sandia National Laboratories, Albuquerque, NM

T. Lemp
Orion International, Albuquerque, NM

High-quality packaging is essential for achieving good performance, high yield, and low cost in MEMS-based circuits. This presentation will cover issues associated with several RF MEMS packaging approaches, including using commercial packages for parallel reliability testing, custom circuit packages using LTCC, and wafer-level bonded packages.

18.2: Wafer-Level Microencapsulation (4:00)

D. Forehand, C. Goldsmith
MEMtronics Corp., Plano, Texas

Microencapsulation is an innovative wafer-level packaging method for hermetically encapsulating RF MEMS switches. This packaging scheme has already demonstrated < 0.1-dB package insertion loss up through 50 GHz. This presentation overviews the processes, performance, and testing methods used for testing the hermeticity and insertion loss of individual encapsulated RF MEMS devices.

18.3: Wafer-Level RF MEMS Package (4:20)

E. Brown
Physical Domains, Inc., Los Angeles, CA

S. Cheung, M. Cohn, G. Kim
MicroAssembly Technologies, Inc., Richmond, CA

Packaging of RF MEMS poses multiple challenges, including loss, hermeticity, process temperature, and economics. In particular, substantial loses are associated with seal rings and thru wafer vias. Novel packaging approaches are enabled by a transfer process. This transfer process is wafer-scale and uses only inorganic non-outgassing materials.

18.4: Hermetic Thin-Film Encapsulation for RF MEMS Switches (4:00)

J. L. Ebel, R. Cortez, K. D. Leedy, R. E. Strawser
AFRL, Wright-Patterson AFB, OH

AFRL has developed, fabricated, and tested working RF MEMS switches in hermetic thin-film encapsulations. The hermeticity of the enclosures has been verified using a vacuum RF testing process. The method of forming the packaging, as well as the method of verifying hermeticity, will be presented.

18.5: Advanced RF MEMS Packaging (4:00)

J. Muldavin, C. Bozler, S. Rabe, C. Keast
MIT Lincoln Laboratory, Lexington, MA

MIT Lincoln Laboratory has developed a wafer-scale low-loss broad-band RF MEMS packaging technology. The fabrication includes CMOS-compatible front-end processing and thick Au back-end processing. Au thermocompression bonding was used to mate a metal-coated capping wafer to a device wafer, offering high-isolation and low-loss transmission lines within the cavity. Hermetic thru-wafer vias carry the rf signal in and out of the package through the 25-μm-thick device wafer. A packaged 100-μm-long transmission line with 0.06 and 0.1 dB total insertion loss at 20 and 50 GHz, respectively, has been demonstrated. The packaged transmission line has a 0.96-dB/cm attenuation at 40 GHz and less than $\pm 1^{\circ}$ phase error from dc to 50 GHz for a 10.8-mm-long line. The isolation of closely spaced lines will also be presented. Hermeticity was evaluated with *in-situ* moisture sensors after submission to an autoclave environment for 10 hours.

THURSDAY, 7 APRIL

Session 19

HIGH-PERFORMANCE COMPUTING

Thursday, April 7 / 8:30 –10:10 am / Grande Ballroom C

Chair: John Grosh
Office of the Secretary of Defense, Rosslyn, VA

19.1: Multiprocessor Performance for Polymorphous Computing Systems (8:30)

D-I. Kang, S. P. Crago, J. Suh, C. Chen, M. C. French
University of Southern California / Information Sciences Institute, Arlington, VA

Polymorphous computing architectures are being developed to provide high performance across a wide range of DoD applications. A multiprocessor PCA prototype system will be described and measured application and communication performance results for a polymorphous architecture will be provided.

19.2: Mapping Signal-Processing Kernels to Tiled Architectures (8:50)

H. Hoffmann, J. Lebak
MIT Lincoln Laboratory, Lexington, MA

A key feature of many new computer architectures is that they are composed of multiple tiles, each of which is a fully capable processor. Examples of tiled architectures include many under development for the DARPA/IPTO Polymorphous Computer Architectures (PCA) program. A programming paradigm called stream algorithms which has been shown to achieve high performance on tiled architectures will be described.

19.3: Smart Memories: A Configurable Processor Architecture for High-Productivity Parallel Programming (9:10)

M. Horowitz, C. Kozyrakis, K. Olukotun, K. Mai
Stanford University, Stanford, CA

Smart memories are a novel architecture for next-generation general-purpose processors for highly parallel computations. Smart memories use a configurable memory system to support high-productivity high-performance parallel programming with streams or transactions for a wide range of regular and unstructured applications.

19.4: High-Performance Embedded Computing Systems for the Next Decade (9:30)

K. V. Palem, S. Yalamanchili
Georgia Institute of Technology, Atlanta, GA

The landscape of customization techniques for high-performance embedded computing (HPEC) systems will be described. As an illustrative example, experiences and performance results for compilation and optimization of the MONARCH polymorphic computing architecture will be presented. The presentation concludes with a strategy for sustaining cost/performance growth for HPEC systems in the next decade.

19.5: Breaking the GOP/Watt Barrier with EDGE Architectures **(9:50)**

D. Burger, S. W. Keckler
The University of Texas at Austin, Austin, TX

The power efficiency (performance/Watt) of a new Explicit Data Graph Execution (EDGE) microprocessor architecture targetted at high-performance and embedded computing will be exaimed. The inherent structural power advantages of EDGE architectures over conventional high-performance architectures will be explored.

BREAK **(10:10–10:40)**

Session 20

VERTICALLY INTEGRATED SENSOR ARRAYS (VISA) I

Thursday, April 7 / 8:30 – 10:10 am / Grande Ballroom D

Chair: **Ray Balcerak**
DARPA/MTO, Arlington, VA

20.1: Recent Developments in Vertically Integrated Sensor Arrays (8:30)

C. Fletcher, M. Skele, R.W. Graham, M. Tang
Raytheon Vision Systems, Goleta, CA

3-D vertically interconnected sensor arrays have been developed. These focal-plane-array assemblies have been processed from whole wafers down to individual stacked die with dense via interconnects. Raytheon Vision Systems has been working with the State University of New York on the Vertically Integrated Sensor Array program, a technology-development program funded by DARPA. This program was tasked with developing 3-D stacked ROICs for imaging sensors, and also the development of high-performance circuitry which will reside in the 3-D ROIC stack.

20.2: Vertically Interconnected Sensor Array (VISA) Technology for High-Operating-Temperature HgCdTe Focal Plane Arrays (8:50)

J. Robinson, L. Wood, T. Murphy, P. Coffman
DRS Infrared Technologies, Plano, TX

HgCdTe focal-plane arrays offer the ultimate in IR sensitivity and have found widespread application in the highest-performance IR military systems. VISA technology is being development to achieve even higher-performance levels by providing increased signal processing at the pixel level for applications such as laser-jamming avoidance, active imaging, and multicolor FPAs.

20.3: High-Density 3-D Interconnect Technology for Massively Parallel Signal Processing in IR FPAs (9:10)

D. Temple, D. Malta, B. R. Stoner, C. A. Bower
MCNC-RDI, Research Triangle Park, NC

3-D interconnect technology has the potential to dramatically enhance signal-processing capabilities of high-resolution staring focal-plane-array (FPA) devices. The technology provides for heterogeneous integration of the 2-D detector arrays with multiple layers of silicon ICs by means of insulated and metallized vias etched through the body of the IC chips.

20.4: Process Development of Z-Axis Interconnects Using Fine-Pitch Through Silicon Vias (9:30)

L. Schaper, S. Spiesshoefer, S. Burkett, G. Vangara
University of Arkansas, Fayetteville, AK

The University of Arkansas has been working on an alternative through-silicon via (TSV) process technology for the VISA program. The goal has been to create thin, freestanding silicon slices for subsequent parallel assembly. The UA focus has been on producing TSVs using copper plating. Implementation of the UA process for TSVs has included five main fabrication areas: formation of the vias, deposition of the insulation and seed layers, copper plating, wafer thinning, and system integration. The project goal is to create high-aspect-ratio vias 4–6 μm in diameter on 20-μm pitch in wafers that are subsequently thinned to a thickness of about 20 μm.

20.5: VISA Architecture for High-Dynamic-Range Two-Color IR Focal Planes (9:50)

D. Cooper, J. Denatale, S. Lauxtermann, P. O. Pettersson
Rockwell Scientific Co., Camarillo, CA

A 3-D interconnect approach was developed based on fine-pitch high-aspect-ratio through wafer vias in relatively thick (250 μm) silicon wafers, enabling vertically interconnected sensor array (VISA) focal-plane arrays (IR FPAs). The mechanical durability of these thicker parts permits die-level assembly of known good die, using indium interconnect technology, increasing the ultimate yield of devices. The indium interconnect approach has been used to fabricate hybrid infrared focal planes for many years and is a mature technology. The extension to the VISA architecture requires that multiple layers be connected by depositing indium interconnects on both sides of the intermediate layers before mating.

BREAK (10:10–10:40)

Session 21

PHOTONICS I

Thursday, April 7 / 8:30 – 10:10 am / Grande Ballroom G

Chair: Ravindra Athale
DARPA/MTO, Arlington, VA

21.1: Optical Detection of Chemical-Warfare Agents and Toxic Industrial Chemicals (8:30)

C. Kumar, N. Patel
UCLA and Pranalytica, Santa Monica, CA

M. Webber, M. Pushkarsky, T. Macdonald
Pranalytica, Santa Monica, CA

The modeling of laser photoacoustic spectroscopy (L-PAS), which permits the attainment of a generalized performance evaluation methodology for CWA, and TIC sensors has been carried out. Both a detailed simulation as well as preliminary experimental results that show that tunable-laser-based L-PAS will be able to provide a sub-ppb sensor for CWAs and PFP less than one part in a million with a measurment time of less than 30 sec will be described. The analysis is applicable to any optical sensor and provides a generalized scheme for performance optimization.

21.2: Volume Bragg Gratings for Sensing and Processing Applications (8:50)

L. B. Glebov
University of Central Florida, Orlando, FL

New robust material for holographic optical elements has been created, which is a photo-thermo-refractive (PTR) glass. Transmitting and reflecting Bragg gratings with a diffraction efficiency up to 98% and an aperture up to 35 mm will be demonstrated. Application of these new elements for sensing and laser-beam control will discussed.

21.3: Infrared Photonics for Sensing Applications Using Chalcogenide Glasses

N. C. Anheier, J. F. Schultz
Pacific Northwest National Laboratory, Richland, WA

Recent developments at Pacific Northwest National Laboratory in the area of photonics for infrared sensing applications using chalcogenide glasses will be reviewed. Both direct-laser writing and holographic exposure techniques show promise for developing useful infrared photonic devices.

21.4: Coded Sampling for Increased Resolution and Higher Sensitivity Optical Spectroscopy and Imaging (9:10)

D. J. Brady, N. Pitsianis, M. Gehm, S. McCain
Duke University, Durham, NC

Multiplex codes and computational sensing enable the size (thickness and volume) of optical imagers and spectrometers to be reduced by several orders of magnitude while increasing sensitivity and resolution.

21.5: PANOPTES: A Thin Agile Multi-Resolution Imaging Sensor **(9:30)**

M. P. Christensen, S. Douglas, D. Rajan
Southern Methodist University, Dallas, TX

M. W. Haney
Univerisity of Delaware, Newark, DE

S. Wood
Santa Clara University, Santa Clara, CA

A thin agile multi-resolution imaging sensor called PANOPTES will be introduced. It is a tiled architecture consisting of micromirror arrays, detector arrays, and micro-optical elements. Individual tiles are directed to areas of the scene with increased information content, thereby matching the sensing capacity of the architecture to the scenes information content.

BREAK **(10:10–10:40)**

Session 22

ADAPTIVE RF II

Thursday, April 7 / 10:40 am – 12:00 pm / Grande Ballroom C

Chair: **Eric D. Adler**
Army Research Laboratory, Adelphi, MD
Co-Chair: **William D. Palmer**
Army Research Laboratory, Adelphi, MD

22.1: Integrated Spectral BIST Technique for IRFFE Systems (10:40)

J. M. Emmert
University of North Carolina at Charlotte, Charlotte, NC

J. A. Cheatham
Wright State University, Dayton, OH

The reconfigurable built-in self-test (BIST) technique for integrated mixed-signal (digital, analog, and RF) systems will be described. Unlike digital systems, BIST for analog and RF systems is difficult to develop due to the inexact nature of analog signals and the complexity of the test circuitry. By taking advantage of low-area-overhead techniques, a spectral BIST approach allows for the incorporattion of test-signal generation and the analysis of analog and RF systems on the same integrated die as the circuits themselves.

22.2: Adaptive Biasing of High-Efficiency X-band PAs for Power Control and Linearity (11:00)

Z. Popovic, D. Maksimovic, N. Wang, P. Bell,
V. Youzefzadeh, S. Pajic
University of Colorado, Boulder, CO

Multifunctional intelligent RF front ends require a variety of bias levels that can be dynamically adjusted to optimize performance. The adaptive efficiency optimization of a transmitter power amplifier (PA) will be addressed. X-band high-efficiency (> 60%) PAs are designed with efficient fast and slow feedback, which controls the bias to maintain efficiency while varying output power and/or improving linearity.

22.3: Toward a Multifunctional LFM-Waveform Communications/Radar System: Single-Crystal AlN-on-SiC SAW Filters for X Band (11:20)

G. N. Saddik, E. R. Brown
University of California, Santa Barbara, CA

A new breed of SAW filter based on single-crystal AlN, a material that has improved significantly in recent years with advances in nitride-compound epitaxy, will be addressed. Simulations for the SAW bandpass filter at X-band will be presented. Near-ideal insertion loss, bandwidth, and out-of-band rejection was observed. Presently, the device is in fabrication and experimental results will be reported.

22.4: Insulated-Gate PHEMT Switching Devices Fabricated with a Low-Temperature-Grown (LTG) GaAs Gate Insulator (11:40)

R. Actis, K. Nichols, D. Xu, X. Yang
BAE SYSTEMS, Nashua, NH

A novel insulated-gate PHEMT for use in low-loss Ka-band switch applications will be described. Using a highly insulating low-temperature-grown (LTG) GaAs material for the gate insulator, a submicrometer-gate-length PHEMT switch device has exhibited significantly improved switching characteristics over conventional PHEMTs, including a 1-Ω-mm on-state resistance (at several volts forward-bias) and a 20-V device breakdown voltage.

GOV'T APPLICATIONS & VISIONS LUNCH (12:00–1:30)

Session 23

VERTICALLY INTEGRATED SENSOR ARRAYS (VISA II)

Thursday, April 7 / 10:40 am – 12:00 pm / Grande Ballroom D

Chair: **Ray Balcerak**
DARPA/MTO, Arlington, VA

23.1: Advances in Lincoln Laboratory's 3-D Circuit Technology (10:40)

J. Burns, B. Aull, C. K. Chen, C. Keast
MIT Lincoln Laboratory, Lexington, MA

Functional 3-D ring oscillators and 1048 × 1048 visible imagers have been fabricated with Lincoln Laboratory's 3-D circuit-integration technology. The building blocks of the technology are fully depleted SOI technology circuit fabrication, precision wafer-wafer alignment, low-temperature oxide bonding, and the construction of dense 3-D electrical interconnections.

23.2: Electrical Model to Hardware Correlation of Through Wafer Vias for Wafer-Stacking Technology (11:00)

M. Lorsung
Mayo Clinic, Rochester, MN

One of the goals of DARPA's Vertically Interconnected Sensor Array (VISA) program is to provide an enabling technology for the stacking of silicon read-out integrated circuits (ROICs) where vertical through wafer vias provide connection from one chip to another in a chip sandwich stack. By providing a silicon stacking technology, additional functionality could be realized beneath each of the optical electrical transducers in a N x M detector array.

23.3: VISA Architectures for HDR and Low Light Detection

S. Kavusi, A. El Gamal
Stanford University, Stanford, CA

WITHDRAWN

Focal-plane-array architectures that take advantage of vertical integration to achieve unprecedented levels of performance will be described. Two schemes will be discussed: (1) folded-multiple capture with background subtraction that is capable of achieving over 20 bits of DR, at high fidelity and low power, and (2) correlated multiple sampling for achieving ultra-low light detection.

23.4: Focal-Plane Architecture with On-Chip ADC and Compression for High-Resolution High-Speed Digital Video Capture (11:20)

L. McIlrath, C. Cheung, J. Dowell
R3 Logic, Inc., Cambridge, MA

A new CMOS readout architecture that provides near lossless in-stream compression of 10-bit video data at rates up to 1000 frames per second on large focal-plane arrays will be presented. The correctness of the circuit design in performing all logic operations at data rates of interest has been fully tested and verified in fabricated prototype arrays. The architecture can be combined with different sensing materials through 3-D integration to permit imaging in different spectral regions.

GOV'T APPLICATIONS & VISIONS LUNCH (12:00–1:30)

Session 24

PHOTONICS II

Thursday, April 7 / 10:40 am – 12:00 pm / Grande Ballroom G

Chair: Ravindra Athale
DARPA/MTO, Arlington, VA

24.1: The Future of Optical Processing (10:40)

T. M. Turpin, C. Price
Essex Corp., Melbourne, FL

The future of optical processing will be projected based on the history of the technology and the common features of failed efforts and successful operational processors.

24.2: Ultra-Wideband Analog Optical Signal Processing of Complex Waveforms for Range Doppler Radar Measurements (11:00)

R. Reibel, K. D. Merkel
Scientific Materials Corp., Bozeman, MT

Z. Cole, D. E. Benson
Montana State University, Bozeman, MT

Real-time ultra-wideband (>2 GHz) analog signal processing is experimentally demonstrated utilizing electro-optical devices and spectrally selective optical materials. A range resolution of 20 cm and a Doppler resolution of 125 Hz has been demonstrated. Complex, large-time bandwidth product analog RF waveforms, including band-limited white noise, can be processed on S-, L-, and X-band carriers without down-conversion.

24.3: Broadband Blind RF Signal Separation with Optoelectronic ICA (11:20)

P. Smith, M. Baylor, K. Erickson, Z. Popovic
University of Colorado, Boulder, CO

An optoelectronic solution to the communications problem of blind-source separation for broadband RF signal sources will be presented. The independent component analysis (ICA) system is capable of dynamic 45–60-dB signal separation for a two-channel case. The signals are completely unknown, can have overlapping spectra, and can originate within a beamwidth of a small-aperture antenna array.

24.4: Light-Emitting Transistor Array for Optical Interconnect Application (11:40)

M. Feng, N. Holonyak, Jr., R. Chan, G. Walter
University of Illinois at Urbana-Champaign, Urbana, IL

The future applications and current progress of InGaP/GaAs heterojunction bipolar light-emitting transistor (HBLET) development for the electronics and optical communications application will be reported. DC and RF performance of an 80-Å QW embedded HBLET with an emitter mesa dimension of 6 x 7 m^2 will be reported. A fabricated device has a beta of 5, f_t of 14.5 GHz at an emission wavelength of 970 nm. The monolithically integrated 2 x 3 array operation of circular HBLETs will also be reported.

GOV'T APPLICATIONS & VISIONS LUNCH (12:00–1:30)

Session 25

ELECTRONICS FOR EXTREME ENVIRONMENTS I

Thursday, April 7 / 1:30 – 3:10 pm / Grande Ballroom C

Chair: **Elizabeth Kolawa**
Jet Propulsion Laboratory, Pasadena, CA

25.1: Considerations for the Operation of Electronics in Extreme Environments (1:30)

Elizabeth Kolawa
Jet Propulsion Laboratory, Pasadena, CA

During the next 20 years, NASA will be challenged to develop the necessary technologies to support missions to extremely diverse environments. In one extreme, Venus Surface Exploration missions require systems that are able to survive and operate in high-temperature (460°C) and high-pressure (90 bar) environments. Survivability in extremely high temperatures (380°C) and high pressures (1000 bar) is also required for deep atmospheric multiprobes to Giant planets. On the other extreme, Comet Nucleus Sample Return, Titan, Europa, and Moon exploration will require systems able to survive in extremely cold environments in the -140 to -230°C temperature range. In addition, the Europa mission presents a challenge of surviving in extremely cold temperatures (-160°C) and high-radiation (5 Mrad) environments. Missions to Mars present the challenge of surviving extreme temperature cycling (-120 to +20°C).

25.2: Using SiGe HBT Technology for Emerging Extreme Environment Electronics Applications (1:50)

J. D. Cressler
Georgia Tech, Atlanta, GA

It is argued that SiGe HBTs offers potential to simultaneously satisfy extreme environment electronics applications involving radiation tolerance, cryogenic temperatures, and/or high temperatures, potentially with little or no process modification, providing compelling cost advantages at both the IC and system level.

25.3: Emerging Heterogeneous Integration Technologies for Extreme Environment (2:10)

H. Sharifi, S. Mohammadi
Purdue University, West Lafayette, IN

M. M. Mojarradi
Jet Propulsion Laboratory, Pasadena, CA

A heterogeneous integration technology suitable for electronic packaging for harsh environments has been developed. The idea is to embed a Si (MEMS, III/V) chip inside a Si carrier substrate (glass, quartz, LCP) with seamless transitions between the chip and substrate. Interconnect lines with widths of 25 μm was easily fabricated.

25.4: Extreme-Environment Electronics by Design (2:30)

T. J. Thornton, H. Barnaby
Arizona State University, Tempe, AZ

B. J. Blalock
University of Tennessee, Knoxville, TN

M. M. Mojarradi
Jet Propulsion Laboratory, Pasadena, CA

Design techniques that can be used with conventional integrated-circuit processes for the development of low-cost electronic circuits and systems that operate reliably in extreme environmental conditions, including ultra-low, ultra-high, and ultra-wide temperature ranges combined with high radiation levels, will be presented.

25.5: Design, Modeling, and Characterization of Power MOSFET in 4H-SiC for Extreme-Environment Applications (2:50)

M. Hasanuzzaman, S. K. Islam, L. M. Tolbert
University of Tennessee, Knoxville, TN

The theoretical limitations of silicon-based switching devices for high-power and high-temperature applications can be overcome by the emerging material silicon carbide (SiC) and can be used in extreme environments, especially in hybrid electric-vehicle applications. An analytical model of a vertical DIMOS transistor structure, a frequently used switching device in power electronics system design, will be presented.

BREAK (3:10–3:40)

Session 26

WIDE-BANDGAP SEMICONDUCTORS I

Thursday, April 7 / 1:30 – 3:10 pm / Grande Ballroom D

Chair: Dave Via
AFRL, Wright-Patterson AFB, OH

26.1: Progress in Advanced PVT Growth of SiC Substrates for RF and High-Power Electronic Applications (1:30)

T. A. Anderson, D. L. Barrett, J. L. Chen, E. Emorhokpor
II-VI, Inc., Pine Brook, NJ

An advanced PVT (APVT) process for the growth of SiC single crystals has been developed. The proprietary process utilizes a high-purity SiC source and employs special measures aimed at the reduction of contamination by nitrogen, boron, and other background impurities. The APVT-grown material demonstrates concentrations of B and N reduced to about 2×10^{15} cm^3 and metals (Fe, Cr, Ni) to 10^{12}–10^{14} cm^{-3}. The X-ray scanning yields wafer maps of the Bragg reflection broadening (FWHM) as well as angular misorientation between the sub-grains. Representative samples were evaluated using EPR and photoluminescence, which give information on the nature of native point defects and their complexes.

26.2: Production-Scale MOCVD Growth of High-Power High-Frequency AlGaN/GaN HEMTs (1:50)

S. Guo, B. Albert, M. Pophristic, I. Eliashevich
EMCORE Corp., Somerset, NJ

AlGaN/GaN HEMTs are of interest for high-power and high-frequency device applications due to their superior material properties. MOCVD growth shows great promise for volume production growth of high-performance AlGaN/GaN HEMTs on large-area substrates. For commercial applications, wafer size is a very important factor in final device cost, especially for power electronics, where individual devices can be quite large, up to several square millimeters. In this work, the production MOCVD growth of AlGaN/GaN HEMTs on 2- and 3-in. SiC as well as on 4-in. sapphire will be addressed. Results of epitaxial material characterization and RF device testing at frequencies from 2 to 40 GHz will be presented.

26.3: Progress in SiC MMIC Production Readiness and High-Efficiency GaN Amplifiers (2:10)

J. Milligan
Cree, Inc., Durham, NC

SiC MMIC and GaN device technologies have progressed rapidly over the last 3 years. High-power SiC MMICs are now being produced in quantity in a commercial MMIC foundry with high yield and reliability. The technology is now a serious consideration for many upcoming military systems as a higher-voltage alternative to high-voltage GaAs. Technical performance and yield statistics for a run of over 2000 high-power SiC MMICs will be presented. Additionally, SiC device reliability data will be presented, showing a minimum reliability of 10^6 MTTF hours at a T_J of 175°C.

26.4: DARPA WBGS GaN Materials Development at Raytheon **(2:30)**

J. Smolko, S. Brierley, W. Hoke, R. Hallock
Raytheon, Tewksbury, MA

State-of-the-art GaN technology, based on HEMT structures grown by MBE, has been developed. The current status of this development, both for GaN HEMT epitaxy and device performance, will be discussed. Results from a production GaN reactor showing good uniformity and reproducibility of AlGaN/GaN HEMT epi structures on SiC substrates up to 100 mm in diameter will be presented. State-of-the-art device results on 1.25-mm FETs demonstrating 10-GHz power-added efficiencies in excess of 60% at 30-V drain bias, with good performance maintained up to 50-V drain bias, will be presented.

26.5: AlGaN/GaN on SiC and on Si for RF Power Applications **(2:50)**

P. Saunier, C. Lee, D.C. Dumka, H.Q. Tserng
TriQuint Semiconductor, Richardson, TX

Excellent results have been achieved with GaN-on-SiC devices using field-plate gates; 8.6 W/mm with a 59% PAE at 10 GHz has been demonstrated. Recently, very promising performance using GaN-on-Si devices with 7 W/m has been demonstrated.

BREAK **(3:10–3:40)**

Session 27

RAD-HARD BY DESIGN I

Thursday, April 7 / 1:30 – 3:10 pm / Grande Ballroom G

Chair: **Daniel J Radack**
DARPA/MTO, Arlington, VA

27.1: Robust Optimization for Rad-Hard Analog/RF Circuits (1:30)

X. Li, J. Wang, K. Y. Tong, L. T. Pileggi
Carnegie Mellon University, Pittsburgh, PA

A novel robust-analog-design tool (ROAD) to minimize the impact of analog single-event transients due to ion strikes and circuit behavior uncertainty due to process variations will be presented. A low-noise-amplifier example was used to demonstrate the efficacy of the proposed methodology.

27.2: Rad-Hard by Design Approaches Applied to Structured ASIC Applications (1:50)

D. Mavis, P. Eaton, M. Sibley, M. Mostrom
ATK Mission Research, Albuquerque, NM

Special layout and circuit-design techniques were used to achieve radiation hardness to both total ionizing dose and single-event effects in high-density deep submicron structured ASICs. The approach promises to provide inexpensive high-performance rad-hard parts using commercial fabrication processes.

27.3: Implementation of High-Speed Circuits for Analysis of Single-Event Effects (2:10)

B. Randall, S. Currie, K. Fritz, J. Coker
Mayo Clinic, Rochester, MN

Under the DARPA/MTO Radiation Hardened by Design Program, Mayo Clinic Rochester is investigating SiGe BiCMOS technology for its tolerance to single-event effects. This analysis was accomplished through the implementation of test circuits as well as special test fixtures that enable the integrated circuits to be tested in a radiation chamber while operating at high speed. Results of this work will be presented.

27.4: One-Mask-Structured ASIC Technology for Cost-Effective Rad-Hard ICs (2:30)

B. Cox, P. Dewell
ViASIC, Durham, NC

D. Mavis, P. Eaton
ATK Mission Research, Albuquerque, NM

J. Kimerling
Triad Semiconductor, Winston-Salem, NC

Recent advances in HBD techniques for deep sub-micron designs enable fabrication of rad-hard ICs through commercial foundries. A unique one-mask-structured ASIC approach, designed with these techniques, enables affordable rad-hard ICs in low volume that contain high-quality digital circuits and future support for integrated mixed-signal capability.

27.5: Rad-Hard Library Synthesis (2:50)

W. P. Snapp, Z. A. Johnson, M. P. Baze, J. W. Clement
Boeing Airplane Co., Seattle, WA

Rad-hard mixed-signal libraries both for hardened and non-hardened commercial fabrication processes, such as provided by the dedicated rad-hard foundries and the DoD Trusted Foundry, are being developed. Innovative foundry flexible library synthesis and hardening-by-design techniques were used and the libraries were integrated into a silicon compiler EDA design flow. The methodology and results of this program will be reported.

BREAK (3:10–3:40)

Session 28

ELECTRONICS FOR EXTREME ENVIRONMENTS II

Thursday, April 7 / 3:40 – 5:20 pm / Grande Ballroom C

Chair: **Elizabeth Kolawa**
Jet Propulsion Laboratory, Pasadena, CA

28.1: Packaging Technology for Extreme-Environment Electronics (3:40)

R. W. Johnson, J. Williams
Auburn University, Auburn, AL

The challenges of packaging SiC power devices for high temperatures include high operating temperature, wide thermal cycle range, high currents, and high voltages. Ongoing research to develop suitable materials and processes for packaging SiC power devices, including high-temperature ohmic and Schottky contacts, die attach wire bonding, and passivation, will be discussed.

28.2: The Need for a High-Temperature Electronics Standard (4:00)

R. Normann
Sandia National Laboratories, Albuquerque, NM

Extreme environments require a complete solution before electronic control and data acquisition systems can be valued by the end customer. For the case of high temperatures (150°C and above), the elimination of all heat-shielding or active-cooling benefits the end consumer, justifying the added expense of extreme electronic components. Following two DOE-sponsored workshops, both small and large component manufacturers have asked for a "general" component standard to help unify the extreme environmental markets (*i.e.*, aircraft engines, automotive, deep drilling).

28.3: One-Year Well Test at 192.5°C (4:20)

R. Normann, J. Henfling, D. Chavira
Sandia National Laboratories, Albuquerque, NM

In October 2003, a complete high-temperature logging tool was deployed within a geothermal well. The well was 192.5°C, located on the Coso Navy test range. The tool contained a complete set of Honeywell HT SOI electronics, polyimide printed wiring board, wires, solders, pressure seals, interconnects along with Quartzdyne quartz pressure and temperature sensors. The results after the first year will be reported and suggestions for improvements will be described.

28.4: Model-Based Design Tools for Extreme Environments (4:40)

A. Mantooth, M. Vlach, J. Shields
Lynguent, Portland, OR

Model-based design (MBD) tools to predict the performance and useful life of electrical components and systems subjected to extreme environmental conditions will be described. These tools will consist of novel modeling tools and advanced system and data analysis capability.

28.5: Operation of a Boost Converter in an Extremely Low-Temperature Environment (5:00)

R. M. Nelms, D. He, C. Cutshaw
Auburn University, Auburn, AL

Power will be required for the electronic systems operating in the extreme cold environments for some future NASA missions. The focus of this effort is the investigation into the operation of a power converter at low temperatures using COTS components.

Session 29

WIDE-BANDGAP SEMICONDUCTORS II

Thursday, April 7 / 3:40 – 5:20 pm / Grande Ballroom D

Chair: Chris Bozada
AFRL, Wright-Patterson AFB, OH

29.1: Wideband and Low-Power AlGaN/GaN HEMT MMIC Robust Low-Noise Amplifier (3:40)

A. Kurdoghlian, H. Moyer, M. Micovic, D. Chow
HRL Laboratories, Malibu, CA

Superior RF power performance from GaN HFET technology has been demonstrated by several groups over GaAs pHEMT technology. GaN HFET technology also has strong potential for harsh-environment receiver applications due to the robust nature of GaN HFETs. Despite being wide-bandgap devices, GaN HFETs have demonstrated excellent noise performance at remarkably low bias power levels of less than 15 mW, which makes them ideal candidates for front-end receivers in phase-array antennas.

29.2: GaN for Ka-Band Solid-State Power Amplifiers (4:00)

M. Wojtowicz, R. Coffie, P-P. Huang, I. Smorchkova
Northrop Grumman Space Technology, Redondo Beach, CA

GaN technology is emerging as the superior microwave and millimeter-wave technology for solid-state power amplification for military, space, and commercial applications. The high breakdown voltage and good thermal conductivity of the AlGaN/GaN material system on SiC enables new levels of solid-state power and robust low-noise amplifier performance.

29.3: DARPA Wideband-Gap Semiconductor Technology Initiative (WBGSTI) Tri-Service Observations (4:20)

G. D. Via
AFRL, Wright-Patterson AFB, OH

S. C. Binari, E. Glaser
Naval Research Laboratory, Washington, DC

D. Judy
Army Research Laboratory, Adelphi, MD

Phase I of DARPAs Wide Bandgap Semiconductor Technology Initiative (WBGSTI) will be completed by the end of the 2004. Deliverables from this program, including substrates (SiC, AlN, and GaN), AlGaN/GaN HEMT epitaxy, and processed device wafers, are being evaluated by the Tri-Service team. A summary of Tri-Service observations will be presented. In addition to the baseline measurements, several critical experiments have been performed in response to technical challenges that have arisen during the program. Select experiments will be described and the findings discussed.

29.4: Highly Survivable Wideband GaN HEMT Low-Noise Amplifier (4:40)

J. M. Yang, S. Cha, Y.H Chung, M. Wojtowwicz
Northrop Grumman Space Technology, Redondo Beach, CA

GaN has emerged as the technology of choice for next-generation high-power electronics. However, its ability to handle high input power also makes it an ideal candidate for a highly survivable receiver component. This feature directly translates MMIC compaction and cost saving because no front-end protection circuitry is required. A wideband GaN HEMT low-noise amplifier using novel dual-gate topology is being designed, fabricated, and tested in fixture to demonstrate a suvivability of greater than 38 dBm.

29.5: Advanced GaN HFETs for Millimeter-Wave Applications (5:00)

M. Micovic, M. Delaney, J. Moon, A. Kurdoghlian
HRL Laboratories, Malibu, CA

The development of advanced GaN HFET technology for millimeter-wave applications will be reported. The GaN MMIC process, which has demonstrated excellent uniformity on four sapphire wafers and three SiC wafers, consistently yields low contact resistance, good buffer isolation, low gate leakage current, and good pinch-off characteristics.

Session 30

RAD-HARD BY DESIGN II

Thursday, April 7 / 3:40 – 4:40 pm / Grande Ballroom G

Chair: Daniel J Radack
DARPA/MTO, Arlington, VA

30.1: Advanced Electronics Technologies: Challenges for Radiation Effects Testing, Modeling, and Mitigation (3:40)

K. A. LaBel
NASA/GSFC, Greenbelt, MD

L. M. Cohn
DTRA, Ft. Belvoir, VA

As plans for space utilization of sub-100-nm digital CMOS technologies and ultra-high-speed mixed-signal technologies gather interest, the issues related to how radiation effects the performance of these technologies provide a significant challenge. These challenges will be discussed, with emphasis on single-event effects and total ionizing dose.

30.2: IBM Silicon Technologies in the Trusted Foundry Program (4:00)

G. Carlson
IBM RTP, NC

IBM will discuss the status of their participation in the Trusted Foundry program. This will highlight the advanced processes available under the program, and a description of how to engage in it

30.3: The Fabrication of Rad-Hard by Design Circuits through the Trusted Foundry (4:20)

D. Both, G. Etzold
NSA/TAPO, Ft. George G. Meade, MD

The Trusted Foundry provides access to leading-edge semiconductor fabrication services and assures the customers against loss of confidentiality or protection against exploitation of the supply chain. The progress employing multi-project wafers on the first runs will be descibed, the process for obtaining services will be reviewed, and future directions will be discussed.

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