GOMACTech-07

Government Microcircuit Applications
and
Critical Technology Conference

ADVANCE PROGRAM

"Countering Terror with Transitional Technologies"

March 19 – 22, 2007

Disney's Coronado Spring Resort
Lake Buena Vista, Florida

GOMACTech-07
ADVANCE PROGRAM
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WELCOME

The GOMACTECH-07 Program Committee is pleased to welcome you to this year's conference in Lake Buena Vista, Florida. GOMACTECH is the pre-eminent conference for the review of developments in microcircuit applications for government systems. Historically, the Conference has been the venue to announce major government microelectronics initiatives such as VHSIC, MIMIC, and others. GOMACTECH was established in 1968 and is an Unclassified, Export-Controlled event that requires all participants to be U.S. Citizens or legal U.S. Permanent Residents.

This year's conference theme, "Countering Terror with Transitional Technologies," provides a forum for the presentation and discussion of these advanced technological solutions and allow for interaction among technology developers and users. Defending the United States against the asymmetric threat of terrorist warfare has caused us to rethink our systems and methods – and once again recognize that advanced microcircuit and critical technologies beyond COTS are one of our key advantages. New technologies that can identify the presence of threats and enable rapid action to nullify them are essential to our security and our prosperity. The technical community of the United States is engaged in a race to create and mature the technologies and tools that will enhance our ability to protect our population and infrastructure while giving our warfighters an advantage over these asymmetric threats.

The conference will follow the successful format used over the past several years, with both technical and topical sessions. The technical sessions comprise contributed and solicited papers, including oral presentations and a Thursday morning Poster Session. The topical sessions will focus on developments and accomplishments within selected ongoing government-sponsored programs. Some of this year's topical session themes are

- 60–600-GHz Novel RF Source Technologies
- Critical Nuclear Detection Sensor Technologies for Homeland Security
- Electro-Optic Surveillance Technology for the GWOT
- High-Performance Integrated Electronics
- Technologies for Urban Warfare
- Trusted Foundry/Trusted Electronics

Two tutorials are offered on Monday afternoon with the cost included as part of the conference registration fee. One tutorial, "Nanotechnology and the nanoHUB," will feature an inside look at the Web site created at Purdue University by the Network for Computational Nanotechnology (NCN) and NSF, bringing together simulation tools and supporting resources to become a national resource for nanotechnology research and education. In the tutorial, "Imaging Through Adverse Environments (RF & IR)," leaders from academia, government, and industry will provide an overview of the latest phenomenology and technology used for security screening, imaging, and weapons detection in real environments.

The conference formally opens on Tuesday morning with an outstanding Plenary Session. Rear Admiral (RET) Jay M. Cohen, Under Secretary for Science and Technology in the Department of Homeland Security, will present the Keynote Address "DHS

Science & Technology Directorate: Moving Ahead." The Plenary Session includes the Kilby Lecture series, which features talks related to the conference theme given by distinguished members of the academic, industrial, and government research communities. This year's conference includes three excellent Kilby Lecturers. Thomas M. Reeves, VP, Semiconductor and Technology Services for the IBM Technology Group in Burlington, VT, will speak on the challenge, importance, and issues that advanced integrated circuit technologies bring to fighting and winning the Global War On Terror in the talk "Collaborative Technology Solutions for Semiconductors: A Case Study." Mr. Benjamin P. Riley, Director, Rapid Reaction Technology Office and Chairman, Combating Terrorism Technology Task Force at the Office of the Secretary of Defense, will present "Research and Technology Needs: Breaking the Terrorist/Insurgency Cycle." Prof. Kathleen Carley, Director of Center for Computational Analysis of Social and Organizational Systems (CASOS), part of the Institute for Software Research International in the School of Computer Science at Carnegie Mellon University, will conclude this year's Plenary Session with "Dynamic Network Approaches to Counter-Terrorism."

The Plenary, Technical, and Topical Sessions are the major venues for information exchange at the conference. Other opportunities for technical interaction are provided through the Exhibit Program that includes major IC manufacturers and commercial vendors of devices, equipment, systems and services for nearly all facets of the electronics business. The exhibition opens on Tuesday at noon and runs through Wednesday at 4:00 pm. On Tuesday evening, attendees can mix in a relaxing atmosphere of food and good spirits at an Exhibitors' Reception sponsored by Northrop Grumman Corp. Wednesday evening features the conference banquet, which will be held in the Wonders of Life Pavilion at Disney's Epcot Center, followed by a viewing of the light and sound show "IllumiNations: Reflections of Earth." The Thursday Government Applications and Vision Keynote Address will be presented during lunch, featuring COL Tim Kokinda, Assistant Chief of Staff, G6, XVIII Airborne Corps, Fort Bragg, NC, speaking on "Battle Command and C4I Lessons Learned from the XVIII Airborne Corps' Experience in Operation Iraqi Freedom."

This year's strong technical program reflects the hard work and enthusiasm of the GOMACTECH-07 Technical Program Committee. The committee members aggressively sought out particular topics and areas for presentations, and the quality of the conference certainly reflects this effort. It is our hope and belief that GOMACTECH-07 will be a rewarding experience for all participants. We appreciate your support.

Dev Palmer
Conference Chair

Gerry Borsuk
Technical Program Chair

REGISTRATION

All GOMACTech-07 sessions will be held at Disney's Coronado Springs Resort in Lake Buena Vista, Florida. Both check-in and on-site registration wil take place at North Registration Counter in the Resort's Convention Center.

Conference check-in and on-site registration hours:

Monday, 19 March – 10:00 am – 5:00 pm
Tuesday, 20 March – 7:00 am – 5:00 pm
Wednesday, 21 March – 7:00 am – 5:00 pm
Thursday, 22 March – 7:00 am – 5:00 pm

SECURITY PROCEDURES

The GOMACTech Conference is an Unclassified, Export-Controlled event that requires participants to be U.S. Citizens or legal U.S. Permanent Residents. All registrants must provide proof of U.S. Citizenship or Permanent Resident status prior to being permitted entry into the conference. Additionally, a signed **Non-Disclosure Statement** will be required.

You may prove U.S. citizenship with any one of the following:
U.S. Passport
Birth Certificate **AND** valid government-issued photo ID
Naturalization Certificate **AND** valid government-issued photo ID

The following are NOT proof of citizenship:
Voter registration card
Driver's license

GOMACTech TUTORIALS

Two tutorials of interest to the GOMACTech community are a special feature of the conference. There is no additional fee for the tutorials, but registrants must indicate their intention to attend on the registration form.

Tutorial 1: Using nanoHUB for Scientific Computing, Education, and Outreach

Monday, March 19, 1:00 – 5:00 pm
Disney's Coronado Springs Resort, Durango 1

Organizer:
Michael McLennan, Purdue University, West Lafayette, IN

nanoHUB.org is a Web site that brings together simulation tools and supporting resources for research, education, and outreach. It has been created by the Network for Computational Nanotechnology (NCN) and funded by the National Science Foundation (NSF) to become a national resource for nanotechnology research and education. In the past 12 months, more than 17,000 persons used nanoHUB to view seminars, tutorials, animations, homework assignments, and, most importantly, to run nanotechnology simulations.

Users can access interactive tool sessions from any Web browser – even with a dial-up connection. Clicking on the Simulate button on each tool's graphical interface launches a job on the nanoHUB's local cluster or sends the job to national grid resources, including the NSF TeraGrid and the Open Science Grid. This brings the power of grid computing to educators, experimentalists, and other researchers who otherwise might not have access.

In this tutorial, we will show how nanoHUB can be used to support education and outreach, as well as cutting-edge research activities.

After presenting a broad overview of the nanoHUB and its capabilities, we will focus in on two specific topics in nanoelectronics-ballistic nanotransistors and quantum dots, teach a little about the underlying science, and show how nanoHUB is used to bring these concepts to a wider audience. Then, we will teach attendees how to upload their own seminars and software, thereby using the nanoHUB cyberinfrastructure to promote their own research to a wider audience.

Tutorial 2: Imaging through Adverse Environments

Monday March 19, 1:00 – 5:00 pm
Disney's Coronado Springs Resort, Durango 2

Organizer:
H. Bruce Williams, *MMW Concepts LLC, Havre de Grace, MD*

In recent years, the field of terahertz (THz) science and technology has entered a completely new phase of unprecedented expansion that is generating ever-growing levels of broad-based international attention. One can legitimately argue that that the potential payoffs of THz sensing (and imaging) to applications areas such as defense, security, biology, and medicine are the major drivers of this new phenomenon. However, there remain major science and technology (S&T) "gaps" within the THz regime that must be reconciled before many of the perceived payoffs ever become realizable. This tutorial will present a number of talks on leading research efforts that are attending to close the S&T gaps with the long-range goal of enabling future sensing (and imaging) applications with relevance to the military and private sectors.

LUNCH SPEAKERS

Lunch will be provided on Tuesday, Wednesday, and Thursday.

Wednesday's Lunch will include a presentation by COL Barry Shoop, Science Advisor for the Joint Improvised Explosive Device Defeat Organization (JIEDDO), speaking on "Science in Support of JIEDDO."

Thursday's Lunch will include the Government Applications and Vision Keynote Address featuring COL Tim Kokinda, Assistant Chief of Staff, G6, XVIII Airborne Corps, Fort Bragg, NC, speaking on "Battle Command and C4I Lessons Learned from the XVIII Airborne Corps' Experience in Operation Iraqi Freedom."

EXHIBITION

An exhibition comprised of commercial vendors exhibiting products of interest to the GOMACTech community is an integral part of the conference. All attendees are reminded to visit the exhibit hall when they have some free time. The Exhibit Hall is located in the hotel's Coronado L Ballroom. Lunch and coffee breaks will be held in the exhibit area when they coincide with the exhibition's hours of operation. On Tuesday evening an Exhibitors' Reception, sponsored by Northrop Grumman, where attendees can mix in a relaxing atmosphere of food and good spirits, will be held.

Exhibition hours are as follows:

Tuesday, 20 March	1:00 pm – 8:00 pm
Wednesday, 21 March	9:00 am – 4:00 pm

Preliminary List of Exhibitors

BAE Systems

M/A-COM

NNSA's Kansas City Plant

Northrop Grumman

REMEC Defense & Space Science, Inc.

Sandia National Laboratories

Synopsys, Inc.

Synplicity, Inc.

WEDNESDAY EVENING DINNER AT EPCOT® WONDERS OF LIFE PAVILION

The Wednesday evening social event will be a buffet dinner held at the Epcot® Wonders of Life Pavilion, with the evening concluding with a viewing of *Illuminations: Reflections of Earth*.

Bus transportation will be provided.

Tickets should be purchased in advance along with your conference registration. Adults $25 Children (12 and under): $15.

HOTEL ACCOMMODATIONS

Inspired by the explorers who searched for the fabled Seven Cities of Gold, Disney's Coronado Springs Resort celebrates the character and traditions of the American Southwest and northern Mexico. Here, palm-shaded courtyards and Spanish-style haciendas create the perfect climate for business and pleasure. You can soak up the sun at a five-story Mayan Pyramid that towers over an elaborate themed pool area or indulge in the flavors of Mexico, the Caribbean, and South America at the Maya Grill. Conveniently located in Disney's Animal Kingdom® Resort area, Disney's Coronado Springs Resort is a stone's throw from all four Walt Disney World® Theme Parks, championship golf course, and Disney entertainment districts.

GOMACTech has reserved a block of rooms at the hotel at a special rate of $150 single or double occupancy. This rate is subject to applicable sales and resort taxes, currently 11.5%. Subject to availability, this group rate will be honored March 14-25, 2007.

To ensure the group rate, just log on to http://www.disneyurl.com/GOMACTech2007. Or, you can call the hotel reservation office at 407/939-1020.

Reservations received after the February 28, 2007 cut-off date will be accepted on a space and/or rate availability basis only.

CONFERENCE CONTACT

Anyone requiring additional information about GOMACTech should contact the Conference Coordinator, Ralph Nadell, GOMACTech, 411 Lafayette Street, Suite 201, New York, NY 10003 (212/460-8090 x203), Rnadell@pcm411.com.

GOMACTech '06 PAPER AWARDS

Paper awards based on audience evaluations from GOMACTech-06 will include the George Abraham Outstanding Paper Award and a Meritorious Paper Award. Presentation of these well-deserved awards will be made at the Plenary Session on Tuesday morning in Coronado J Ballroom. The GOMACTech-06 winners are:

The George Abraham Outstanding Paper Award (26.3)

H. Zhang, A. A. Pesetski, J. E. Baumgardner, and J. M. Murdock, Northrop Grumman, Linthicum, MD

"Low-Power High-Speed Carbon-Nanotube Field-Effect Transistors for Defense rf Electronics"

Meritorious Paper Award (28.2)

E. Snow, K. Perkins, and S. Stepnowski, Naval Research Laboratory, Washington, DC

E. Houser, TSA, Atlantic City, NJ

"Chemical Detection Using a Single-Walled Carbon-Nanotube Network Sensor"

RATING FORM / QUESTIONNAIRE

Don't forget to vote for your favorite presentation this year before you leave the conference. A rating form/questionnaire is being handed out at conference check-in. To encourage submission of these forms, GOMACTech has a special gift for all attendees submitting a completed form. Please turn your form in at the Conference registration desk when you leave the Conference to receive your gift item.

SPEAKERS' PREP ROOM

The El Paso 2 room is designated as a speakers' preparation room and will be available during the hours the conference registration desk is open. Speakers are encouraged to use the El Paso facilities to ensure compatibility with the meeting's AV equipment. Speakers having difficulties should request at the conference registration desk to see an AV operator. ***Speakers are also asked to be at their assigned presentation room 30 minutes before the sessions begins to meet with their session chair.*** An AV operator will be assigned to each technical session room.

CD-ROM PROCEEDINGS

A volume of the GOMACTech-07 CD-ROM Proceedings, containing searchable, condensed versions of submitted papers presented at the Conference will be distributed to all registrants. Additional copies of the CD-ROM can be purchased at the Conference at a cost of $40.00 per CD.

Previously published as the GOMAC Digest of Technical Papers, Volumes I – XXVIII, this publication is the only record of the conference. Previous GOMAC Digests will, upon request, made available copies to qualified Defense Technical Information Center (DTIC) users. Please call 1-800-225-3842 to order copies. Past Digests can be ordered by calling the above number and identifying the following accession numbers (please note that GOMAC was not held in the calendar year of 1995):

GOMAC-84 B113271	-86 B107186	-87 B119187
-88 B129239	-89 B138550	-90 B150254
-91 B160081	-92 B169396	-93 B177761
-94 B195015	-96 B212362	-97 B222171
-98 B235088	-99 B242763	-00 B254138
-01 B264749	-02 B275146	-03 M201604
-04 M201663	-05 M201849	-06 M202011

INFORMATION / MESSAGE CENTER

The Information/Message Center will be located adjacent to the GOMACTech Registration Desk. The message center telephone number for incoming calls is 407/824-2222. Callers should ask to be transferred to the GOMACTech Registration Desk.

PARTICIPATING GOVERNMENT ORGANIZATIONS

Participating Government Organizations of GOMACTech-07 include: Department of Defense (Army, Navy, Air Force) ... National Aeronautics and Space Administration ... Department of Commerce (National Institute of Standards and Technology) ... National Security Agency ... Department of Energy (Sandia National Laboratories) ... Defense Logistics Agency ... Department of Health and Human Services ... Defense Threat Reduction Agency ... Advisory Group on Electron Devices ... Defense Advanced Research Projects Agency ... Central Intelligence Agency ... National Reconnaissance Office ...

GOMACTech WEB SITE

Information on GOMACTech may be obtained through its Web site at www.gomactech.net.

TUESDAY

Session 1

PLENARY SESSION

Tuesday, 20 March / 8:30 am – 12:00 pm / Coronado J Ballroom

Opening Remarks **(8:30–8:45)**

William Dev Palmer, GOMACTech-07 General Chair
Army Research Office, Durham, NC

GOMACTech-06 Awards **(8:45–9:00)**

Keynote Address **(9:00–10:00)**

The Honorable Jay M. Cohen
Under Secretary for Science & Technology,
U.S. Department of Homeland Security, Washington, DC

"*DHS Science & Technology Directorate: Moving Ahead*"

BREAK **(10:00–10:30)**

Jack S. Kilby Lecture Series **(10:30–12:00)**

Thomas M. Reeves
VP, Semiconductor and Technology Services,
IBM Technology Group, Burlington, VT

"***Collaborative Technology Solutions for Semiconductors: A Case Study***"

Prof. Kathleen M. Carley
Director, Center for Computational Analysis of Social and Organizational Systems, Institute for Software Research, International School of Computer Science, Carnegie Mellon University, Pittsburgh, PA

"***Dynamic Network Approaches to Counter-Terrorism***"

Benjamin P. Riley
Director, Rapid Reaction Technology Office,
Chair, Combating Terrorism Technology Task Force,
Office of the Secretary of Defense, Washington, DC

"***Research and Technology Needs -- Breaking the Terrorist/Insurgency Cycle***"

LUNCH **(12:00–1:30)**

Session 2

NANOTECHNOLOGY FOR SYSTEMS I

Tuesday, March 20 / 1:30 – 3:00 pm / Coronado J

Chair: **Cliff Lau**
Institute for Defense Analyses, Alexandria, VA
Co-Chair: **Joe E. Brewer**
University of Florida, Melrose, FL

2.1: **The National Nanotechnology Initiative: Potential Impact on DoD** **(1:30)**

J. S. Murday
University of Southern California, Washington, DC

The National Nanotechnology Initiative is one of many global efforts addressing the S&T of nanostructures. The U.S. status in those efforts will be assessed and the impact anticipated on the DoD will be elaborated.

2.2: **Nanotechnology: From Devices to Circuits and Systems** **(1:50)**

M. Lundstrom
Purdue University, West Lafayette, IN

As silicon microelectronics becomes nanoelectronics, questions about its ultimate and practical limits and the possibilities of new technologies are being raised. Assessment of new technologies must consider both the device and systems aspects. A simple perspective on the challenges and opportunities for nanoelectronic devices and systems will be addressed.

2.3: **Design of Imperfection-Immune Carbon-Nanotube Field-Effect-Transistor Circuits** **(2:10)**

N. Patil, J. Deng, S. Mitra, H-S. P. Wong
Stanford University, Stanford, CA

Two fundamental limitations to circuit design using carbon-nanotube field-effect transistors (CNFETs) – misaligned tubes and metallic tubes – will be addressed. CNFET circuit-design techniques immune to such imperfections and related open questions will be discussed.

2.4: **Quantum-Tunneling-Based Systems on Mesoscopic and Nano Dimensions** **(2:30)**

P. Mazumder
University of Michigan, Ann Arbor, MI

Conventional shrinking methods to improve CMOS VLSI chip performance through the scaling of device and interconnect geometries in all three dimensions may continue until the channel length of transistors is reduced to about 40 nm, thereby possibly heralding the end of the present shrinking era. Thoughts about numerous formidable challenges that must be effectively grappled with to witness any spectacular return on investments made by numerous governmental and private agencies towards the R&D of promising emerging technologies for electronic, photonic, and biological systems will be shared.

BREAK **(3:00)**

Session 3

DISTORTION IN RF ELECTRONICS

Tuesday, March 20 / 1:30 – 3:00 pm / Coronado Q&R

Chair: **Michael B. Steer**
North Carolina State University, Raleigh, NC
Co-Chair: **William D. Palmer**
U.S. Army Research Office, Durham, NC

3.1: **Stochastic Simulation as an Aid to the Uncertainty Modeling of Sensors: Modeling Phase Noise in an Oscillator** **(1:30)**

M. Steer
North Carolina State University, Raleigh, NC

A basis of incorporating uncertainty in modeling will be discussed. Through modeling, understanding is gained and real world environments can be more precisely explored enabling sensing strategies to be developed. As a primitive example of what could be achieved, the modeling of large signal noise and flicker noise in an electronic circuit will be described. Extrapolation of this to sensing will be discussed.

3.2: **Measurements of High-Power Passive Components** **(1:50)**

W. Chappell, A. Christianson, J. Henrie
Purdue University, West Lafayette, IN

The effects of circuit-design choices on the passive intermodulation in high-power circuits will be discussed. The effect of the quality factor of matching circuits on passive intermodulation, for example, will be detailed. In addition, the presence of deep subharmonic patterns (up to the 17th order) or higher and the methods used to detect them will be discussed.

3.3: **Electrothermal Generation of Intermodulation Distortion in Film Resistors** **(2:10)**

K. Gard
North Carolina State University, Raleigh, NC

Instantaneous heat fluxuations modulate the instantaneous resistance in proportion to the instantaneous power of an applied communication signal, resulting in a self-mixing process which generates intermodulation products of the input signal. Electrothermal analysis, a self-heating resistor model, and measurements of intermodulation distortion generated by surface-mount resistors will be presented.

3.4: **Passive Intermodulation in Planar Interconnects Due to Ohmic-Loss Heating** **(2:30)**

A. Ramachandran, A. C. Cangellaris
University of Illinois at Urbana-Champaign, Urbana, IL

A methodology for the modeling of passive intermodulation in RF interconnects due to ohmic power loss and associated heating in the metallization have been developed. With interconnect geometry, material properties, and operating frequencies defined as input, the model provides for the quantification of passive intermodulation levels in the signal distribution network of RF and microwave printed-circuit boards.

BREAK **(3:00)**

Session 4

HIGH-PERFORMANCE INTEGRATED ELECTRONICS: SILICON RF

Tuesday, March 20 / 1:30 – 3:00 pm / Coronado S&T

Chair: **Daniel J. Radack**
Institute for Defense Analyses, Alexandria, VA
Co-Chair: **Michael Fritze**
DARPA/MTO Arlington, VA

4.1: **Silicon-Based Millimeter-Wave ICs for Gbps Wireless Communications and Radar Systems** **(1:30)**

B. Gaucher, B. Floyd, S. Reynolds, A. Valdes-Garcia
IBM T. J. Watson Research Center, Yorktown Heights, NY

The viability and suitability of silicon-based technologies, enablement tools, circuit design, and packaging for millimeter-wave applications today and a roadmap to the future has been established. Key elements to be discussed include SiGe, bulk CMOS, and SOI technologies and design enablement advancements with specific SiGe examples which demonstrate the world's most highly integrated, lowest-power 60-GHz transmitter/receiver ICs and highest-frequency silicon circuits.

4.2: **Mixed-Signal SiGe Radar-on-a-Chip** **(1:50)**

M. Lucas, H. Ball, C. Marcelli, H. Fudem
Northrop Grumman, Baltimore, MD

Recent results on the DARPA-sponsored TEAM Program will be described. SiGe mixed-signal technology and design methods have enabled monolithic multiple-band receiver/digital beamformer chips targeted for advanced radar systems. Northrop Grumman has used the Jazz Semiconductor SiGe BiCMOS process to fabricate and demonstrate a radar-on-a-chip, containing an LNA, mixer, A/D converter, and digital filter/beamformer completely onto a single ASIC.

4.3: **SiGe Technology Application to Wideband Electronic-Warfare Systems** **(2:10)**

F. Stroili, R. Elder, T. Keegan, R. Chan
BAE Systems, Nashua, NH

The work of BAE Systems on the DARPA TEAM program will be described. The program concluded with a demonstration of two IBM SiGe chips implementing a wideband electronic-warfare receiver function. A custom rf IC and high-speed ADC are integrated with an FPGA into a compact receiver module.

4.4: **Novel Silicon Transistors for High-Performance Mixed-Mode Systems** **(2:30)**

J. Woo
UCLA, Los Angeles, California

The challenges of deeply scaled CMOS for rf/mixed-mode applications will be reviewed. Several novel transistor structures with excellent analog/rf characteristics will be proposed. Advanced passives made feasible by the multi-level backend interconnect of advanced CMOS will also be discussed.

BREAK **(3:00)**

Session 5

NANOTECHNOLOGY FOR SYSTEMS II

Tuesday, March 20 / 3:30 – 5:00 pm / Coronado J

Chair: **Joe E Brewer**
University of Florida, Melrose, FL
Co-Chair: **Cliff Lau**
Institute for Defense Analyses, Alexandria, VA

5.1: **Nanoscale Device Failure Mechanisms and the Reliability of Logic Circuits** **(3:30)**

E. Taylor, J. Fortes
University of Florida, Gainesville, FL

Recent work on transistor failure mechanisms in emerging silicon and other nanoscale technologies in order to confirm the validity of the fault types used in previously proposed reliability models will be examined. How many of the failure mechanisms of devices can be captured in a reliability model and how it can potentially be used in the design and manufacturing of circuits will be discussed.

5.2: **Bench-Top Circuit Fabrication and Repair with Thermal Dip-Pen Nanolithography** **(3:50)**

P. E. Sheehan, L. J. Whitman
Naval Research Laboratory, Washington, DC

W. P. King
Georgia Institute of Technology, Atlanta, GA

In thermal Dip Pen Nanolithography (tDPN), a heated atomic-force microscope cantilever controls the deposition of a solid ink, acting like a nanoscale glue gun or soldering iron. tDPN can be used to deposit a range of materials that are immobile at room temperature (without solvents) – from semiconductors to insulators to metals, in both ambient and UHV environments – offering the potential for bench-top circuit fabrication and repair.

5.3: **Nanostructured Perovskite Thin Films for Tunable RF Applications** **(4:10)**

D. P. Norton, C. Callender
University of Florida, Gainesville, FL

The manipulation of ferro-functional oxides, namely, perovskites, in designing novel materials for tunable RF electronics will be reported. In particular, the synthesis of superlattice structures utilizing lattice-matched solid solutions of $K(Ta,Nb)O_3$ and $(Ba,Sr)FeO_3$, is being investigated.

5.4: **Nanotechnology for Miniaturized Electronic Systems** **(4:30)**

A. Biswas, P. C. Karulkar
University of Alaska Fairbanks, Fairbanks, Alaska

Novel inorganic–organic hybrid nanomaterials for a number of advanced electronic applications, such as high-performance integrated electronics, energy conversion and storage, EM shielding, and a number of novel device applications, will be discussed. Advances in materials synthesis for nanoelectronics will be described.

Session 6

ELECTRONICALLY STEERABLE ARRAYS

Tuesday, March 20 / 3:30 – 5:00 pm / Coronado Q&R

Chair: **Eric D. Adler**
Army Research Laboratory, Adelphi, MD
Co-Chair: **William D. Palmer**
U.S. Army Research Office, Durham, NC

6.1: **Next-Generation Multi-Function Radar for the Class IV UAV Affordable, Adaptive Conformal Electronically Scanned Antenna (ESA) Radar (AACER)** **(3:30)**

R. Robertson, C. Engels, R. T. Lewis, R. T. Kihm, K. Krikorian, Y. Kwong, R. Rosen, M. Pines, C Luo
Raytheon Space and Airborne Systems, El Segundo, CA

D. W. Baker, K. Kaneko-Baker
Raytheon Missile Systems,Tucson, AZ

B. Tousley, T. McClure, D. Giglio, J. Smith
DARPA, Arlington, VA

E. Adler
Army Research Laboratory, Adelphi, MD

The DARPA AACER Program is a joint effort between DARPA, the Army Research Laboratory, and Raytheon to develop a light-weight and low-cost multifunction radar for the Class IV Army Unmanned Aerial Vehicle (UAV). Unlike federated systems, which require separate apertures and subsystems for each function, AACER is multifunctional. AACER implements ultra-high-range-resolution SAR, very-slow-speed GMTI for dismount detection, Geolocation, Data Link, Communications, and Cooperative Combat Identification (CID) in one system with a common set of hardware. This revolutionary new multifunction radar at both the system and subsystem levels will be discussed.

6.2: **Batch-Fabricated Scalable Millimeter-Wave Electronically Steered Array Transceivers** **(3:50)**

J. Hacker, J. Denatale, C-L. Chen, C. Hillman
Rockwell Scientific Co., Thousand Oaks, CA

A 44-GHz transceiver array architecture that integrates all required functionality, from silicon digital beam control and rf beam-forming electronics to InP ultra-high-power amplifiers and sensitive receivers, with wide-scan apertures, into a compact, rugged, micromachined three-dimensional structure will be reported.

6.3: **Integrated Micro-Coaxial Ka-Band Antenna and Array** **(4:10)**

D. Filipovic, K. Vanhille, M. Lukic
University of Colorado, Boulder, CO

D. Fontaine
BAE Systems, Nashua, NH

A Ka-band antenna element, array routing, 16 × 16 Butler matrix beamformer, and interconnect to the active control will be demonstrated. The results of this research clearly pave the path for the integration of various three-dimensional micro-electromagnetic radio-frequency systems in FCS.

6.4: Development of Simple Affordable Beamformers for Army Platforms (4:30)

S. Weiss, S. Keller
Army Research Laboratory, Adelphi, MD

Affordable electronic scanning arrays (ESAs) have long been a desirable technology for Army requirements, such as Satellite on the Move (SOTM) and Communications on the Move (COTM). One way to fabricate an electronically scanned array is to use commercial-off-the-shelf (COTS) phase shifters. For COTM C-band systems, these shifters tend to have insertion losses on the order of 3 or 4 dB and they require a shifter for each element of the array – increasing the complexity (and cost) of the design. For SOTM (generally at X, Ku, or Ka bands) the insertion losses become higher.

Session 7

HIGH-PERFORMANCE INTEGRATED ELECTRONICS: LOW POWER

Tuesday, March 20 / 3:30 – 5:00 pm / Coronado S&T

Chair: **Michael Fritze**
DARPA/MTO, Arlington, VA

7.1: **A Parallel Energy-Efficient 100-Mbps Ultra-Wideband Radio Baseband** **(3:30)**

B. P. Ginsburg, V. Sze, A. P. Chandrakasan
MIT, Cambridge, MA

An analog-to-digital converter (ADC) and a digital baseband processor for an ultra-wideband (UWB) radio receiver perform sampling and demodulation of 100-Mbps UWB pulses has been developed. Parallelism is used to achieve the high throughput with state-of-the-art power consumption. The 5-bit 500-MS/sec ADC consumes only 6 mW, and the digital processor operates at 0.4 V.

7.2: **Ultra-Low-Power Logic Design Using Subthreshold Operations** **(3:50)**

A. Raychowdhury, K. Roy
Purdue University, West Lafayette, IN

A novel design methodology for ultra-low-power design (in bulk and double-gate SOI technology) using subthreshold leakage as the operating current (suitable for medium frequency of operation: tens to hundreds of MHz) will be presented.

7.3: **Ultra-Low-Power Electronics: Design Observations and CULPRiT Experiences** **(4:10)**

S. Whitaker, P. Winterrowd, R. Nelson
University of Idaho, Post Falls, ID

P-S. Yeh,
NASA GSFC, Greenbelt, MD

Ultra-low-power (ULP) electronics has applications in numerous applications that range from space to handheld units. An ULP program that (a) has successfully flown on a NASA mission, (b) possesses unique abilities in an ultra-low-temperature (ULT) environments, and (c) has a program to implement a ULP deep submicron process will be described.

7.4: **Analysis of Energy-Starved Electronics-Power-Savings Opportunities in Software-Defined Radios** **(4:30)**

B. Fette
General Dynamics C4 Systems, Scottsdale, AZ

Power consumption is an extremely important consideration of handheld electronics. Software-defined radios (SDRs) are an extremely important part of the handheld electronics complement of the soldiers of the future, and several SDR radios are in development under the JTRS program. Power analysis of each subsystem in an SDR allows us to focus attention on minimizing power throughout the hardware and software architecture. By focusing on power, the size and weight of batteries that must be carried by the soldier can be significantly improved. Power-savings opportunities identified by this study will be described.

WEDNESDAY, 21 MARCH

Session 8

TRUSTED FOUNDRY UPDATE

Wednesday, March 21 / 8:30 – 10:00 am / Durango 1&2

Chair: **Charlie Meyer**
DoD, Fort George G. Meade, MD
Co-Chair: **Sonny Maynard**
ODUSD(S&T), Washington, DC

8.1: **Trusted Integrated-Circuit Policy** **(8:30)**

S. Pope
DoD, Washington, DC

Microelectronics is dominated by global commercial interests, making DoD issues of trust, obsolescence, and product assurance increasingly difficult to manage. Partnerships with industry offer a significant opportunity to address these issues by identifying areas of common interest and enabling industry to partner in developing solutions.

8.2: **Trusted Foundry Update: IBM's Offerings through TAPO** **(8:50)**

M. Kerbaugh, E. Hall, B. Salimi, J. Turvey
IBM, Essex Junction, VT

IBM continues to press the envelope of innovation and collaboration, and, as a result, offerings available through TAPO have been updated. An overview of ASIC and foundry offerings, including the latest status on 90- and 200-mm trusted manufacturing, will be provided. The technology highlights and characteristics, technology development and qualification status, and the status of the 65-nm ASIC offering, Cu-65, will be described. Plans for library and IP development for both performance-oriented bulk technology and low-power technology in both ASIC and foundry models will be discussed.

8.3: **Efficient Design and Access to a Leading-Edge Trusted Foundry** **(9:10)**

D. J. Radack
Institute for Defense Analyses, Alexandria, VA

High-performance / low-power circuit designers using best-practice leading-edge semiconductor foundries are under enormous pressure to achieve first-pass success. Models and methodologies for attaining leading-edge design capabilities with small teams will be reported. The highlights of the First Trusted Foundry Circuit Designers Meeting will also be presented.

8.4: **Accrediting Additional Trusted Suppliers and Assuring Trusted IC Availability** **(9:30)**

D. Pentrack
DMEA, McClellan, CA

Efforts to expand the trusted supplier base, to develop criteria for additional levels of trust, and to provide trusted fabrication capabilities at DMEA to assure the long-term availability of trusted ICs, will be described.

BREAK **(10:00)**

Session 9

WIDE-BAND-GAP OXIDES

Wednesday, March 21 / 8:30 – 10:00 am / Coronado Q&R

Chair: **Michael D. Gerhold**
U.S. Army Research Office Research, Triangle Park, NC
Co-Chair: **Paul H. Shen**
Army Research Laboratory, Adelphi, MD

9.1: **Ultraviolet Emission of ZnO-Based Light-Emitting Diodes** **(8:30)**

M. Pan, J. Nause
Cermet, Inc., Atlanta, GA

Efficient p-type doping of ZnO was performed to achieve UV lighting. Nitrogen and phosphorus were in-situ doped into ZnO epilayers by MOCVD. Dopant concentrations were in the range of 10^{18} cm^{-3}. Doped ZnO demonstrated p-type behavior. PL and EL of UV emissions were detected at 380 and 384 nm, respectively.

9.2: **ZnO-Based Band-Gap Engineering and UV-to-Visible Light Emitters** **(8:50)**

A. V. Osinsky, J. W. Dong, B. Hertog, P. P. Chow
SVT Associates, Inc., Eden Prairie, MN

Band-gap engineering of ZnO-based materials will be discussed. Single-crystal $Mg_xZn_{1-x}O$ and $Cd_xZn_{1-x}O$ films and quantum wells were grown by rf-plasma-assisted MBE. Strong visible emission in the 400–580-mn spectral range was observed at room temperture. The complex index of refraction for CdZnO was determined as a function of wavelength in the range 300–800 nm. The index of refraction for $Cd_{0.16}Zn_{0.84}O$ varies between 2.02 and 2.26.

9.3: **Development of ZnO Technology for UV/visible LED Applications** **(9:10)**

J. Zhang, G. Cantwell, C. K. Choi, J. J. Song
ZN Technology, Inc., Brea, CA

Recent progress made in the ZnO program will be presented, including high-quality ZnO substrates with the x-ray rocking-curve FWHM as small as 22 arc-sec; 2D ZnO homoepitaxial films and high-quality ZnMgO/ZnO quantum-well structures grown by MOCVD; high-quality MOCVD-grown ZnO nanotips; and nanotip LED applications.

9.4: **Present Status of ZnO Materials and Devices** **(9:30)**

D. Look
Wright State University, Dayton, OH

ZnO is a material rapidly becoming of age in the areas of photonics and electronics, and it has many advantages over its chief rival, GaN. The status of bulk and epitaxial growth and devices, such as UV LEDs and transparent transistors, will be described.

BREAK **(10:00)**

Session 10

60–600-GHZ NOVEL RF SOURCE TECHNOLOGIES

Wednesday, March 21 / 8:30 – 10:00 am / Coronado S&T

Chair: **Steven C. Binari**
Naval Research Laboratory, Washington, D.C.
Co-Chair: **Mark Rosker**
DARPA/MTO, Arlington, VA

10.1: Development of a 600–675-GHz Source for TIFT (8:30)

K. Kreischer, J. Tucek, D. Gallagher, R. Vogel
Northrop-Grumman Corp., Rolling Meadows, IL

A vacuum electronic oscillator has been successfully operated between 600 and 675 GHz. RF powers up to 16 mW were measured at the output window. The folded waveguide resonant circuit in this compact source was fabricated using DRIE technology. Operation at duty cycles up to 1% was demonstrated.

10.2: High-Frequency MMW and Sub-Millimeter-Wave MMIC Amplifiers for Next-Generation RF Electronics (8:50)

R. Lai, W. Deal, P. P. Huang, X-B. Mei
Northrop Grumman Corp., Redondo Beach, CA

Future imaging, radar, and communications systems will extend the need for higher-frequency devices and circuits beyond current capability and concepts. The latest advancements of HEMT MMIC technology that have led to amplifiers from 100 to beyond 300 GHz with unprecedented performance capabilities will be described. Also, for the first time, gain amplification has been in the sub-MMW frequency domain above 300 GHz, opening a new frontier of sub-MMW MMIC (SMMIC) amplifiers.

10.3: Advanced Millimeter-Wave /Sub-Millimeter-Wave Device Development (9:10)

P. M. Smith, P. C. Chao, J. J. Komiak, D. Xu
BAE Systems, Nashua, NH

Development of sub-0.1-µm gate-length high-electron-mobility transistor (HEMT) technology for applications at frequencies above 60 GHz will be described. Two different technologies will be presented: PHEMT, a mature technology already implemented on 6-in. wafers at BAE Systems and capable of power amplification at frequencies up to 150 GHz, and MHEMT, a higher-performance technology based on high-indium InGaAs/InAs channels that promises operating frequencies up to several-hundred GHz.

10.4: New Vistas for Micro-Fabricated Slow-Wave Devices **(9:30)**

B. Levush, J. P. Calame
Naval Research Laboratory, Washington, DC

T. M. Antonsen, Jr.
University of Maryland, College Park, MD

K-T. Nguyen
Beam Wave Research, Inc., Bethesda, MD

RF power at 100 W (CW) at frequencies of 200 GHz is believed attainable from micro-fabricated vacuum-electronic slow-wave devices using spatially distributed electron beams. Relevant micro-fabrication techniques are evaluated for applicability to sheet and multiple-sheet electron-beam formation and transport, beam-wave interaction, and beam collection for several oscillators and amplifiers. RF power at 100 W (CW) at frequencies at 200 GHz is believed attainable from micro-fabricated vacuum-electronic slow-wave devices using spatially distributed electron beams. Relevant micro-fabrication techniques are evaluated for applicability to sheet and multiple-sheet electron-beam formation and transport, beam-wave interaction, and beam collection for several oscillators and amplifiers.

BREAK **(10:00)**

Session 11

TRUSTED ELECTRONICS RESEARCH

Wednesday, March 21 / 10:30 am –12:00 pm / Durango 1&2

Chair: **Dean R. Collins**
DARPA/MTO, Arlington, VA
Co-Chair: **Ray A. Price**
Department of Defense, Fort George G. Meade, MD

11.1: TRUST for Integrated Circuits **(10:30)**

D. Collins
DARPA, Arlington, VA

Because of global economic pressures, fabrication of advanced ICs is migrating to foreign foundries, and business models are increasingly driven by commercial, rather than military, demand. A new DARPA initiative is being considered to address these issues.

11.2: Metrics for Trusted Integrated Circuits **(10:50)**

D. P. Wilt, R. C. Meitzler
John Hopkins University, Applied Physics Laboratory, Laurel, MD

Quantitative metric techniques to evaluate Trusted IC technologies will be reported. Adoption of a detector-based approach to individual technology metrics allows the use of probabilistic data fusion methods for evaluation of overall technology performance.

11.3: Physical Unclonable Functions and Applications to Device Authentication **(11:10)**

S. Devadas, T. Ziola
MIT, Cambridge, MA

E. Suh
PUFCO, Menlo Park, CA

Physical unclonable functions (PUFs) are innovative circuit primitives that extract secrets from complex physical characteristics of integrated circuits (ICs). PUF designs that exploit inherent delay characteristics of wires and transistors that differ from chip to chip will be presented, and how PUFs can be used to authenticate individual integrated circuits and field-programmable gate arrays will be examined.

11.4: IC Fingerprinting and Stable IC Sensors for Enhanced IC Trust **(11:30)**

K. Nowka, G. Carpenter, P. Rohatgi
IBM Corp., Austin, TX

D. Agrawal
IBM Corp., Hawthorne, NY

Nondestructive analysis of side-channel signal perturbations can be used to detect Trojans in ICs. Simulated power signatures have identified Trojans in benchmark circuits. On-die sensors were evaluated for application to Trojan detection and tamper detection.

LUNCH **(12:00)**

Session 12

WIDE-BAND-GAP RF SEMICONDUCTORS

Wednesday, March 21 / 10:30 am – 12:00 pm / Coronado Q&R

Chair: **Glen David Via**
AFRL/SNDD, Wright-Patterson AFB, OH
Co-Chair: **Harry B. Dietrich**
Naval Research Laboratory, Washington, DC

12.1: DARPA WBGS-RF Program Reliability Status (10:30)

S. C. Binari
Naval Research Laboratory, Washington, DC

G. D. Via, J. A. Roussos, J. A. Mittereder
Air Force Research Laboratory, Wright-Patterson AFB, OH

A summary of RF life-test results obtained from recent deliverables from the DARPA Wide-Bandgap Semiconductors for RF Applications (WBGS-RF) program will be presented. The testing methodology for the evaluation of the electrical performance and reliability of AlGaN/GaN HEMTs will be reviewed.

12.2: GaN HEMT and Wideband Power Module Development (10:50)

A. Balistreri, C. Lee, P. Saunier
TriQuint Semiconductor, Richardson, TX

P. C. Chao
BAE Systems, Nashua, NH

TriQuint Semiconductor and its partners, BAE Systems, Lockheed Martin, IQE, II-VI, Nitronex, MIT, and RPI, are developing gallium-nitride devices suitable for wide-band applications for the DARPA Wide-Bandgap Semiconductor Technology RF thrust. The goals of the program are to produce reliable, reproducible high-performance devices and demonstrate capabilities through a 100-W 2–20-GHz module. The program encompasses continued improvement in material capabilities, development of device structures and process techniques, design and fabrication of MMICs, and thermal and mechanical design of high-power combiners and modules. The progress toward the program milestones and improvements made in performance and reliability of AlGaN/GaN HEMT devices will be discussed. This program, covering both Phase II and III, is supported by DARPA and the Army Research Laboratory.

12.3: GaN HEMT Technology for High-Performance PA and LNA Applications (11:10)

M. Wojtowicz, R. Coffie, I. Smorchkova, B. Heying
Northrop Grumman Corp., Redondo Beach, CA

Improvements in GaN HEMT technology for power amplifiers (PAs) and low-noise amplifiers (LNAs) for microwave and millimeter applications will be described. Through GaN HEMT device profile, topology, and process optimization, state-of-the-art power and low-noise performance at various frequencies have been demonstrated. Excellent long-term reliability has also been observed from our GaN HEMT LNA MMICs.

12.4: Raytheon–Cree Team DARPA WBGS Phase 2 Program Status **(11:30)**

J. Smolko
Raytheon Co., Tewksbury, MA

J. Milligan, S. Allen
Cree, Inc., Durham, NC

S. Brieley
Raytheon Co., Andover, MA

The Raytheon-Cree WBGS is accelerating the pace of GaN technology development to align with military and commercial system needs and to reduce insertion risk. Close coordination and open sharing between the two foundries eliminates duplication of development effort and reduces risk against technical hurdles. Progress on the WBGS program since its inception is presented.

LUNCH **(12:00)**

Session 13

MICROELECTRONIC TECHNOLOGIES FOR PROGNOSTICS AND DIAGNOSTICS

Wednesday, March 21 / 10:30 – 11:40 am / Coronado S&T

Chair: **Romeo D. del Rosario, Jr.**
Army Research Laboratory, Adelphi, MD
Co-Chair: **Eric D. Adler**
Army Research Laboratory, Adelphi, MD

13.1: **Withdrawn**

13.2: **Electronic Prognostics: Engineering Capability** **(10:30)**

P. W. Kalgren, R. Brewer, M. J. Roemer
Impact Technologies, LLC, Rochester, NY

P. Dussault
U.S. Army AMRDEC, Huntsville, AL

Research has indicated that physics-based modeling, signal and condition monitoring, and usage monitoring all exhibit promise in predicting failures of electronic systems. A new usage that integrates all three approaches, resulting from a study of an electronic-weapons system currently in use on the AH-64D Apache Attack Helicopter, will be described.

13.3: **A Leveraged Sampling Technique for Learning Diagnostic and Prognostic Models from Small Data Sets** **(10:50)**

P. L. Dussault
U.S. Army RDECOM, Redstone Arsenal, AL

J. W. Sheppard, S, G. W. Butcher
The Johns Hopkins University, Baltimore, MD

Modern weapons systems continue to be plagued by high cannot duplicate and retest OK rates. A new sampling method, called “leveraged sampling,” for generating additional examples from small data sets by considering raw test measurements and test tolerances to determine the sampling distribution for each test will be described.

13.4: SiP Wireless Micro-Power Sensors **(11:10)**

J. P. Vogt, M. Chen
Georgia Tech Analog and Power IC Lab, Atlanta, GA

The demands of SiP wireless sensors that can operate for long periods of time and in any environment require an in-package energy supply that delivers needed power for a number of power modes. A hybrid supply of a Li-ion battery and micro-fuel-cells can match such usage, but a long life demands micro-power solutions to sensors and telemetry. Transistor- and capacitor-based sensors show the most promise for realizing such systems. Constant envelope OOK or BFSK modulation allows high-efficiency amplifiers to be used, freeing up more power for the oscillator, which, using in-package high-Q inductors, can operate at lower power levels than on-chip inductors for a given performance.

LUNCH **(12:00)**

Session 14

TRUSTED ELECTRONICS

Wednesday, March 21 / 1:30 – 3:10 pm / Durango 1&2

Chair: **Gerry Etzold**
Department of Defense, Fort George G. Meade, MD
Co-Chair: **Sonny Maynard**
ODUSD(S&T), Washington, DC

14.1: **The Role of a Multi-Project Wafer (MPW) Aggregator in Tracking Critical Process Parameters at Multiple Foundry Fabrication Facilities: The use of Specialized Process Monitors to Detect Anomalous Deviations in Critical Process Parameters** **(1:30)**

R. Parker
USC Information Sciences Institute, Arlington, VA

V. C. Tyree, Z. Sparling
USC Information Sciences Institute, Marina del Rey, CA

A MPW aggregator is in an ideal position to monitor critical process parameters in semiconductor manufacturing (*e.g.*, on CMOS and CMOS/SiGe technologies) to assure that process parameters that are critical to DoD applications are not changing in an anomalous manner. The data from an inserted process monitor serves to enhance data already available from the foundry kerf data and to provide additional parametric data not included in the foundry kerf data that is of special interest to DoD ASIC designs. Process monitor data considered to be most critical is trend charted to provide a visual history of the foundry performance in a particular technology and serves to build confidence in process stability.

14.2: **Multi-Project Wafer Approach: Maximizing Value, Flexibility, and Customer Service** **(1:50)**

D. Brown, P. Tapp, J. Meinhardt, J. McCord
Kansas City Plant, Kansas City, MO

Process improvements have maximized the program's value. Customer guidance and improved communication has decreased cycle time while consistently meeting or exceeding customer requirements. New tools have allowed us to increase customers served while decreasing program costs. Alternate sources were exercised for aggregation, dicing, testing, and packaging to reduce risks.

14.3: **Trusted Products and Capabilities Available from National Semiconductor** **(2:10)**

J. Monk, T. Bent, D. Ossman, C. Varney
National Semiconductor Corp., Annapolis Junction, MD

National Semiconductor is a domestic leader in high-performance analog products. With the clearing of National's South Portland, Maine, foundry, they can now offer mixed signal products and trusted ASICs for the most-sensitive U.S. Government defense systems.

14.4: BAE Systems Trusted Foundry Status and Plans (2:30)

L. Rockett, S. Danziger
BAE Systems, Manassas, VA

BAE Systems in Manassas, Virginia, is pursuing designation as a Trusted Foundry; has been developing and producing radiation-hardened technologies and products for over 25 years; has been a leader in supplying ASIC design services, technologies, components, and processor products supporting DoD needs; and is certified for DoD classified work.

14.5: *Late-News Paper:* An Advanced Trusted Foundry for Accelerating Application of Microelectronics Technology into DoD Electronic Systems (2:50)

D. Wick and G. Panning
Honeywell Solid State Electronics Center, Plymouth, MN

Under the sponsorship of the Defense Threat Reduction Agency (DTRA), Honeywell has developed, and has available for use today, a 150-nm silicon-on-insulator (SOI) CMOS wafer process and microelectronic product set, manufactured in a secure and DoD Class 1 accredited Trusted Foundry that will accelerate the application of advanced microelectronic technology in new or upgraded DoD electronic systems.

BREAK (3:10)

Session 15

POWER ELECTRONICS I

Wednesday , March 21 / 1:30 – 3:00 pm / Coronado Q&R

Chair: **Fritz Kub**
Naval Research Laboratory, Washington , DC
Co-Chair: **Allen Hefner**
NIST Gaithersburg, MD

15.1: **Status of DARPA WBST High-Power Electronics Program in SiC Device Development and Technology Transition** **(1:30)**

A. Hefner
NIST, Gaithersburg, MD

S. Beermann-Curtin
DARPA/DSO, Arlington, VA

The emergence of high-voltage high-frequency (HV-HF) silicon-carbide (SiC) power devices is expected to revolutionize commercial and military power distribution and conversion systems. The DARPA Wide-Bandgap Semiconductor Technology (WBST) High-Power Electronics (HPE) program is spearheading the development of HV-HF SiC power semiconductor technology. Recent progress made in HPE device development will be discussed and new efforts to establish reliability and manufacturability of the devices will be described.

15.2: **SiC Devices for High-Power Applications** **(1:50)**

A. Hefner
NIST, Gaithersburg, MD

S. Beermann-Curtin
DARPA/DSO, Arlington, VA

D. Grider
Cree, Inc., Durham, NC

Because of the higher breakdown fields and operating temperatures inherent in SiC devices, this technology offers significant advantages for power applications from 600 V to 10 kV. Recent crucial developments in SiC DMOSFET, BJT, IGBT, PiN, and JBS diode power device technologies and their impact on power applications will be reviewed.

15.3: **Carbide JBS Diodes for Advanced Power Systems at 13.8 kV** **(2:10)**

S. Van Campen, A. Walker, T. McNutt, K. Ha
Northrop Grumman Electronic Systems, Linthicum, MD

A junction-barrier Schottky (JBS) diode was designed, fabricated, and tested to a a breakdown voltage of 10 kV. This JBS diode offers low reverse recovery current in power-conversion circuits.

15.4: SiC Vertical-Junction Field-Effect Transistors: Processing, Testing, Yields, and Applications **(2:30)**

V. Veliadis, T. McNutt, E. Stewart, M. McCoy
Northrop Grumman Electronic Systems, Linthicum, MD

Ion-implanted vertical-junction field-effect transistors (VJFETs) have been manufactured on silicon-carbide wafers with high yields and excellent performance parameter uniformity. VJFETs were connected in the cascode configuration to form all-SiC normally off switches. A cascade-based half-bridge inverter was successfully operated.

BREAK **(3:00)**

Session 16

TECHNOLOGIES FOR SENSOR C-SWAP REDUCTION

Wednesday, March 21 / 1:30 – 3:00 pm / Coronado S&T

Chair: **Bradley Paul**
AFRL/SNDI, Wright-Patterson AFB, OH
Co-Chair: **Christopher D. Lesniak**
AFRL, Wright-Patterson AFB, OH

16.1: **High-Frequency C-SWAP Plastic Packages for Space Applications** **(1:30)**

R. A. Anderson, N. Kinayman, J-P. Lanteri
M/A-COM, Lowell, MA

Results extending the application of C-SWAP to x-band and 24 GHz will be reported. C-SWAP packages have been modeled, produced, and tested at these frequencies. RF performance is comparable to hermetic packages. Reliability tests show parts exceed NASA and military space-based reliability and outgassing requirements. Exploration of flip-chip packages designed to handle high-power devices and new materials such as LCP with dramatically improved moisture resistance will also discussed.

16.2: **Wideband Passive Amplitude-Compensated True-Time-Delay (TTD) Module for Active Phased Arrays** **(1:50)**

J. Iannotti
GE Global Research Center, Niskayuna, NY

C. Kapusta, W. J. Taft, A. Jacomb-Hood
LM CSS, Newtown, PA

The TTD is a critical function for active phased arrays which require wide instantaneous bandwidth and large scan angles. A major challenge associated with TTDs is providing equal insertion loss between states over a wide instantaneous frequency band. A solution to this problem for long-delay (1.0+ nsec) TTDs utilizing chip-on-flex (COF) high-density interconnect packaging will be described. This approach is compatible with semiconductor-based switches and other low-loss RF switch technologies such as RF MEMS.

16.3: **X-Band Receiver Front-End Components in Silicon Technology** **(2:10)**

T. Quach
AFRL/SND, Dayton, OH

P. Wyatt
MIT Lincoln Laboratory, Lexington, MA

The demonstration of receiver rf front-end components using fully depleted silicon-on-insulator CMOS technology will be reported. The system architecture is a single down-conversion operating from X- to S-band.

16.4: Wide-Band Plastic Packaged Highly Integrated TDU MMIC with Variable Time Delay (2:30)

R. Anderson, G. Clark, J. Dishong
M/A-COM, Lowell, MA

S. Anderson
REMEC D&S, Richardson, TX

A plastic packaged highly integrated transmit–receive MMIC has been designed for AFRL radar applications, offering variable time delay and low dc power dissipation. The time-delay "TDU" T/R MMIC offers a total time delay for six time-delay bits of 1.008 nsec, twice that of previous time-delay MMICs; in addition to a 5-bit 31-dB attenuator, six buffer amplifier gain stages, four T/R switches, and two drain bias switches, all integrated into a single MMIC.

BREAK (3:00)

Session 17

THROUGH-THE-WALL SENSING

Wednesday, March 21 / 3:30 – 5:00 pm / Durango 1&2

Chair: **Deepak Varshneya**
DARPA/STO, Arlington, VA
Co-Chair: **Kathleen A. Griggs**
Puritan Research Corp., Vienna, VA

17.1: Radar Applications in Urban Sensing (3:30)

E. J. Baranoski
DARPA/STO, Arlington, VA

Radar offers unique capabilities for addressing many urban-sensing challenges. The DARPA programs ranging from sensing through walls (Radar Scope and VisiBuilding) to future efforts on target tracking through urban canyons will be described.

17.2: Through-the-Wall Target Detection and Identification Using Impulse SAR (3:50)

J. Tatoian, G. Franceschetti
Eureka Aerospace, Pasadena, CA

G. Gibbs
MARCORSYSCOM, Quantico, VA

H. Lackner
E&TS, Oakland, CA

Prototype Impulse SAR operating in a transient regime is capable of through-the-wall imaging of targets. The proposed ImpSAR radiates carrierless short (~100 psec) impulse waveforms, whose bandwidth spans 350–3000 MHz, is well suited for wall penetration, and yields exceptionally high (centimeters) resolution. The system is potentially deployable in a UAV- or helicopter-based operational system.

17.3: Through-the-Wall Sensing Based on a Compact Lobster-Eye X-Ray Imager (4:10)

K. Shoemaker, M. Gertsenshteyn, T. Jannson, G. Savant, V. Grubsky
Physical Optics Corp., Torrance, CA

A novel compact through-the-wall sensor based on Physical Optics Corp.'s Lobster-Eye hard x-ray focusing lens will be discussed. The new non-scanning Lobster-Eye x-ray backscattering technology is especially suited to identifying the presence of threats in real time and enabling rapid action to nullify them. This is possible because a new x-ray lens replaces the standard scanning optics, making possible not only the use of low-efficiency Compton backscattering but also operation in real time, with low-flux x-ray beams and increasing operator safety; it also results in an extremely efficient power budget. The Lobster-Eye lens, consisting of square-cross-section microchannels, transmits an x-ray beam by total external reflection. The proposed system is compact, can be man-portable or deployed on a small, remotely operated vehicle (ROV) or a man-operated vehicle, and preserves high-quality imaging parameters so it can detect concealed improvised explosives or the presence of terrorists, even through metal walls.

17.4: Platform Stabilization for Detection of Respiration for Through-the-Wall Radars (4:30)

K. Shoemaker, M. Gertsenshteyn, T. Jannson, G. Savant, V. Grubsky
Physical Optics Corp., Torrance, CA

J. V. Richard, L. D. Elam
SAIC, San Diego, CA

The typical breathing signature of a person has a displacement of 0.5–1 cm at 0.25 Hz. Soldier-mounted, wheeled vehicles, and airborne platforms move considerably greater distances then 1 cm every 4 sec. Therefore, motion compensation is required to detect a stationary person. The requirements necessary to detect respiration of a stationary person from a platform will be described.

Session 18

POWER ELECTRONICS II

Wednesday, March 21 / 3:30 – 5:00 pm / Coronado Q&R

Chair: **Allen Hefner**
NIST Gaithersburg, MD
Co-Chair: **Fritz Kub**
Naval Research Laboratory Washington , DC

18.1: **Rugged UHF 4H-SiC BJTs with Record 22.8 W/mm Power Density and 8.3-dB Gain at 500 MHz** **(3:30)**

F. Zhao, I-P. Wurfl, K. Torvik
Microsemi, PPG ATC, Boulder, CO

J. Chiu
Microsemi, PPG RF, Santa Clara, CA

4H-SiC BJTs are promising candidates for applications such as radar, avionics, and network-centric communications due to their ability to handle higher bias voltage and power density compared to their silicon counterparts. Devices with an emitter finger length of 1.8 mm that exhibit 41 W of output power at 500 MHz with a power density of 22.8 W/mm and 8.3 dB gain when operated in pulsed class AB mode with a pulse width of 150 msec and a duty cycle of 5% will be reported. This power density is, to the authors' best knowledge, the highest ever published to date for SiC bipolar transistors.

18.2: **Using AMSC PEBBs to Accelerate New Technology Development** **(3:50)**

P. Schugart
American Superconductor, New Berlin, WI

New technology development is analogous to solving an ever-shifting multivariable problem that has more variables than equations. The more aggressive the advance in technology is, the more unknowns are present. Using AMSC PEBB technology to reduce the amount of unknown variables provides focus on the key technology unknowns and accelerates the development process.

18.3: **Power-Dense Bi-Directional DC-DC Converter Development** **(4:10)**

D. P. Urciuoli
U.S. Army Research Laboratory, Adelphi, MD

The dc-dc converter slated to provide bi-directional power flow between the battery pack and the propulsion bus in the future electric ground vehicle requires a power-dense design. ARL has demonstrated 90-kW performance in a bi-directional converter testbed and through converter enhancements has designed a packaged, power-dense 150-kW converter for vehicle system-integration testing.

18.4: Design and Fabrication of a High-Temperature (250ºC base plate) single-phase silicon carbide (SiC) multichip power-module (MCPM) Inverter (4:30)

E. Cilio, J. Hornberger, B. McPherson, M. Schupbach
APEI, Inc., Fayetteville, AK

A complete design strategy (mechanical and electrical) for a single-phase 3-kW power inverter utilizing SiC and SOI electronics will be presented. A prototype module capable of operating from 25ºC up to an ambient temperature of 250ºC has been built and tested. Results of high-temperature operation will be presented.

Session 19

MICROSYSTEMS FOR ENERGY HARVESTING

Wednesday, March 21 / 3:30 – 5:00 pm / Coronado S&T

Chair: **David Edward Dausch**
RTI International, Research Triangle Park, NC
Co Chair: **John Posthill**
RTI International, Research Triangle Park, NC

19.1: **Power and Energy Requirements for the Army** **(3:30)**

S. Bayne, E. Shaffer
Army Research Laboratory, Adelphi, MD

The Army is transforming and upgrading its technologies and systems to meet the changing threats. A major part of the transformation is investigating power and energy requirements for the current and future force. The areas mobile systems, solider systems, and sensors will be focused upon. In order to meet the Army's needs, power and energy systems should have higher-power and higher-energy-density components capable of operating at higher temperatures, having longer lifetimes and being more reliable.

19.2: **Assessment of Micro-Components for Energy Harvesting from Thermal Gradients, Light, and Mechanical Vibrations** **(3:50)**

J. Lewis, J. Posthill, D. Dausch, C. Watkins, M. Lee
RTI International, Research Triangle Park, NC

RTI's ultra-small-form-factor thin-film thermoelectric (TE) technology for small-thermal-gradient energy harvesting and a conceptual design for combining TE, photovoltaic (PV), and mechanical vibration (MV) energy harvesting technologies for reliably powering microsystems that can be less than 1 cc in volume will be described.

19.3: **RF Energy Recycling and Wireless Powering for Low-Power Distributed Sensors** **(4:10)**

Z. Popovic, R. Zane, T. Paing, J. Morroni
University of Colorado, Boulder, CO

Several rectenna elements and arrays for low-power applications will be discussed: (1) a 10-GHz array for powering sensors in aircraft wings; (2) a single antenna in the 2.4-GHz ISM band for low-power assisted-living sensors; and (3) a broad-band array for power harvesting in the 2–18-GHz frequency range.

19.4: **Photovoltaically Based Integrated Power Sources for Distributed Autonomous Systems** **(4:30)**

R. J. Walters, P. P. Jenkins, G. C. Gilbreath, J. L. Murphy
Naval Research Laboratory, Washington, DC

The development of energy-harvesting systems based on photovoltaics for powering-distributed autonomous systems will be presented. Details of the IR-sensitive PV-powered modulating retroreflector (MRR) for free-space self-powered optical communications will be given. Plans for developing underwater PV systems for optical power beaming and solar photon scavenging will be presented.

THURSDAY, 22 MARCH

Session 20

RAD-HARD SUB-100-nm MICROELECTRONICS TECHNOLOGY

Thursday, March 22 / 8:30 – 10:00 am / Durango 1&2

Chair: **John Franco**
Defense Threat Reduction Agency, Ft. Belvoir, VA
Co-Chair: **Captain T. A. Uhlman**
Defense Threat Reduction Agency, Ft. Belvoir, VA

20.1: Electronic-Design-Automation Challenges for Sub-100-nm Rad-Hard IC Design **(8:30)**

Z. Johnson
The Boeing Company, Seattle, WA

Under the DTRA Radiation Hardened Microelectronics program, Boeing is developing rad-hard ultra-deep submicron mixed-signal libraries for both advanced hardened and non-hardened semiconductor fabrication processes. Issues impacting electronic design automation at the <100-nm node and EDA solutions for effective design of rad-hard ICs will be discussed.

20.2: Technology Trends for Advanced SRAM-Based FPGAs **(8:50)**

R. Padovani, J. Fabula
Xilinx, San Jose, CA

SRAM-based FPGAs have reached system-on-a-chip integration levels today enabled by architectural advances and leading-edge deep submicron CMOS technology. Aggressive scaling of CMOS technology will continue and provide FPGAs with even higher system complexity and performance in the future. Application of this technology to meet the requirements of aerospace and defense systems, including reliability aspects, will be examined.

20.3: Radiation Test Challenges for Scaled CMOS Electronics **(9:10)**

K. A. LaBel
NASA/GSFC, Greenbelt, MD

As sub-100-nm CMOS technologies gather interest, the radiation-effects performance of these technologies provides a significant challenge. The radiation-testing challenges as related to commercial devices will be discussed.

20.4: Rad-Hard by Design Results in 90-nm Technology **(9:30)**

W. P. Snapp, T. Amort, M. Baze
The Boeing Co., Seattle, WA

The DARPA Radiation-Hardening–by–Design program results for hardening techniques in advanced mixed-signal processes from the trusted foundry will be presented, including radiation test results for 90-nm CMOS test chips containing a wide array of digital devices, SRAM, and IP.

BREAK **(10:00)**

Session 21

ELECTRONICS FOR EXTREME ENVIRONMENTS

Thursday, March 22 / 8:30 – 10:00 am / Coronado Q&R

Chair: **Mohammad M. Mojarradi**
Jet Propulsion Laboratory, Pasadena, CA
Co-Chair: **Elizabeth A. Kolawa**
Jet Propulsion Laboratory, Pasadena, CA

21.1: Advanced Rad-Hard Technology for Cryogenic Applications **(8:30)**

N. F. Haddad, R. Lawrence, M. Polavarapu
BAE Systems, Manassas, VA

J. Benedetto
ATK Mission Research, Colorado Springs, CO

An advanced rad-hard technology (RH15) was evaluated for application at cryogenic temperatures. Devices were very well behaved and no degradation was observed during and after 1-Mrad total-dose irradiation at 43ºK.

21.2: SOI CMOS for Extreme-Temperature Applications **(8:50)**

B. W. Ohme, B. J. Johnson
Honeywell, Plymouth, MN

A high-temperature wafer-process flow has been developed by modifying a rad-hard process flow. The resulting wafer process is optimized for an extremely wide operating temperature range, while maintaining commonality of layout rules and the overwhelming majority of manufacturing operations.

21.3: –5-V Compatible Rad-Hard SOI Rail-to-Rail Input/Output Operational Amplifier for Extreme Environments **(9:10)**

R. L. Greenwell, S. C. Terry, B. J. Blalock
University of Tennessee, Knoxville, TN

M. M. Mojarradi
Jet Propulsion Laboratory, Pasadena, CA

A 5-V compatible high-performance operational amplifier on a rad-hard 3.3-V SOI process for wide-temperature-range operation will be presented. A novel biasing scheme is used to enable –180ºC to +120ºC operation with optimal analog performance, and a methodology for reliability-by-design will be presented.

21.4: Fully Depleted SOI CMOS Technology for Extreme Environments **(9:30)**

C. L. Keast, P. Gouker, R. D'Onofrio, A. Soares
MIT Lincoln Laboratory, Lexington, MA

Fully depleted silicon-on-insulator (FDSOI) CMOS offers several performance advantages when compared to bulk CMOS for integrated-circuit applications in extreme environments. MIT-LL's FDSOI CMOS technology will be described and its electrical performance in a full range of extreme (high-temperature, low-temperature, and radiation) environments will be presented.

BREAK **(10:00)**

Session 22

HIGH-EFFICIENCY HIGH-LINEARITY RF POWER AMPLIFIERS I

Thursday, March 22 / 8:30 – 10:00 am / Coronado S&T

Chair: **Chris W. Hicks**
Naval Air Systems Command, Patuxent River, MD
Co-Chair: **Gerald M. Borsuk**
Naval Research Laboratory, Washington, DC

22.1: Wideband VHF/UHF Quadrature LINC Power-Amplifier System (8:30)

G. Hegazi, T. Chu, D. Abbey, J. Jordan
Rockwell Collins, Cedar Rapids, IA

The components of a quadrature outphasing wideband LINC power amplifier system covering 30–450 MHz will be described. The components include the GaN class D power amplifiers, the DSP responsible for the constant envelope decomposition, the high-efficiency power supplies, and the wide-band hybrid combiners. The measured results of both linearity and efficiency will be reported.

22.2: Unmatched GaN-on-Si Power Transistors for Broadband High-Efficiency Linear Power Amplifiers (8:50)

W. Nagy, R. Therrien, A. Chaudhari, C. Snow
Nitronex Corp., Raleigh, NC

A family of unmatched GaN-on-Si power transistors to be used in broadband high-efficiency linear power amplifiers has been developed. The power transistors offer 25, 50, and 90 W of saturated power and 10 dB of gain at 3 GHz. The high power density and low output capacitance offered by GaN enable the development of high-power unmatched RF power transistors to be used over octaves of bandwidth. Performance of the GaN devices over frequency and operating temperature will be presented.

22.3: High-Efficiency SSPA Development and Trade Studies for EW Applications (9:10)

J. Komiak, P. Smith, R. Actis, R. Lender
BAE Systems, Nashua, NH

Development of solid-state power amplifiers (SSPAs) for broadband electronic-warfare (EW) applications will be described. Technologies include GaAs PHEMT, high-voltage GaAs, SiC FET, GaN HEMT, SiGe HBT, and Si LDMOS with requirements for octave to multi-octave bandwidths from 100 MHz to 20 GHz at power levels greater than 25 W.

22.4: Highly Efficient and Linear Class-E SiGe Medium-Power Amplifier Design for Wireless Sensor Network Applications **(9:30)**

D. Y. C. Lie, J. Lopez
Dynamic Research Corp. (DRC), San Diego, CA

J, F. Rowland, J. D. Popp
SPAWAR System Center, San Diego, CA

The design of monolithic rf broadband Class-E SiGe power amplifiers (PAs) that are highly efficient and linear will be discussed. Load-pull measurement data on IBM 7HP SiGe power devices have been made at 900 MHz and 2.4 GHz in a chip-on-board fashion and monolithic Class-E PAs have been designed using these devices to achieve the highest power-added-efficiency (PAE) at these frequencies. It was found that high PAE can be achieved for single-stage Class-E PAs using high-breakdown SiGe transistors at ~65% (900 MHz) and ~45% (2.4 GHz), respectively. Two-stage SiGe PAs have also been designed that shows similar measured ~40% PAE at 2.4 GHz. SiGe Class-E PAs can also be successfully linearized using an open-loop envelope tracking (ET) technique. These promising results indicate the feasibility of true single-chip wireless transceivers with on-chip medium power RF PAs suitable for wireless sensor network applications.

BREAK **(10:00)**

Session 23

ENABLING TECHNOLOGIES FOR SUB-100-nm RAD-HARD MICROELECTRONICS

Thursday, March 22 / 10:30 am – 12:00 pm / Durango 1&2

Chair: **John Franco**
Defense Threat Reduction Agency, Ft. Belvoir, VA
Co-Chair: **Captain Troy A. Uhlman**
Defense Threat Reduction Agency, Ft. Belvoir, VA

23.1: **Process Technology for Rad-Hard Sub-100-nm CMOS Technologies** **(10:30)**

J. G. Ryan
CNSE, Albany, NY

H. Hughes, P. McMarr
Naval Research Center, Washington, DC

A Rad-Hard Focus Research Center has been formed at the College of Nanoscale Science and Engineering (CNSE) to develop improved processes and materials for 90-nm rad-hard device technology. The research is focused on isolation processing and new resistor and capacitor materials and structures that can be integrated into an advanced interconnect process flow. The capabilities of the research center at CNSE and the results to date will be discussed.

23.2: **Sub-100-nm Rad-Hard IC Design: Single-Event Mechanisms Impacting Modeling and Simulation for EDA** **(10:50)**

L. W. Massengill, R. A. Weller, R. A. Reed, R. D. Schrimpf
Vanderbilt University, Nashville, TN

Key emerging single-event radiation-effects mechanisms associated with sub-100-nm technologies will be discussed. Modeling challenges and techniques to support a radiation-aware design flow for EDA and hardened-library development will be presented.

23.3: **Terrestrial Single-Event Effect Characterization and Analysis** **(11:10)**

X. Zhu
Texas Instruments, Dallas, TX

Radiation-induced soft error poses a serious reliability threat to terrestrial electronic systems built in deep submicron technologies. Novel techniques used in terrestrial single-event effect characterization and analysis at accelerated conditions will be presented.

23.4: **SEE Challenges and Solutions in Sub-100-nm Technologies** **(11:30)**

P. Eaton, D. Mavis
Micro-RDC, Albuquerque, NM

As technology feature sizes decrease below 100 nm, single-event upsets, single-event transients, and multiple-bit upsets dominate the radiation response of microcircuits. Characterization, modeling, simulation, and mitigation approaches are presented to enable the single-event hardening of these technologies to radiation environments.

LUNCH **(12:00)**

Session 24

RAD-HARD ELECTRONICS FOR SPACE ENVIRONMENTS

Thursday, March 22 / 10:30 am – 12:00 pm / Coronado Q&R

Chair: **Michael D. Watson**
NASA/MSFC, Huntsville, AL
Co-Chair: **Don Frazier**
NASA Marshall Space Flight Center, Huntsville, AL

24.1: Rad-Hard Electronics for Space Environments (10:30)

M. Watson
NASA/MSFC, Huntsville, AL

The NASA Rad-Hard Electronics for Space Environments (RHESE) Program is currently advocating and developing several electronics applications for space-radiation and low-temperature space environments. RHESE has both a broad-technology-area focus and a broad-products focus. Technology areas include high-performance processors, reconfigurable computing, radiation-effects modeling, rad-hard by design approaches, rad-hard and low-temperature materials, rad-hard memory, and low-temperature microelectromechanical-system (MEMS) design. Products include field-programmable gate arrays (FPGAs), field-programmable analog arrays, processors, reconfiguration fabrics, software, and radiation-environment models.

24.2: Self-Reconfigurable Analog Array for Very-Low-Temperature Lunar Operation (10:50)

A. Stoica, D. Keymeulen, R. Zebulum, M. Mojarradi
Jet Propulsion Laboratory, Pasadena, CA

A designed self-reconfigurable analog array currently being fabricated will provide circuits operating down to –180°C for a Moon-like environment. A single programmable/reconfigurable chip will map functions currently done with multiple ASICs, reducing development and qualification time. Reconfiguration algorithms are designed to be on-chip for reconfiguration and drift compensation.

24.3: High-Performance Processors for Space Environments: A Subproject of the NASA Exploration Missions Systems Directorate – Radiation Hardened Electronics for Space Environments Technology Development Program (11:10)

G. Bolotini, E. Kolawa
Jet Propulsion Laboratory, Pasadena, CA

B. Hodson
Langley Research Center, Hampton, VA

D. Hyde
Marshall Space Flight Center, Huntsville, AL

M. Johnson
NASA/GSFC, Greenbelt, MD

Implementation of challenging Exploration Systems Missions Directorate objectives and strategies can be constrained by computing capabilities and power efficiencies. The objective of this project is to significantly advance the sustained throughput and processing efficiency of high-performance rad-hard processors, targeting the delivery of products by the end of FY11.

24.4: Si-Ge Integrated Electronics for Extreme Environments **(11:30)**

J. D. Cressler
Georgia Tech, Atlanta, GA

The development of low-power radiation-tolerant integrated SiGe BiCMOS mixed-signal electronic components for sensor/imager and control/actuator systems that can operate reliably from –180 to +120°C and under radiation exposure for applications on the lunar surface will be addressed.

LUNCH **(12:00)**

Session 25

HIGH-EFFICIENCY HIGH-LINEARITY RF POWER AMPLIFIERS II

Thursday, March 22 / 10:30 am – 12:00 pm / Coronado S&T

Chair: **Paul A. Maki**
Office of Naval Research, Arlington, VA
Co-Chair: **Chris W. Hicks**
Naval Air Systems Command, Patuxent River, MD

25.1: **High-Efficiency MMIC Amplifiers Using Advanced GaN/AlGaN HEMTs on SiC** **(10:30)**

S. Sheppard, B. Pribble, M. Willis, R. P. Smith
Cree, Inc., Durham, NC

An overview and recent results of the application of GaN HEMT devices to high-efficiency amplifiers will be presented. Previous hybrid power amplifiers exhibited 10 W CW with an associated PAE of 85% and peak CW power of 63 W and 75% PAE at 2 GHz. For more advanced work, high-efficiency monolithic amplifiers were designed, fabricated, and tested. In a MMIC format, a high-efficiency amplifier exhibited over 33 W of power (pulsed) at a peak PAE of 70% and 10 dB of associated power gain at 3.2 GHz. The MMIC amplifier exhibits high efficiency over considerable bandwidth that makes it suitable for pulsed-power radar applications, and the topology lends itself to rapid scaling to high power levels.

25.2: **High-Performance X-Band GaN MMIC Power Amplifiers with 20-W Output Power and 43% PAE** **(10:50)**

J. S. Moon, H. P. Moyer, A. Kurdoghlian, P. Macdonald
HRL Labs, Malibu, CA

Excellent small- and large-signal performances of three GaN MMIC power amplifiers covering the 6–18-GHz range will be described. The X-band GaN MMIC power amplifier offers state-of-the-art performance at an ~20-W output power level in terms of simultaneous output power, PAE, MMIC power density, NF, phase noise, and junction temperature.

25.3: **Envelope-Tracking Power Amplifier Based on DSP Techniques and Wide-Bandgap Devices Using JTRS COFDM Wide-Band Networking Waveforms** **(11:10)**

D. Kimball, P. Asbeck, C. Hsia, P. Draxler
University of California at San Diego, La Jolla, CA

A GaN HFET power amplifier using an envelope-tracking system to achieve high linearity and efficiency at 2 GHz with JTRS COFDM wideband networking waveforms will be presented. The measured PAE was >40% with DSP linearization at an average output power >20 W for a 10-MHz channel bandwidth at an 8–10-dB PAR.

25.4: Wide-Band High-Efficiency GaN Power Amplifiers Utilizing a Non-Uniform Distributed Topology (11:30)

J. Gassmann, L. Kehias, P. Watson
AFRL/SND, Wright-Patterson AFB, OH

G. Henry
Northrop Grumman Corp., Linthicum, MD

Future multifunction array platforms require efficient performance from wide-band power amplifiers. Wide-band high-efficiency non-uniform distributed GaN power amplifiers have been designed and fabricated towards this end. Results demonstrate multi-watt output power with state-of-the-art power-added efficiency over nearly a decade of bandwidth.

LUNCH (12:00)

Session 26

CRITICAL NUCLEAR-DETECTION PASSIVE SENSOR TECHNOLOGIES FOR HOMELAND SECURITY

Thursday, March 22 / 1:30 – 3:00 pm / Durango 1&2

Chair: **Bernard Phlips**
Naval Research Laboratory, Washington, DC
Co-Chair: **Michael Roberts**
Defense Threat Reduction Agency, Ft. Belvoir, VA

26.1: Defense Threat Reduction Agency Research in Nuclear-Detection Technology to Meet DoD Requirements (1:30)

J. Howell
Defense Threat Reduction Agency, Ft. Belvoir, VA

The Nuclear Detection Technology Division at the Defense Threat Reduction Agency develops radiological and nuclear sensors to fulfill DoD operational requirements. Energy-resolved directional imagers for wide-area search applications, handheld gamma spectrometers for local search and inspection, systems for shielded item detection, and sensors for distributed sensor applications such as tracking will be reviewed.

26.2: First 3-D CdZnTe Array Systems for Gamma-Ray Imaging and Spectroscopy (1:50)

Z. He
The University of Michigan, Ann Arbor, MI

The first array system with a detection volume of about two orders of magnitude larger than the largest detector constructed thus far and with an angular resolution of about 3–5° has been developed. The system should be able to detect the presence of 1 kg of highly enriched uranium within a radius of 5 m in about 1 minute. Furthermore, detectors using CdZnTe and HgI_2 can detect the presence of neutrons, another unique signature of fissionable materials. The capability of performing gamma-ray spectroscopy with the best possible energy resolution at ambient temperatures and detecting neutrons with good efficiency will put three-dimensional position-sensitive wide-band-gap semiconductors among the most-sensitive high-performance radiation detectors for detecting special nuclear materials.

26.3: High-Efficiency Perforated Semiconductor Neutron Detectors (2:10)

D. S. McGregor, J. K. Shultis, W. Dunn, S. Bellinger
Kansas State University, Manhattan, KS

A neutron-detector configuration utilizing microscopic perforations backfilled with neutron reactive materials offers a solution to increase detection efficiency. The pin-diode detectors have millions of microscopic perforations backfilled with 6-LiF. Efficiencies exceeding 12% thermal neutron detection efficiency have been reached for devices only 500-μm thick.

26.4: Passive Gamma-Ray Detection of Special Nuclear Materials **(2:30)**

B. Philips, E. Novikova, E. Wulf, J. Kurfess
Naval Research Laboratory, Washington, DC

The performance of a non-imaging scintillating array was compared to the performance of two imaging arrays: a coded aperture imager and a Compton imager. The sensitivity was modeled at three energies for the emission from a 1-kg sphere of uranium enriched to 95% U-235: the 185-keV emission from U-235, the 1001-keV emission from U-238, and the 2614-keV emission from U-232.

BREAK **(3:00)**

Session 27

EO SURVEILLANCE TECHNOLOGY FOR THE GWOT

Thursday, March 22 / 1:30 – 3:00 pm / Coronado Q&R

Chair: **Linda Mullen**
NAVAIR, Patuxent River, MD

27.1: **Eye-Safe Laser Surveillance: From Imaging to Chemical Detection** **(1:30)**

R. Billmers, E. Billmers, M. Ludwig, M. Van Buren
RL Associates, Inc., Chester, PA

Systems to protect soldiers and first responders from what they cannot see are being developed. Current systems under development have various applications including (i) enabling first responders and military personnel to image through fire and smoke and (ii) enabling military personnel to remotely detected IEDs and chemical/biological agents.

27.2: **Hybrid Lidar-Radar for Underwater Imaging and Communications Applications** **(1:50)**

L. Mullen, B. Cochenour, A. Laux
NAVAIR, Patuxent River, MD

The Hybrid Lidar-Radar technique combines the penetration capability of light with the benefits of radar modulation and detection schemes. Use of this hybrid approach for underwater imaging has resulted in enhanced image contrast. This hybrid technology can also be used to transmit and receive information underwater via a wireless optical link. Both applications will be discussed.

27.3: **Wide-Field-of-View Retroreflectors for Short-Range Free-Space Optical Communications** **(2:10)**

J. Muth, K. Alhammadi, E. Grant
NCSU, Raleigh, NC

High-bandwidth short-range optical communications links are of increasing interest. The requirements for underwater modulating retroreflectors will be discussed, including preliminary results for wide-bandgap-semiconductor optical modulators. Novel wide-field-of-view retroreflectors with fields of view near 180° will be presented.

27.4: **Joint Multi-Mission Electro-Optic System (JMMES) Joint Capability Technology Demonstration (JCTD)** **(2:30)**

J. E. Prentice, V. M. Contarino
NAVAIR, Patuxent River, MD

The Joint Multi-Mission Electro-Optic System (JMMES) Joint Capability Technology Demonstration (JCTD) program that applies selectively developed auto-detection and auto-cueing algorithms to a system of state-of-the-art passive electro-optic sensors integrated into a militarized 15-in. turret that provides real-time day/night localization, identification, tracking, and targeting capability for multiple combatant command (COCOM) joint missions will be described. The sensor hardware, a result of a decade of E-O technology work that has resulted in a suite of commercial-off-the-shelf (COTS) sensors that is a mature, proven technology will also be described.

BREAK **(3:00)**

Session 28

ADVANCED PACKAGING: FUNCTIONAL INTEGRATION I

Thursday, March 22 / 1:30 – 3:00 pm / Coronado S&T

Chair: **Eric D. Adler**
Army Research Laboratory, Adelphi, MD
Co-Chair: **Mark Andrew Gouker**
MIT Lincoln Laboratory, Lexington, MA

28.1: **Optical/Electrical Technologies for High-Speed-Signal Communications in High-Performance Servers** **(1:30)**

J. A. Kash
IBM T. J. Watson Research Center, Yorktown Heights, NY

The status and possible future of optical interconnects placed inside high-performance servers will be discussed for several regimes of interconnects: rack-to-rack, between chips or modules on a circuit board including a back-plane, and within a chip. Possible implementations are discussed.

28.2: **3-D Integration Technologies and Applications** **(1:50)**

V. Ozguz
Irvine Sensors Corp., Costa Mesa, CA

The ever-increasing demand for more electronic functionality in smaller volumes requires new approaches. One solution is to use the third dimension by combining multiple layers of integrated circuits that overcomes the limitations of planar approaches. A general overview of 3-D packaging and integration approaches will be presented in relation to systems and applications that will benefit from 3-D implementation.

28.3: **Materials, Devices, and Heterogeneous Integration for New Functions** **(2:10)**

S. Banerjee
University of Texas, Austin, TX

There is interest in heterogenous integration of advanced memory and logic devices to enhance Si CMOS. Work funded by DARPA/MTO in biologically inspired nanoscale self-assembly of quantum-dot flash memories and Si-Ge-C heterostructure channel enhnaced mobility MOSFETs will be discussed.

28.4: **Miniaturization Technologies for System-Scale Functional Integration** **(2:30)**

P. C. Karulkar
University of Alaska, Fairbanks, AK

Using some specific examples, the trends and developments in miniaturization technologies for system-scale functional integration will be discussed and the challenges facing the further advancements and wider application of miniaturization technologies will be described.

BREAK **(3:00)**

Session 29

CRITICAL NUCLEAR DETECTION ACTIVE SENSOR TECHNOLOGIES FOR HOMELAND SECURITY

Thursday, March 22 / 3:30 – 5:00 pm / Durango 1&2

29.1: Nuclear Detection Sensor Opportunities in Active Interrogation for Homeland Security (3:30)

R. L. Feinstein
Department of Homeland Security, Washington, DC

Under the Office of Transformational Research and Development, an aggressive program of exploratory research is under way to make significant advances in basic detection technology. A brief overview of the DNDO R&D mission objectives and implementation strategy will be discussed with particular emphasis on opportunities in nuclear detection sensor technologies for particle interrogation screening solutions.

29.2: Nuclear-Material Detection by Neutron-Based Techniques (3:50)

T. Gozani
Rapiscan Systems Neutronics and Advanced Technologies, Santa Clara, CA

Neutron-based inspection techniques are very efficient in detecting concealed nuclear materials such as U235 or Pu239. The highly sensitive detection via the differential die-away analysis of prompt fission neutrons is in an advanced stage of development and will be described along with auxiliary techniques using delayed fission radiations.

29.3: Active Photon Interrogation Techniques for Detecting Nuclear Materials (4:10)

R. J. Ledoux, W. Bertozzi, S. Korbly, W. Park
Passport Systems, Inc., Acton, MA

Nuclear resonance fluorescence (NRF), an active high-energy-photon-based technique, provides a signal that is unique and present for all nuclei with Z > 2. All isotopes have different NRF signatures enabling, for example, the discrimination between high-Z shielding and fissile materials. The development status of a non-intrusive scanner-based on NRF will be presented.

29.4: Novel SiCDetector for Active Inspections (4:30)

J. G. Seidel, R. W. Flammang, F. Ruddy
Westinghouse Electric Co., Pittsburgh, PA

J. L. Jones
Idaho National Laboratory, Idaho Falls, ID

A novel silicon carbide detector is now being utilized to successfully address both neutron- and bremsstrahlung-type inspection applications. Although this paper describes this detector and highlights efforts related to neutron inspection, it will focus on bremssstrahlung-type inspection applications and the detector's neutron and photon detection performance.

Session 30

TECHNOLOGIES FOR URBAN WARFARE

Thursday, March 22 / 3:30 – 5:00 pm / Coronado Q&R

Chair: **Kathleen A. Griggs**
Puritan Research Corp., Vienna, VA
Co-Chair: **Deepak Varshneya**
DARPA/STO, Arlington, VA

30.1: Soldier-Wearable System for Shooter Localization and Weapon Classification (3:30)

A. Ledeczi, P. Volgyesi, T. Bapty
Vanderbilt University, Nashville, TN

A soldier-wearable small microphone array was developed to localize shooters. Multiple units can share their information via an ad hoc wireless network and localize the shots with even higher precision and estimate the caliber and weapon type at high accuracy. An independent evaluation reported a 1° azimuth and over 90% classification accuracy.

30.2: Integration of Vision-Based Obstacle Avoidance on Micro Air Vehicles for Flight in Cluttered Urban Environments (3:50)

J. E. Corban
Guided Systems Technologies, Inc., McDonough, GA

Micro air vehicles promise to make the proven advantages of unmanned flight systems available to the smallest units and even individual soldiers. However, integration of vision-based obstacle avoidance, a rapidly maturing technology, is precluded by severe constraints on size, weight, and power consumption. The state of this guidance technology is reviewed and the need for advanced microelectronic solutions is identified.

30.3: Compact Tunable High-Power Microwave System for Vehicle Immobilization (4:10)

J. Tatoian
Eureka Aerospace, Pasadena, CA

G. Gibbs
MARCORSYSCOM, Quantico, VA

W. Nunnally
University of Missouri, Columbia, MO

H. Lackner
E&TS, Oakland, CA

A compact, tunable, high-power electromagnetic system is being developed for the remote immobilization of vehicles using microwave energy to disable/damage a vehicle's electronic control module/microprocessor which controls the engine's vital functions. The system is capable of (1) high-value asset perimeter protection, (2) bringing automobiles to a halt on highways, and (3) perimeter protection for gas-oil (fueling) platforms at sea. The host platforms for HPEMS include ground vehicle, helicopter, or UAV. The HPEMS can be utilized in law enforcement and homeland security and applications such as counter-terrorism activities.

30.4: Frequency-Agile Radios Using MEMS Resonators (4:30)

K. J. Smart, R. H. Olsson, III, D. Ho, D. Heine, J. G. Fleming
Sandia National Laboratories, Albuquerque, NM

One of the primary challenges of communicating in urban environments is frequency-selective fading caused by multipath interference. In order to combat fading in small radios, Sandia has been investing in the development of small CMOS-compatible MEMS resonators. The use of several of these on-chip resonators allows for small, high-performance radios with frequency agility to combat frequency-selective fading.

Session 31

ADVANCED PACKAGING: FUNCTIONAL INTEGRATION II

Thursday, March 22 / 3:30 – 5:10 pm / Coronado S&T

Chair: **Mark Andrew Gouker**
MIT Lincoln Laboratory, Lexington, MA
Co-Chair: **Daniel J. Radack**
Institute for Defense Analyses, Alexandria, VA

31.1: 3-D Packaged GaAs–Si T/R MMIC (3:30)

S. Burkett
University of Arkansas, Fayetteville, AR

C. Essary
REMEC D&S, Forsyth, MO

G. McGuire
ITC, Research Triangle Park, NC

S. Nelson
REMEC D&S, Richardson, TX

A three-dimensional (3-D) packaging technique to vertically interconnect a silicon control IC to a GaAs transmit/receive (T/R) MMIC will be described. The X-band T/R MMIC is fabricated using the GCS 0.5-µm E/D pHEMT process and is designed for a thick dielectric coating. A through-silicon via (TSV) process developed by the University of Arkansas, Fayetteville, provides necessary interconnects through and routing across the silicon control IC, and 30-µm-diameter 80-µm-high copper posts are used to connect the silicon and GaAs ICs into a vertical 3-D package. This silicon GaAs 3-D package takes up one-third the area of conventional plastic- or ceramic-packaged T/R MMIC and ASIC circuits.

31.2: Thin-Film Liquid-Crystal-Polymer Surface-Mount Packages for Millimeter-Wave Applications (3:50)

A-V. Pham
University of California at Davis, Davis, CA

Multilayered thin-film liquid-crystal-polymer surface-mount packages for millimeter-wave applications are being developed. A package feed-through has an insertion loss of ~1 dB and a return loss of ~15 dB at 30 GHz. The package is enclosed with an LCP lid to provide moisture protection.

31.3: Dual-Function Heat-Sink Antennas for 3-D RF System Integration (4:10)

L. Covert, J. Lin
University of Florida, Gainesville, FL

D. Janning, T. Dalrymple
AFRL, Wright-Patterson AFB, OH

Dual-function heat-sink antennas that radiate electromagnetic and thermal energy are introduced. 5.8- and 2.4-GHz heat-sink antennas were fabricated using a hybrid patch antenna approach. Simulations and measurements are reported. Significant increases in radiation efficiency, gain, and bandwidth were achieved with the heat-sink antennas over their basic patch antenna counterparts.

31.4: Multilayer MMIC Integration Using Wafer-Scale Assembly (4:30)

P. Chang-Chien, M. Yajima, C. Cheung, X. Zeng
Northrop Grumman Space Technology, Redondo Beach, CA

A multilayer integration technology at the wafer scale using a wafer packaging process has been developed. This wafer-scale assembly method can be used to assemble substrates with different thicknesses and cavity heights. Three- and four-layer wafer-stack construction has been demonstrated, and assembly sequence as well as data obtained from these multiple wafer stacks will be presented.

31.5: Thin-Film LCP Capping of RF MEMS (4:50)

J. Iannotti, C. Kapusta
GE Global Research Center, Niskayuna, NY

N. Karabudak
Lockheed Martin Commercial Space Systems, Newtown, PA

The development of a wafer-scalable hermetically sealed packaging solution for rf microelectromechanical system (MEMS) switches using a liquid-crystal-polymer (LCP) film will be described. Cavities were formed in the LCP film and then laminated, at low temperature, onto the Si MEMS switch wafer to create a hermetically sealed wafer-scale planar MEMS package. The sealed MEMS switches can be diced up and incorporated into next-level assemblies using a variety commercially available attach methods that have inherently low parasitics, including flip-chip and solder attach.

COMPONENTS FOR ELECTRONICALLY SCANNED ARRAYS

Thursday, March 22 / 9:00 am – 12:00 pm / Coronado L

Chair: **Chris W. Hicks**
Naval Air Systems Command, Patuxent River, MD

32.1: **Withdrawn**

32.2: **Efficient Operation of Traveling-Wave-Tube Amplifier with Dynamically Adjusted Collector Bias Voltages**

J. X. Qiu, D. K. Abe, B. G. Danly
Naval Research Laboratory, Washington, DC

T. M. Antonsen, Jr.
University of Maryland, College Park, MD

An efficiency-enhancement technique for traveling-wave-tube amplifiers (TWTAs) for applications in digital communications systems will be described. The enhancement is obtained by tracking the envelope of the input waveform and dynamically changing the bias voltages of the depressed collectors according to the instantaneous amplitude of the input waveform.

32.3: **Miniature Tunable Combline Filters**

S. Mehta, P. Petre, J. Foschaar
HRL Laboratories, Malibu, CA

HRL Laboratories' progress in developing state-of-the-art extremely miniature, tunable combline filters for the C, X, and Ku-bands will be reported. These filters are essential components for ONR's Advanced Multifunction RF System Concept (AMRF-C). The salient filter features are small size, low insertion loss, high tunability, and fast response time.

32.4: **Wideband Low-DC-Power mHEMT LNAs for Active Phased Arrays**

E. Crespin, D. Greenway, M. Montano, K. Gass
Sandia National La+boratories, Albuquerque, NM

A key challenge for next-generation phased arrays is to minimize power per active element. To address this challenge, wideband low-DC-power LNAs have been developed and demonstrated. RF bandwidths of 4–18 GHz with 2-dB noise figure and 10-dB gain per stage have been achieved using mHEMT technology.

32.5: **Withdrawn**

32.6: Optical Fourier Cell for Optical True Time Delays

D. Rabb, B. L. Anderson
The Ohio State University, Columbus, OH

W. Cowan, O. Blum-Spahn
Sandia National Laboratories, Albuquerque, NM

An optical Fourier cell allows arrays of light beams to be individually steered among different optical paths to provide many bits of true-time delay for hundreds of antenna elements in a very small volume. The first experimental reduction-to-practice using MEMS micromirrors and a slow-tool-servo diamond-turned mirror array will be reported.

32.7: Miniature Wideband RF Channelizer ASIC for Overlapping Pulse Detection

H. L. Levitt, E. W. Justh, T. A. Roberts
Tactical Electronic Warfare Division, Naval Research Laboratory, Washington, DC

F. J. Kub
Electronics Science & Technology Division, Naval Research Laboratory, Washington, DC

A channelizer uses a bank of filters to decompose a high-frequency input signal into a collection of baseband signals corresponding to the power in successive equally spaced frequency bins. For continuous-wave (CW) signals, the steady-state outputs of the channelizer indicate which frequencies are present. For pulse-modulated radar signals, spillover into adjacent frequency channels at the leading and trailing edges – the “rabbit ear” effect – significantly complicates information extraction from the channelizer output. Because of the broadband spectral content of short pulses, this difficulty cannot be circumvented through choice of filter order and bandwidth: an entirely different approach is required. By using a novel technique based on non-linear and cross-channel processing, efficiently implemented as a mixed-signal ASIC, a compact low-power rf channelizer optimized for detection of pulsed signals, including time-overlapping pulses at multiple frequencies, in real time, has been developed.

ELECTRONICALLY SCANNED ARRAYS

Thursday, March 22 / 9:00 am — 12:00 pm / Coronado L

Chair: **Chris W. Hicks**
Naval Air Systems Command, Patuxent River, MD

33.1: **Withdrawn**

33.2: **Withdrawn**

33.3: **Withdrawn**

33.4: **Low-Power-Density-Panel Phased Array**

A. Puzella
Raytheon, Sudbury, MA

A low-power-density-panel array integrating patch radiators, dual linear-polarized feed, rf beam-forming, dc, and digital control have been designed. An air-cooled 0.21-µm-thick 128-T/R-channel panel array weighing 2.16 lbs. with a surface-mounted flip-chip SiGe MMIC and a GaAs LNA was demonstrated. The power radiated per channel was 10 mW.

33.5: **Withdrawn**

ELECTRONICS FOR EXTREME ENVIRONMENTS

Thursday, March 22 / 9:00 am – 12:00 pm / Coronado L

Chair: **Chris W. Hicks**
Naval Air Systems Command, Patuxent River, MD

34.1: Ultra-Dynamic Voltage Scaling for Energy-Starved Electronics

A. Wang
Texas Instruments, Dallas, TX

A. Chandrakasan
MIT, Cambridge, MA

Many burst-mode applications require high-performance for brief time periods between extended sections of low-performance operation. Sub-threshold circuits can minimize energy for computations executed during the low-performance slots. The key challenges that oppose sub-threshold circuit design will be identified and the fabricated chips that verify techniques for overcoming the challenges will be described.

34.2: SOI and SOS MESFETs for Extreme-Environment Electronics

J. Ervin, A. Balijepalli, A. Shanmugam
RF Micropower, Inc., Fountain Hills, AZ

T. Thornton
Arizona State University, Tempe, AZ

It has been demonstrated that SOI MESFETs can be fabricated using commercial CMOS foundries. Recently, the MESFET process flow has been adapted to make it compatible with silicon-on-sapphire (SOS) technologies. The latest results from SOI and SOS MESFETs will be presented, and their potential application for extreme-environment electronics will be discussed.

34.3: Extreme-Environment Modeling Tools for Scaling the TRL Mountains

A. Mantooth, J. Holmes, C. Webber, M. Francis
Lynguent, Fayetteville, AK

Modeling tools that enable the addition of extreme-environment effects, including both radiation and temperature effects, will be described. An example of how this integrated modeling environment promotes ascention through Technology Readiness Levels will be discussed.

34.4: The Development of a Motor-Drive Power Stage for Cryogenic Space Environments

J. Garrett, R. Schupbach, A. B. Lostetter
Arkansas Power Electronics International, Inc., Fayetteville, AK

H. A. Mantooth
University of Arkansas, Fayetteville, AK

Various components and component technologies utilized in motor-drive applications were cryogenically tested to determine which component technologies would demonstrate promising performance for operation in extreme cold environments. Based upon the results of these tests, components were selected to fabricate a dc motor-drive power stage that was cryogenically tested.

34.5: A Rad-Hard 16M SRAM for Space Applications

S. Doyle, T. Hoang, J. Ross, N. Haddad
BAE Systems, Manassas, VA

A high-performance 16M SRAM is being developed in the 0.15-µm CMOS RH15 technology and is intended for use in space and other strategic rad-hard applications. The SRAM design is implemented in a 1.5-V 0.15-µm seven-layer-metal CMOS technology. Using integrated process features and advanced design techniques, SEE immunity beyond LET of 199-MeV/mg/cm^2 and worst-case performance of less than 15 nsec have been achieved.

34.6: Manufacturability of 0.1-µm AlSb/InAs HEMTs for Low-Power Applications

Y. C. Chou, J. M. Yang, M. Lange, C. Lin, M. Lange, C. Lin
Northrop Grumman Corp., Redondo Beach, CA

Excellent uniformity of 0.1-µm metamorphic AlSb/InAs HEMTs on 3-in. GaAs substrates were demonstrated. This is mainly attributed to the improvement of epitaxial material, gate processes, and nitride passivation. The excellent uniformity achieved suggests possible large-volume fabrication of low-power electronics for military and space applications using metamorphic AlSb/InAs HEMT technology.

34.7: Development of Reprogrammable Low-Power High-Density High-Speed Rad-Hard FPGAs Using Proven Commercial Technology and RADHARD-by-Process Techniques

R. Manohar, C. W. Kelly, J. L. Holt, C. Liu
Achronix Semiconductor Corp., San Jose, CA

Demand for high-performance field-programmable gate arrays (FPGAs) with performance defined in terms of speed, power, and density are increasing in both the commercial and military markets. Massive NRE costs for custom application-specific integrated circuits (ASICs) combined with the high unit costs of low-to-mid-volume production of ASICs make FPGA an economical and high-performance alternative for a wide range of applications. BAE Systems, in partnership with the DoD community, has implemented rad-hard 150-nm bulk CMOS process technology in a facility located in Manassas, Virginia. Using this process technology, the Achronix architecture is currently being adapted into a RADHARD-by-process FPGA in cooperation with BAE Systems. The BAE Systems' RADHARD process provides the capability to achieve 1-MRAD total internal dose.

34.8: Withdrawn

34.9: Implications of Cold-Temperature Environments for Single-Event Radiation Effects

M. L. Alles, R. A. Reed, A. N. Kalavagunta, B.D. Sierawski
Vanderbilt University, Nashville, TN

TCAD simulations of silicon MOSFETs and SiGe HBTs indicate that single-event effects are exacerbated at cold temperatures, such as those targeted for lunar applications. Results suggest the need for additional modeling and experimental investigation because HBD techniques may require adaptation to account for enhancement of the low-temperature SE response.

HIGH-PERFORMANCE ELECTRONICS

Thursday, March 22 / 9:00 am – 12:00 pm / Coronado L

Chair: **Chris W. Hicks**
Naval Air Systems Command, Patuxent River, MD

35.1: Signal Sources and Detectors Operating Near 200 GHz Fabricated in CMOS

K. K. O, J. E. Brewer, C-H. Cao, E-Y. Seok
University of Florida, Gainesville, FL

The feasibility of CMOS circuits operating at frequencies approaching 200 GHz has been demonstrated. A 140-GHz fundamental-mode VCO in 90-nm CMOS, a 192-GHz push-push VCO in 130-nm CMOS, and a 180-GHz detector circuit in 130-nm CMOS have been designed, fabricated, and tested. The VCO circuits exhibit the highest fundamental and harmonic operating frequencies ever achieved by silicon integrated-circuit technology. The Schottky diode in the detector circuit has a 1.5-THz cutoff frequency.

35.2: Parameterizable Decimation-Based Digital Receiver for High Update Rate

P. Buxa, G. Creech
AFRL/SND, Dayton, OH

M. Emmert
Wright State University, Dayton, OH

A parameterizable decimation-based digital receiver has been designed for the purpose of trading update rate for frequency resolution without loss of dynamic range. In addition, the design is written in generic VHDL that is compiler, simulator, and synthesis-tool independent. The parameterizable code is written so it can be used to automatically generate hardware for varying mission requirements. It addresses legacy system issues and is fabrication process independent, so it can target current or future FPGA or ASIC-based implementation technologies. The receiver can currently be demonstrated on a Xilinx FPGA, and a 4-GHz IC layout that targets the IBM 8RF technology is being developed.

35.3: Withdrawn

35.4: MonoBIT Receiver Architecture and Signal Threshold Determination

J. Buck, J. Tsui, S. Hary, K. Graves
AFRL/SND, Dayton, OH

The MonoBIT receiver was developed by AFRL. It is a wideband (1-GHz) device similar to Instantaneous Frequency Measurement (IFM) receivers, but it is capable of detecting two or more simultaneous signals. Details of the current FPGA-based, MonoBIT receiver architecture as well as the MonoBit design is targeted for wide bandwidth frequency detection that can be implemented as a queuing receiver or a standalone receiver. The MonoBIT was scheduled for flight test in Northrop Grumman's Inventus UAV sometime in November 2006.

35.5: Trusted Chip

G. Fitzhugh, J. Bellando, S. Williamson
EDAptive Computing, Dayton, OH

Two areas of FPGA security that seemingly are not addressed by industry are (1) an unprogrammed FPGA that contains undetected, malicious programming into which a design is synthesized and (2) a fully packaged FPGA that has a malicious device in the package itself.

35.6: 2-D Modeling of Current–Voltage Characteristics of AlGaN/AlN/GaN High-Electron-Mobility Transistors

R. K. Jain, S. R. Winzer
Lockheed Martin Space Systems Co., Palo Alto, CA

GaN-alloy-based high-electron-mobility transistors (HEMTs) have shown excellent performance and are attractive for space and Earth-based commercial and defense applications (communications, radars, missiles). This work presents two-dimensional modeling results for an AlGaN/AlN/GaN HEMT device using the ATLAS device-simulation code from Silvaco. To the best of our knowledge, these are the first reported modeling results incorporating high-bandgap (6.2 eV) AlN sub-barrier layer in an AlGaN/G+aN HEMT device. The results are compared with the measured drain current (Ids) versus gate voltage (Vgs) data. The effects of electron mobility and interface charge density on the device-transfer characteristics have been calculated. The device modeling could play an important role in optimizing the device design to improve the performance and understand the physics of failure affecting the reliability of these devices.

35.7: Withdrawn

35.8: Withdrawn

35.9: Automatic Match Control for Cognitive RF Front Ends

K. L. Melde
University of Arizona, Tucson, AZ

W. R. Eisenstadt
University of Florida, Gainesville, FL

The design of a dynamically reconfigurable automatic match control (AMC) circuit will be presented. The AMC consists of an impedance tuner, an S11 detector, and bias control circuits. A 5-GHz impedance tuner with a 30% instantaneous bandwidth has been designed and tested. The results of the integration of the tuner with a UWB antenna demonstrate the spectral agility achieved by AMC.

35.10: Ultrafast Monolithic Picosecond Sampler and Pulser Architecture

H. L. Levitt
Naval Research Laboratory, Washington, DC

J. M. Libove, S. J. Chacko, B. R. Illingworth
Furaxa Corp., Orinda, CA

A fully monolithic dual-function sampler and pulser ASIC architecture that can generate pulses or sampling apertures in the 2–10-psec range with repetition rates up to 30 billion pulses per second and jitter too low to measure with conventional test equipment will be developed. A fully monolithic implementation enables small, low-cost, and power-efficient samplers and pulsers to be deployed in a variety of critical applications, including secure UWB LPOI/LPOD communications, wideband digital rf memory (DRFM), impulse radar, and direct satellite up-conversion and down-conversion.

35.11: Ultra-Thin Packaging of CMOS Silicon-on-Insulator (SOI)

Bruce Offord, Hugo Jazo
SPAWAR, San Diego, CA

Joe Ianotti, Christopher Kapusta
GE Global Research, Niskayuna, NY

An advanced form of interconnect using high-density interconnect (HDI) technology, combined with ultra-thin silicon-on-insulator (SOI)CMOS technology, will be described. A manner of interconnect that can be used for 3-D integration, as well as for ultra-thin form factor and mechanically flexible circuits, is demonstrated.

PHOTONICS AND OPTOELECTRONICS

Thursday, March 22 / 9:00 am – 12:00 pm / Coronado L

Chair: **Chris W. Hicks**
Naval Air Systems Command, Patuxent River, MD

36.1: Nano ZnO UV Sensors: Enhanced Sensitivity Due to Micro-Spheres in a Matrix of Nanowires

S. S. Hullavard, P. C. Karulkar
University of Alaska, Fairbanks, AK

Nanostructure ZnO-based UV detectors were fabricated by utilizing the naturally grown combination of ZnO microspheres (2–3 μm) embedded in a matrix of ZnO nanowires (50–80 nm). ZnO nanostructures were grown by using the direct vapor-phase method. Nanostructures were characterized by PL and studied under oxygen pressure. These multistructures offer enhanced sensitivity.

36.2: MEMS-Based Photonic Switching Developments

S. Yuan, R. Helkey, V. Kaman, O. Jerphagnon
Calient Networks, Inc., Goleta, CA

Recent MEMS-based photonic switch-technology developments and high-density photonic switch module integrations that are important for many types of government systems will be presented. The MEMS device, fiber-optic components, optical performances, module integration, and reliability data of high-port-count photonic switches will be given.

36.3: THz Thermal Radiation Enhancement Using Photonic Crystals

H. Xin, Z. Wu
University of Arizona, Tucson, AZ

A. Young
Raytheon Missile Systems, Tucson, AZ

A new idea for the thermal radiation-based THz source utilizing photonic crystals will be introduced. Preliminary theoretical and experimental results will be reported, and promising indications that a new type of low-cost and high-performance THz source may be realized using carefully designed photonic crystal thermal radiators will be discussed.

36.4: Withdrawn

36.5: Indium Gallium Zinc Oxide: A Material for Transparent Electronics

J. Muth, A. Suresh, P. Wellenius
North Carolina State University, Raleigh, NC

Recent developments for amorphous wide-bandgap semiconducting oxides show that they have 1–2-orders-of-magnitude-higher electron mobility than amorphous silicon. The materials are transparent to visible light, enabling the fabrication of transparent thin-film transistors that are an enabling technology for transparent electronics.

36.6: Power-Savings Techniques for Optical and Electrical High-Speed Data Links

F. Kiamilev, J. Kramer
University of Delaware, Newark, DE

Various techniques for dynamic power optimization that our research group has developed will be reviewed. One set of methods provides different levels of speed and power depending on the current workload of the system. Another set uses bit-error-rate (BER) requirements for the link to power savings.

36.7: Spectrophotometric Characterization of Complex Refractive Index of $Cd_xZn_{1-x}O$ for Photonic Device Applications

W. V. Schoenfeld, J. W. Mares, M. Falanga
College of Optics and Photonics, Orlando, FL

A. Osinsky, B. Hertog
SVTA, Eden Prairie, MN

Epitaxially grown $Cd_xZn_{1-x}O$ epilayers were characterized by spectrophotometry to determine their complex indices of refraction through the UV/visible wavelength range. Transmission spectra were analyzed using an evolutionary algorithm yielding the real and imaginary parts of the refractive index and the band-gap energies as a function of cadmium concentration.

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