GOMACTech-08

Government Microcircuit Applications and Critical Technology Conference

PROGRAM

"Microsensor Technologies Enabling Information on Demand"

March 17 – 20, 2008

Riviera Hotel
Las Vegas, Nevada

www.gomactech.net

GOMACTech-08
ADVANCE PROGRAM
CONTENTS

WELCOME

The GOMACTech-08 Program Committee is pleased to welcome you to this year's conference in Las Vegas, Nevada. GOMACTech is the pre-eminent conference for the review of developments in microcircuit applications for government systems. GOMACTech was established in 1968 and is an unclassified export-controlled event that requires all participants to be U.S. Citizens or legal U.S. Permanent Residents. Historically, the Conference has been the venue to announce major government microelectronics initiatives such as VHSIC, MIMIC, and others. This year also marks a new milestone for the technical breath of GOMACTech. This is the first year that the interests of the Space Environmental Effects Working Group (SEEWG) will be integrated into the Conference. We welcome the participation of this technical community.

This year's conference theme, "Microsensor Technologies Enabling Information on Demand," provides a forum that highlights emerging highly innovative technologies that provide a bridge from the world today to the world of tomorrow where information is available on demand everywhere. The proliferation of cognitive emerging nanometer-scale integrated electronics embedded in government and civilian systems will create a world in which information access is ubiquitous and available on demand at anytime and from anyplace. The capability to communicate seamlessly throughout the world requires complex wired and wireless networks that utilize nano- and micro-scale transducers that sense and interact with the physical environment. Development of secure, robust, intelligent sensor networks that deliver information instantaneously between urban and rural areas is also a necessary element for defending our homeland and protecting our national interests. Critical research in nano-circuit technologies is the prime driver for integrating and deploying cognitive sensors into miniature and large electronic systems for military, homeland defense, space systems, and medical applications. Topics that support this vision are highlighted at this year's conference.

The conference will follow the successful format used over the past several years, with both technical and topical sessions. The technical sessions comprise contributed and solicited papers, including oral presentations and a Thursday morning poster session. A special section of the poster session will highlight the work of student contributors. This is a new feature of this year's GOMACTech. The topical sessions will focus on a broad range of developments and accomplishments ranging from components to systems within selected ongoing government-sponsored programs. Some of this year's topical session themes are

Wide-Bandgap RF Semiconductors
Nanotechnology for Systems
Ultra-High-Speed Transistors
Ultra-Low-Power RF Transceivers
Autonomous Sensor Platforms
Embedded Command and Control
THz Sources
Space-Environment Modeling
Space-Environment Monitoring
Advanced A/D Front-End Processors and Components
Rad-Hard Microelectronics Technologies
Power Electronics

Two outstanding tutorials are offered on Monday with the cost included as part of the conference registration fee. The first tutorial, "Micro-Sensor Networks," will review recent progress made in micro-sensor network technology, cover applications in defense and commercial sectors, and review the outlook for the future. We will trace the evolution of the technology through several DARPA

programs (such DSN, SensIT, NEST, and others) and through deployments. This tutorial will be conducted by Srikanta (Sri) Kumar, Eric Hoenes, and Steve Beck from BAE Systems, Dr. Jeff Paul from DARPA/IXO, Dr. Akos Ledeci from Vanderbilt University, and Tom Rosenbury from Sperient, Inc. The second tutorial, "Introduction to Radar Systems," will provide an indebt understanding of radar-system concepts and technologies and instill a basic working knowledge of radar systems. John Wilkinson and Robert Galejs from MIT Lincoln Laboratory will present this tutorial.

The conference formally opens on Tuesday morning with an outstanding Plenary Session including a Keynote presentation by Dr. Anthony J. Tether, Director, Defense Advanced Research Projects Agency, Arlington, VA. Dr. Tether's Keynote will be followed by three Kilby Lecture speakers: Dr. Starnes Walker, Director of Research, Department of Homeland Security (S&T); Dr. William S. Rees, Jr., Deputy Under Secretary of Defense (Laboratories and Basic Sciences), Office of the Director, Defense Research and Engineering; and Dr. Andrea Goldsmith, Professor of Electrical Engineering, Stanford University, Stanford, CA.

The Plenary, Technical, and Topical Sessions are the major venues for information exchange at the conference. Other opportunities for technical interaction are provided through the Exhibit Program that includes major IC manufacturers and commercial vendors of devices, equipment, systems, and services for nearly all facets of the electronics business. The exhibition opens on Tuesday at noon and runs through Wednesday at 4:00 pm. The Wednesday Luncheon speaker will be LtCol Tom Arnold, USMC, G-6 Marine Forces, U.S. Strategic Command. Col. Arnold will provide operational experience “in theatre” to help give real-world motivation to the researchers in the area of networking and communications. The title of his speech is “That's Great -- But Where Do I Plug into the Network.” On Tuesday evening, attendees can mix in a relaxing atmosphere of food and good spirits at the Exhibitors’ Reception sponsored by Northrop Grumman Corp. Wednesday evening features the conference banquet, which this year will be held at the Monte Carlo Hotel, followed by the world-renowned master magician Lance Burton and his “Magic Show.”

This year's strong technical program reflects the hard work and enthusiasm of the GOMACTech-08 Technical Program Committee. The committee members aggressively sought out particular topics and areas for presentations, and the quality of the conference certainly reflects this effort. It is our hope and belief that GOMACTech-08 will be a rewarding experience for all participants. We appreciate your support.

Gerry Borsuk
Conference Chair

Chris Hicks
Technical Program Chair

REGISTRATION

All GOMACTech-08 sessions will be held at The Riviera Hotel in Las Vegas, Nevada. Both check-in and on-site registration wil take place in the hotel's Convention Center Foyer.

Conference check-in and on-site registration hours:

Monday, 17 March	–	9:00 am – 5:00 pm
Tuesday, 18 March	–	7:00 am – 5:00 pm
Wednesday, 19 March	–	7:00 am – 5:00 pm
Thursday, 20 March	–	7:00 am – 5:00 pm

SECURITY PROCEDURES

The GOMACTech Conference is an Unclassified, Export-Controlled event that requires participants to be U.S. Citizens or legal U.S. Permanent Residents. All registrants must provide proof of U.S. Citizenship or Permanent Resident status prior to being permitted entry into the conference. Additionally, a signed **Non-Disclosure Statement** will be required.

You may prove U.S. citizenship with any of the following:
U.S. Passport
Birth Certificate **AND** valid government-issued photo ID
Naturalization Certificate **AND** valid government-issued photo ID

The following are NOT proof of citizenship:
Voter registration card
Driver's license

GOMACTech TUTORIALS

Two tutorials of interest to the GOMACTech community are a special feature of the conference. The tutorials are both being held on Monday, 17 March. There is no additonal fee for the tutorials, but registrants must indicate their intention to attend on the registration form.

Tutorial 1: Introduction to Radar Systems

Monday, March 17, 10:00 am – 5:00 pm
The Rivera Hotel, Capri Room 101

Organizer:
Chris Johnson, MIT Lincoln Laboratory, Lexington, MA

This tutorial was developed to provide an understanding of radar system concepts and technologies and to instill a basic working knowledge of radar systems. It begins with an introductory description of basic radar concepts and terms. The radar equation, needed for the basic understanding of radar, is developed, along with several examples of its use in radar systems design. Radar propagation issues, such as attenuation, multipath effects, and ducting, are described. The concepts of radar cross section, waveform design, transmitter and receiver characteristics, and the detection of radar signals in the presence of noise are presented.

Some radars are required to detect small targets in the presence of much larger radar echoes from sea or land clutter; the characteristics of this clutter are discussed, along with Moving Target Indicator (MTI) and pulse Doppler techniques for mitigating the negative effects of clutter. The course continues with lectures covering the basic principles of target tracking, target parameter estimation and radar imaging and is completed with a discussion of the techniques used to quantitatively test and evaluate radar performance.

Tutorial 2: Micro-Sensor Networks

Monday March 17, 1:00 – 5:00 pm
The Rivera Hotel, Capri Room 102

Organizer:
Sri Kumar, *BAE Systems, Wayne, NJ*

Instructors:
Eric Hoenes and Steve Beck, BAE Systems
"*Micro-Sensor Evolution and Applications"*

Dr. Jeff Paul, DARPA/IXO
"*Networked Embedded Systems and Technology: Progress and Outlook for Future"*

Dr. Akos Ledeci, Vanderbilt University
"*Spatio-Temporal Sensing and Processing"*

Tom Rosenbury, Sperient Inc.
"*Integrated, Low-power Design and Applications"*

This tutorial will review recent progress in micro-sensor network technology, cover applications in the defense and commercial sectors, and review the outlook for the future. We will trace the evolution of the technology through several DARPA programs (such DSN, SensIT, NEST, and others) and through deployments. We will review the state-of-the-art in (a) platform design, (b) networking strategies, (c) in-network spatio-temporal information processing including data and information fusion, detection, classification, tracking, caching, querying, and tasking, of micro-sensor networks. Ultra-low-power communication and processing design techniques, as well as techniques and challenges for design that integrates multiple sensors with processing, communication, computation, and visualization will be presented. Methods for highly scalable and reliable micro-sensor network systems will be outlined. Applications and case studies will include industrial process systems, gun-shot detection and localization, perimeter security, persistent intelligence gathering and surveillance, chemical and biological sensor networks, and ubiquitous computing.

LUNCH SPEAKERS

Lunch will be provided on Tuesday, Wednesday, and Thursday. Both Wednesday's and Thursday's lunches will include presentations of interest to the GOMAC-Tech community. Wednesday's lunch will feature a presentation by LtCol Tom Arnold, USMC, entitled, *"That's Great – but Where Do I Plug In?*

EXHIBITION

An exhibition comprised of commercial vendors exhibiting products of interest to the GOMACTech community is an integral part of the conference. All attendees are reminded to visit the exhibit hall when they have some free time. The Exhibit Hall is located in the hotel's Grand Ballroom A/B. Coffee breaks will be held in the exhibit area when they coincide with the exhibition's hours of operation. On Tuesday evening, an Exhibitors' Reception, sponsored by Northrop Grumman, where attendees can mix in a relaxing atmosphere of food and good spirits, will be held, is scheduled.

Exhibition hours are as follows:

Tuesday, 18 March	12:00 pm – 8:00 pm
Wednesday, 19 March	9:00 am – 4:00 pm

List of Exhibitors (As of December 18)

Aeroflex Colorado Springs
AMI Semiconductor
BAE Systems
Iqonic IC Design
Kansas City Plant
M/A – COM
Maxtek Components Corp.
National Semiconductor Corp.
Northrop Grumman
REMEC Defense & Space, Inc.
Rohm and Haas Electronic Materials
Sandia National Laboratories
Synopsys, Inc.
TriQuint Semiconductor
Trusted Access Program Office

WEDNESDAY EVENING DINNER
LANCE BURTON
MASTER MAGICIAN

The 2008 GOMACTech Wednesday evening social event features a wonderful buffet dinner at the Monte Carlo Hotel & Casino followed by the daring and brilliant skills of Lance Burton, Master Magician. Lance has generated annual specials on NBC. He's been voted Best Magician, Best Entertainer, Best Value, and Best Theatre. Come and see this amazing performance at the Monte Carlo in the beautiful Lance Burton Theatre. Bus transportation will be provided. Buses will leave the Riviera for the Monte Carlo promptly at 4:30 pm after the day's presentations. Tickets should be purchased in advance along with your conference registration. Adults $25, Children (12 and under) $15.

HOTEL ACCOMMODATIONS

The Riviera Hotel and Casino enjoys a legendary past as one of the first top-notch Las Vegas hotels in the State of Nevada, known for its big name entertainment and friendly hospitality, as well as its worldwide name recognition. The historic Riviera is one of the State's premier destination spots offering the passion and excitement of nostalgic Las Vegas and the Rat Pack Era, combined with a modern-day multi-million dollar remodeling of rooms and convention facilities, bringing the property up to par with today's mega-resort competition.

Over 2000 refurbished oversized rooms offer maximum comfort and breathtaking views of the glittering Las Vegas Strip with its western scenic panoramas. Each accommodation has been attractively decorated, including all the important amenities Las Vegas has to offer for both leisure and business travelers.

GOMACTech has reserved a block of rooms at the hotel at a special rate of $116 single or double. These rates are exclusive of Clark County tax (currently 9%).

Reservations may be made by calling the hotel reservations department at 1-800-634-6753.

The deadline for reservations from the GOMACTech block is 25 February 2008.

CONFERENCE CONTACT

Anyone requiring additional information about GOMACTech should contact the Conference Coordinator, Ralph Nadell, GOMACTech, 411 Lafayette Street, Suite 201, New York, NY 10003 (212/460-8090 x203), Rnadell@pcm411.com.

GOMACTech '07 PAPER AWARDS

Paper awards based on audience evaluations from GOMACTech-07 will include the George Abraham Outstanding Paper Award, two Meritorious Paper Awards, and a Best Poster Paper Award. Presentation of these well-deserved awards will be made at the Plenary Session on Tuesday morning in Grande Ballroom C/D. The GOMACTech-07 winners are:

The George Abraham Outstanding Paper Award (21.4)

C. L. Keast, J. Burns, P. Gouker, R. D'Onofrio, A. Soares, P. Wyatt
MIT Lincoln Laboratory, Lexington, MA
"Fully Depleted SOI CMOS Technology for Extreme Environments"

Meritorious Paper Award (31.4)

P. P. Chang-Chien, M. Yajima, C. Cheung, X. Zeng, K. Luo, C. Geiger, D. Eaves, K. Tornquist, J. Uyeda, R. Tsai
Northrop Grumman Space Technology, Redondo Beach, CA
"Multi-Layer MMIC Integration Using Wafer-Scale Assembly"

Meritorious Paper Award (23.2)

L. W. Massengill, O. A. Amusan, S. Dasgupta, A. L. Sternberg, J. D. Black, A. F. Witulski, B. L. Bhuva, M. L. Alles,
Vanderbilt University, Nashville, TN
"Sub-100-nm Radiation-Hardened IC Design: Single-Event Mechanisms Impacting Modeling and Simulation for Design"

Best Poster Paper Award (33.4)

A. Puzella, R. Alm
Raytheon Integrated Defense Systems, Sudbery, MA
"Low-Power-Density Panel Phased Array"

RATING FORM / QUESTIONNAIRE

Don't forget to vote for your favorite presentation this year before you leave the conference. A rating form/questionnaire is being handed out at conference check-in. To encourage submission of these forms, GOMACTech has a special gift for all attendees submitting a completed form. Please turn your form in at the Conference registration desk when you leave the Conference to receive your gift item.

SPEAKERS' PREP ROOM

The Capri Room 103 is designated as a speakers' preparation room and will be available during the hours the conference registration desk is open. Speakers are encouraged to use the Capri 103 facilities to ensure compatibility with the meeting's AV equipment. Speakers having difficulties should request at the conference registration desk to see an AV operator. ***Speakers are also asked to be at their assigned presentation room 30 minutes before the sessions begins to meet with their session chair.*** An AV operator will be assigned to each technical session room.

CD-ROM PROCEEDINGS

The GOMACTech CD-ROM Proceedings, containing searchable, condensed versions of submitted papers presented at the Conference, will be distributed to all registrants. Additional copies of the CD-ROM can be purchased at the Conference at a cost of $40.00 per CD.

Previously published as the GOMAC Digest of Technical Papers, Volumes I – XXVII, this publication is the only record of the conference. Previous GOMAC Digests will, upon request, made available copies to qualified Defense Technical Information Center (DTIC) users. Please call 1-800-225-3842 for bound or microfiche copies. Past Digests can be ordered by calling the above number and identifying the following accession numbers (please note that GOMAC was not held in the calendar year of 1995):

GOMAC-84 B113271	-86 B107186	-87 B119187
-88 B129239	-89 B138550	-90 B150254

-91 B160081	-92 B169396	-93 B177761
-94 B195015	-96 B212362	-97 B222171
-98 B235088	-99 B242763	-00 B254138
-01 B264749	-02 B275146	-03 M201604
-04 M201663	-05 M201849	-06 M202011
-07M202134		

INFORMATION / MESSAGE CENTER

The Information/Message Center will be located adjacent to the GOMACTech Registration Desk. The message center telephone number for incoming calls is 702/734-5110. Callers should ask to be transferred to the GOMACTech Registration Desk.

PARTICIPATING GOVERNMENT ORGANIZATIONS

Participating Government Organizations of GOMACTech-07 include: Department of Defense (Army, Navy, Air Force) ... National Aeronautics and Space Administration ... Department of Commerce (National Institute of Standards and Technology) ... National Security Agency ... Department of Energy (Sandia National Laboratories) ... Defense Logistics Agency ... Department of Health and Human Services ... Defense Threat Reduction Agency ... Advisory Group on Electron Devices ... Defense Advanced Research Projects Agency ... Central Intelligence Agency ... National Reconnaissance Office ...

GOMACTech WEB SITE

Information on GOMACTech may be obtained through its Web site at www.gomactech.net.

TUESDAY, 18 MARCH

Session 1

PLENARY SESSION

Tuesday, 18 March / 8:30 am – 12:00 pm / Grande Ballroom C/D

Opening Remarks **(8:30–8:45)**

Dr. Gerald M. Borsuk, GOMACTech-08 General Chair
Naval Research Laboratory, Washington, DC

GOMACTech-07 Awards **(8:45–9:00)**

Keynote Address **(9:00–10:00)**

Dr. Anthony J. Tether
Director, Defense Advanced Research Projects Agency, Arlington, VA
"The Integrated Microsystem and How It Is Changing the World"

BREAK **(10:00–10:30)**

Jack S. Kilby Lecture Series **(10:30–12:00)**

Dr. Starnes Walker
Director of Research, Department of Homeland Security (S&T), Washington, DC

"Making the Nation Safer: Challenges and Opportunites in Science and Technology"

Dr. William S. Rees, Jr.
Director, Deputy Under Secretary of Defense (Laboratories and Basic Sciences), Washington, DC

"Roles of Basic Research in DoD"

Dr. Andrea Goldsmith
Professor of Electrical Engineering, Stanford University, Stanford, CA
"Co-operation and Cognition in Wireless Sensor Materials"

LUNCH **(12:00–1:30)**

Session 2

NANOSENSOR TECHNOLOGY I

Tuesday, 18 March / 1:30 – 3:00 pm / Grande Ballroom D

Chair: **Cliff Lau**
Institute for Defense Analyses, Alexandria, VA

Co-Chair: **Joe E. Brewer**
University of Florida, Melrose, FL

2.1: **The DoD Nanotechnology for Chemical and Biological Defense 2030 Workshop and Study: Results and Reccommendations** **(1:30)**

M. Kosal
Georgia Institute of Technology, Atlanta, GA

Nanotechnology-based countermeasures, including sensing current and advanced chemical and biological agents and threat scenarios were developed outlining the key science and technology capabilities necessary to achieve those scenarios and strategizing research directions that would enable innovative and revolutionary capabilities were generated by the DoD's Nanotechnology for Chemical and Biological Defense 2030 study.

2.2: **Reagentless Electronic Nanosensors Assembled on a Viral Scaffold** **(2:10)**

A. S. Blum, C. M. Soto, B. R. Ratna
Naval Research Laboratory, Washington, DC

C. D. Wilson,
Geo-Centers, Newton, MA

J. E. Johnson
Scripps Research Institute, La Jolla, CA

Work showing the organization of 5-nm gold nanoparticles at specific interparticle distances, using Cowpea Mosaic Virus as a template, will be presented. The nanoparticles can be interconnected with dithiol molecules, generating nanoscale conductive networks. Network conductance is exquisitely sensitive to the environment, allowing the formation of reagentless electronic nanosensors.

2.3: **Chemical-Sensing System-on-Chip Transmissions** **(2:30)**

J. Chan
APIC, Culver City, CA

Chemical, explosive, and biological sensors have been developed. These sensors, equipped with communications links, are building blocks for the embedded C2 network. A biosensor chip based on silicon-on-insulator (SOI) photonics integrated circuits (PICs), which leads to a low-cost and small-sized biological/chemical agent detection system, has been developed. In addition, APIC is working with PSU in applying a nanofabrication technique to produce a reliable SERS sensor. Sensor systems and a roadmap for further miniaturization will be described. The Navy-funded M3PF, which supports the fabrication of all our photonic sensors and fiber communications network components, will also be described.

BREAK **(3:00)**

Session 3

ULTRA-HIGH-SPEED TRANSISTORS

Tuesday, 18 March / 1:30 – 3:00 pm / Capri 101

Chair: **Mark Rosker**
DARPA/MTO, Arlington, VA

Co-Chair: **Daniel J. Radack**
Institute for Defense Analyses, Alexandria, VA

3.1: From DHBTs with f_T = 670 GHz and PHBTs with f_T = 765 GHz Towards THz Operation of InP HBTs (1:30)

M. Feng, W. Snodgrass
University of Illinois at Urbana-Champaign, Urbana, IL

Vertically scaled InGaAs/InP pseudomorphic HBTs (PHBTs) demonstrate a record f_T = 765 GHz with a collector-emitter breakdown voltage of 1.65 V. Type-II GaAsSb/InP double-HBTs (DHBTs) exhibit an f_T = 670 GHz with a breakdown voltage of 3.2 V. The future of scaling for InP HBTs towards THz cutoff frequencies is explored.

3.2: High-Speed InP HEMT Devices with an f_T = 500 GHz and an f_{max} > 1 THz (1:50)

R. Lai, X.B. Mei
Northrup Grumman Corp., Redondo Beach, CA

T. Gaier, A. Fung
NASA Jet Propulsion Laboratory, Pasadena, CA

The latest advancements of 35-nm InGaAs/InAlAs/InP high-electron-mobility transistor (InP HEMT) devices that have achieved a peak device transconductance at 1 V of 2600 mS/mm, peak device cutoff frequencies as high as 500 GHz, and an extrapolated f_{max} above 1 THz is presented. The f_{max} extrapolation is based on both unilateral gain (1.2 THz) and maximum stable gain/maximum available gain (1.1 THz) extrapolations.

3.3: On the Feasibility of Low-THz InP HBTs (2:10)

M. Rodwell, Z. Griffith, U. Singisetti, M. Wistey, A. C. Gossard
University of California at Santa Barbara, Santa Barbara, CA

E. Lind
Lund University, Lund, Sweden

An InP HBT scaling roadmap, indicating a feasibility of ~1.5-THz devices, is presented. 250-nm emitter-size devices that obtained a record 560-GHz simultaneous f_t and f_{max} will be reported. A record 755-GHz f_{max} has been attained for a device with a thicker collector.

3.4: Low-Power 400-GHz InP DHBT (2:30)

M. Sokolich, T. Hussain, J. C. Li, D. A. Hitko, K. R. Elliott
HRL Laboratories, Malibu, CA

HRL has demonstrated extremely low power (2 mW/HBT) InP HBTs with a cutoff frequency above 400 GHz, enabling full Nyquist digital synthesis of up to 8-GHz signals with 40-dB SFDR at low circuit power dissipation.

BREAK (3:00)

Session 4

ADVANCED PACKAGING FOR RF SYSTEMS

Tuesday, 18 March / 1:30 – 3:00 pm / Capri 102

Chair: **Thomas W. Dalrymple**
AFRL / Sensors Directorate / Aerospace Components Division, Wright-Patterson AFB, OH

Co-Chair: **Tony K. Quach**
AFRL, Wright-Patterson AFB, OH

4.1: Si and GaAs Integration through 3D Packaging (1:30)

W. Mecouch, B. Richards, G. McGuire,
ITC, Raleigh, NC

J. Dishong, H. Clifton, R. Mongia, S. Nelson
REMEC Defense & Space, Richardson, TX

T. Dalrymple
Air Force Research Laboratory, Wright Patterson AFB, OH

An approach for heterogeneous semiconductor material integration and some of the IC designs that this approach enables will be described. The approach allows Si-based control circuits to be packaged above the GaAs amplifier circuits, reducing the total package size. Ring oscillator test structures have been fabricated, and digital amplifier controllers with matching adjustable gain amplifiers have been designed.

4.2: Multi-Chip-Module-Based X-Band Receiver Utilizing Silicon Germanium MMICs (1:50)

R. G. Drangmeister, L. M. Johnson, M. A. Gouker, V. Bolkovsky,
MIT Lincoln Laboratory, Lexington, MA

T. K. Quach, G. L. Creech, P .L. Orlando, A. G. Mattamana,
Air Force Research Laboratory, Dayton, OH

B. K. Kormanyos, R. K. Bonebright
The *Boeing Co., Seattle, WA*

The demonstration of an X-band receiver using MMICs implemented in a 0.18-µm silicon germanium (SiGe) technology mounted on an MCM-D substrate using flip-chip techniques is reported. The MCM-D substrate incorporates embedded resistors, capacitors, and inductors, as well as various SMT components to perform filtering, impedance matching, and power-supply bypassing. Data showing the RF performance of the receiver and the output of an included high-speed A/D converter are presented.

4.3: Performance of Microwave Surface-Mount LCP Packages under Environmental Tests **(2:10)**

A-V. Pham, K. Aihara, M. Chen, C. Chen, E. Zhang
University of California, Davis, Davis, CA

T. W. Dalrymple
Air Force Research Laboratory, Wright-Patterson AFB, OH

The reliability evaluation of surface-mount LCP packages is presented. The LCP packages house MMICs in cavities that are sealed with LCP materials and achieve a fine leak rate of 5 x 10-8 cm3-atm/sec. The electrical results of these packages under 85/85 temperature cycling and other environmental tests will be reported.

4.4: Affordable High-Performance RF Integration Methodology **(2:30)**

J. Iannotti, C. Kapusta, K. Durocher
GE Global Research Center, Niskayuna, NY

B. Taft
Lockheed Martin Commercial Space Systems, | Newtown, PA

A broadband 2-bit Long True Time Delay component has been designed. This component is to be used in large-area apertures in aerospace where C-SWaP is a critical requirement. Design goals include return losses greater than 10 dB, insertion loss variations throughout the time delays within ±1 dB, and a cost reduction of greater than 5x with respect to an RF chip-on-flex integration methodology.

BREAK **(3:00)**

Session 5

NANOSENSOR TECHNOLOGY II

Tuesday, 18 March / 3:30 – 5:00 pm / Grande Ballroom D

Chair: **Cliff Lau**
Institute for Defense Analyses, Alexandria, VA

Co-Chair: **Joe E. Brewer**
University of Florida, Melrose, FL

5.1: A High-Gain Low-Noise Single-Photon Detector for SWIR (3:30)

O. G. Memis, W-W. D. Dey, A. Katsnelson, H. Mohseni
Northwestern University, Evanston, IL

A novel photon detector was developed for SWIR. Stable gain values exceeding 10,000 were demonstrated at room temperature with dark current ranging from 90 nA to 1 μA. The devices did not exhibit any excess noise or after-pulsing and could provide high-frequency operation (250-psec rise time, 14-psec jitter) with some gain-bandwidth tradeoff by passivation.

5.2: Nanotechnology to Enable Abiotic Biological Sensing and Communications (3:50)

M. J. Lesho, J. D. Adam, J. X. Przybysz
Northrop Grumman Corp., Linthicum, MD

Two elements of nanotechnology for sensing and communication that will enable WMD surveillance on demand will be discussed. The first is novel nanomaterials for chem/bio sensing to replace current bio-recognition, and the second is high-linearity low-power electronics for tactical networking capability.

5.3: Integrated Multi-Layer Design of Ad-Hoc Smart Small Sensor Networks (4:10)

M. Peckerar, C-C. Shen, S. Bhattacharyya, N. Goldsman
University of Maryland, College Park, MD

Work in distributed sensor arrays for asymmetric threat detection will be reviewed. This is a system problem. Subsystems must be designed to act together to meet global detection goals. No one element dominates in defining performance.

5.4: Low-Power Wide-Dynamic-Range Carbon-Nanotube Vacuum Gauges (4:30)

A. Kaul, H. Manohara
Jet Propulsion Laboratory, Pasadena, CA

The first reported results of carbon-nanotube (CNT) vacuum gauges that operate at low power (nW–μW) and exhibit a wide dynamic range (760 – 1 x 10^{-6} Torr) will be presented. The ultra-miniatured size of such sensors compared to conventional high-vacuum sensors makes them non-intrusive and easily integratable with other vacuum-encased microdevices and vacuum microtube oscillators and amplifiers.

Session 6

ULTRA-LOW-POWER RF TRANSCEIVERS

Tuesday, 18 March / 3:30 – 5:00 pm / Capri 101

Chair: **Michael Fritze**
DARPA/MTO, Arlington, VA

Co-Chair: **Mark Gouker**
MIT Lincoln Laboratory, Lexington, MA

6.1: Single-Chip Radio-Transceiver Power Reduction (3:30)

K. K. O, J. E. Brewer, J-J. Lin, H-T. Wu, S. Wang
University of Florida, Gainesville, FL

Reduction of power consumption in emerging single-chip radio transceivers is of strong interest for the extension of operating life and/or minimization of battery weight/volume. Approaches for ~5x power reduction in completely self-contained (no off-chip active or passive components) radio devices are proposed.

6.2: Fractional-N Synthesizer Techniques for Low-Power Wireless Sensor Nodes (3:50)

T. M. Hancock, M. Straayer, A. Messier
MIT Lincoln Laboratory, Lexington, MA

Modulation of fractional-N synthesizers is an energy-efficient architecture capable of moderate data rates and is beginning to see use in commercial applications. However, this technique can also be used in defense applications for power-efficient RF and microwave frequency modulation and is well-suited for use in low-power sensor networks.

6.3: An Ultra-low-Power Wakeup Receiver for Wireless Sensor Nodes (4:10)

N. Pletcher, S. Gambini, J. Rabaey
University of California at Berkeley, Berkeley, CA

The use of a wakeup receiver can lead to reduced power consumption and communication latency in wireless sensor networks. However, its power consumption must be extremely low (<100 µW). This paper introduces the wakeup receiver concept, discusses specific design considerations, and presents a fully integrated receiver consuming just 65 µW.

6.4: Miniature Balun Component Demonstration in Advanced Silicon Germanium Technology (4:30)

P. L. Orlando, C. A. Bryant, K. S. Groves, T. L. James
AFRL, Wright-Patterson AFB, OH

Two balun design topologies that enable system-on-chip (SoC) demonstration using 0.18-µm silicon germanium (SiGe) BiCMOS technology is reported. The purpose of these circuits is to explore the feasibility of passive baluns in silicon technology while maintaining low insertion loss, magnitude/phase balance, and proper input/output matching for a 50-Ω system.

Session 7

WIDE-BANDGAP RF SEMICONDUCTORS

Tuesday, 18 March / 3:30 – 5:00 pm / Capri 102

Chair: **Mark Rosker**
DARPA/MTO, Arlington, VA

Co-Chair: **Steven C. Binari**
Naval Research Laboratory, Washington, DC

7.1: **DARPA Wide-Band-Gap Semiconductors for RF Applications (WBGS-RF) Tri-Service Observations** **(3:30)**

G. D. Via, E. Viveiros
Air Force Research Laboratory, Wright-Patterson AFB, OH

S. C. Binari
Naval Research Laboratory, Washington, DC

Phase II of the DARPA WBGS-RF program is drawing to a close. Over the last 3 years, hundreds of processed wafers and fixtured reliability circuits have been delivered to the government for independent evaluation. The Tri-Service Team will present a summary of data collected and analysis performed. Emphasis will be placed on RF performance with respect to program milestones and the status of ongoing reliability assessments.

7.2: **Raytheon–Cree Team DARPA WBGS Phase 2 Program Accomplishments** **(3:50)**

J. Smolko, S. Brierley, K. Smith, M. Chumbes
Raytheon, Tewksbury, MA

J. Milligan, S. Allen, P. Smith
Cree, Durham, NC

The Raytheon–Cree WBGS is accelerating the pace of GaN technology development to align with military and commercial system needs and to reduce insertion risk. Close coordination and open sharing between the two foundries eliminates duplication of development effort and reduces risk against technical hurdles. WBGS Phase 2 program accomplishments against the technical metrics are presented.

7.3: **Q-Band GaN HEMT with Improved Performance and Reliability** **(4:10)**

Y. Chen, M. Wojtowicz, B. Heying, I. Smorchkova, W-B. Luo, W. Sutton, V. Gambin, C. Namba, P-H. Liu, B. Poust
Northrop Grumman Corp., Redondo Beach, CA

Northrop Grumman, under the DARPA WBGS-RF Program, is developing GaN HEMT technology for reliable high-performance power-amplifier applications at Q-band. Progress will be summarized and a record 4-W/mm output power, 8.1-dB gain, and 40% PAE measured from a 0.5-mm GaN HEMT at 40 GHz will be reported.

7.4: GaN HEMT and Wideband Power Module Development (4:30)

A. Balistreri, C. Lee, P. Saunier, J. Jimenez
TriQuint Semiconductor, Richardson, TX

TriQuint Semiconductor and its partners, BAE Systems, Lockheed Martin, IQE-RF, II-VI, Nitronex, MIT, and RPI, are developing gallium nitride devices suitable for wide-band applications for the DARPA Wide Bandgap Semiconductor Technology RF Thrust. The goals of the program are to produce reliable reproducible high-performance devices and demonstrate capabilities through a 100-W 2-20–GHz module. The program encompasses continued improvement in material capabilities, development of device structures and process techniques, design and fabrication of MMICs, and thermal and mechanical design of high-power combiners and modules. The results of the Phase II program and progress toward the MMIC and module milestones of Phase III will be discussed. This program is supported by DARPA and the Army Research Laboratory.

WEDNESDAY, 19 MARCH

Session 8

SPACE-ENVIRONMENT MODELING

Wednesday, 19 March / 8:00 – 9:30 am / Grande Ballroom C

Chair: **Gregory P. Ginet**
AFRL/RVBX, Hanscom AFB, MA
Co-Chair: **Stuart Lee Huston**
Huston Associates, Newport Beach, CA

8.1: AE(P)-9: Next-Generation Radiation Specification Models (8:00)

G. Ginet
Air Force Research Laborotaty, Hanscom AFB, MA

P. O'Brien
Aerospace Corp., Chantilly, VA

A new set of standard radiation-belt models, AE-9 and AP-9, is being developed by a consortium of institutions to replace the current AE-8 and AP-9 models. The architecture, current status, and future plans will be presented.

8.2: Modeling Space Weather Effects Using Nascap-2k (8:30)

M. J. Mandell, V. A. Davis
SAIC, San Diego, CA

A. T. Wheelock, D. L. Cooke
Air Force Research Laboratory, Hanscom AFB, MA

Nascap-2k is an interactive toolkit for studying plasma interactions with spacecraft. The capabilities of the code are illustrated by four examples: geostationary charging, self-consistent potentials for a negative probe in a LEO wake, spacecraft potential in the solar wind, and eclipse exit of a geosynchronous satellite with potential control.

8.3: Solar Proton and Cosmic-Ray Models for Spacecraft Design (8:50)

J. Adams
NASA/MSFC, Huntsville, AL

The current status and future development plans for solar proton and cosmic-ray models used to estimate single-event effects and dose degradation for satellite design will be presented.

8.4: Modeling Artificial Radiation Belts from a High Altitude Nuclear Detonation (9:10)

B. Roth
Applied Research Associates, Santa Barbara, CA

G. Ginet, R. Hilmer
AFRL, Hanscom AFB, MA

The history and available data from the U.S. and USSR high-altitude nuclear tests that produced artificial radiation belts will be reviewed. Two DoD belt-pumping models, SNRTACS and DGBETS, will be compared and their uncertainties, sensitivities, and limitations will be discussed. An example total-dose calculation illustrates the impact on a representative LEO system.

BREAK (9:30)

Session 9

ADVANCED ANALOG/DIGITAL FRONT-END PROCESSORS AND COMPONENTS I

Wednesday, 19 March / 8:00 – 9:30 am / Grande Ballroom D

Chair: **Daniel J. Radack**
Institute for Defense Analyses, Alexandria, VA
Co-Chair: **Mark Rosker**
DARPA/MTO, Arlington, VA

9.1: **Heterogeneous Transistor-Scale Integration of Advanced InP HBT and CMOS Si Technologies for High Performance Mixed Signal Applications** **(8:00)**

A. Gutierrez-Aitken, P. Chang-Chien, B. Oyama, R. Sandhu, K. Tornquist, K. Thai, D. Scott, W. Phan, J. Zhou, P. Nam
Northrop Grumman Space Technology, Redondo Beach, CA

Northrop Grumman Space Technology is developing an Advanced Heterogeneous Integration process for the Compound-Semiconductor-Materials–on–Silicon (COSMOS) DARPA Program. The transistor-scale integration of advanced InP HBT and CMOS will have major impact on many space and defense systems. The technology and progress made to date will be described.

9.2: **Direct Growth of Compound Semiconductors on Silicon** **(8:20)**

K. J. Herrick
Raytheon, Tewksbury, MA

E. Fitzgerald
MIT, Cambridge, MA

A. Liu
IQE, Bethlehem, PA

B. Brar, M. Urteaga
Teledyne, Thousand Oaks, CA

M. Bulsara
Paradigm, Windham, NH

D. Clark
Raytheon, Glenrothes, Scotland

T. Kazior
Raytheon, Andover, MA

This direct growth approach of integrating compound semiconductors (CS) and silicon CMOS is based on a unique silicon template wafer with an embedded CS template layer of germanium (Ge). This unique wafer technology enables placement of CS devices in arbitrary locations on a silicon CMOS wafer for simple high-yield monolithic integration. Further discussion of the approach and initial InP metamorphic HBT device results will be presented.

9.3: Transistor Level Integration of Compound Semiconductor Devices and CMOS (CoSMOS) **(8:40)**

K. Elliott
HRL Laboratories, LLC., Malibu, CA

HRL Laboratories, LLC, is developing technology for intimate integration of CMOS devices with 400-GHz InP HBTs to form complex integrated circuits. By using this approach, dramatic improvement in the linearity, dynamic range, and bandwidth of mixed-signal converter circuits can be obtained with immediate application to advanced systems.

9.4: Printing Approaches to Heterogeneous Integration **(9:00)**

J. A. Rogers
University of Illinois, Urbana, Illinois

Soft transfer elements can be used as stamps in printing-like processes that enable heterogeneous integration of diverse classes of semiconductor devices in two- or three-dimensional layouts. The methods, with several application examples, will be described.

BREAK **(9:30)**

Session 10

AUTONOMOUS SENSOR PLATFORMS

Wednesday, 19 March / 8:00 – 9:30 am / Capri 101

Chair: **David E. Dausch**
RTI International, NC,

Co-Chair: **R. D. delRosario, Jr.**
U.S. Army Research Laboratory, Adelphi, MD

10.1: Family of UGS Demonstration (8:00)

J. Houser
ARL, Adelphi, MD

The U.S. Army Research Laboratory (ARL) has a major laboratory program involving the development of enabling technologies used in unattended ground sensor (UGS) systems. Because of this work, ARL is frequently called upon by the user community to provide technical evaluations and solutions on a wide range of UGS issues. The concept, integration effort, and demonstration details along with initial results will be described. The family of UGS concepts and its benefits for the development, operation, acquisition, and sustainment of UGS will be presented.

10.2: Persistent Communications for Unattended Ground Sensors (UGS) (8:20)

R. Tobin, P. Fisher, C. Karan
Army Research Laboratory, Adelphi, MD

Unattended ground sensors (UGS) are a key system in battlefield situational awareness. A major thrust in the UGS community has been networked sensor systems that allow nodes to collaborate in tracking and identifying a target. The critical UGS problems will be addressed and ARL's solutions to achieve an optimized UGS communications solution will be described.

10.3: Common Sensor Module (8:40)

M. Roberson, D. Strube, J. Swartz, M. Powell, C. Bartee, M. Hunt, K. McGuire|
RTI International, Research Triangle Park, NC

RTI International has used VLF electromagnetic sensing of vehicles to develop an unattended ground sensor capable of identify and classifying vehicles. Work using wavelet signatures and neural networks to achieve better than 80% accuracy in identifying from among 20 vehicles at varying speeds will be reported.

10.4: Electromagnetic Methods of Submerged Marine Communications for Fixed Sensor Networks (9:00)

J. Hodges, M. Rippen
SRI International, St. Petersburg, FL

SRI International's investigation of a critical technology needed to create an underwater sensor network will be documented. It is specifically for sensors in shallow waters for an effective communication mechanism between sensors and communication from the sensor to the backhaul. Current communications technologies are based on the acoustic modem, but state-of-the-art devices leave much to be desired.

BREAK (9:30)

Session 11

EMBEDDED COMMAND AND CONTROL I

Wednesday, 19 March / 8:00 – 9:30 am / Capri 102

Chair: **Deepak Varshneya**
DARPA/STO, Arlington, VA
Co-Chair: **Kathleen A. Griggs**
Puritan Research Corp., Vienna, VA

11.1: Embedded Command and Control for the Soldier (8:00)

J. Kamp
Sage Solutions Group, Centreville, VA

The Army has asserted that every soldier is a sensor. Assuming this end goal, a novel blending of the soldier's tactical sensors with available netted sensors in order to refine situation and relevant local data is being postulated. Such a system would need to update sensor position, fire-fight location, and voice, video, and data communications between soldier sensors. This concept will be described, and some of the notional information exchanges will be discussed. Some hierarchical inferred conditions and situations will be explained, and some of the technical challenges and novel aspects of battle command will be highlighted.

11.2: Robust Surface Navigation (8:20)

S. Tompkins
DARPA, Arlington, VA

Blue force tracking in a GPS-denied situation poses a challenge for small unit operations, particularly when visibility is limited and battlefield chaos is high. Navigation based on signals of opportunity (SoOP), augmented when necessary with lightweight, deployable beacons, offers an alternative to GPS. DARPA's Robust Surface Navigation (RSN) program explores the limits of such an approach. The goal of RSN is a system that adapts seamlessly to any combination of signals, including GPS, beacons, a variety of signals including space and terrestrial communications, commercial broadcast, and navigational signaling systems.

11.3: User Programmability of Embedded Sensor Networks (8:40)

A. Arora
The Ohio State University, Columbus, OH

Collecting a snapshot over a network typically involves communication with every node in the network. This cost impedes a verity of network-centric applications, including situational awareness. A snapshot maintenance system where the communication cost is restricted to O(ln(n)), rather than o(n2), by reducing the fidelity of distant features will be described.

11.4: Distributing Embedded Command and Control Data via the Tactical Component Network (TCN) **(9:00)**

M. M. McMahon, G. J. Hagen
Raytheon Solipsys, Fulton, MD

E. C. Firkin
Raytheon Solipsys, Suffolk, VA

The Tactical Component Network (TCN) provides a collaborative and scalable architecture for exchanging data to create a common track picture. TCN can combine data from multiple ESNs with other sensors and disseminate common tracks. TCN facilitates reachback to command-and-control nodes, cluster management, visualization tools, and ESN data storage.

BREAK **(9:30)**

Session 12

SPACE-ENVIRONMENT MONITORING MISSIONS

Wednesday, 19 March / 10:00 am – 11:30 am / Grande Ballroom C

Chair: **Maj Bill Olson**
USAF/NRO Chantilly, VA

12.1: Observations of the Earth's Radiation Belts: From the Beginning to the Present (10:00)

J. F. Fennell
The Aerospace Corp., Los Angeles, CA

The missions that contributed significant data to the evolving radiation models and understanding of the near-Earth environments will be reviewed. These efforts will be summarized, the spatial regions of interest will be highlighted, and the phenomena and parameters that dominate environment modeling will be described. A discussion on the need for new measurements and better spatial coverage will conclude the presentation.

12.2: NASA's Radiation-Belt Storm Probes: Opportunity in GTO (10:20)

T. P. O'Brien
The Aerospace Corp., Chantilly, VA

In 2012, NASA will launch a science mission, Radiation Belt Storm Probes, into a GTO-like orbit, with low inclination, low altitude perigee, and apogee somewhat below GEO. To many, it is not intuitive that such an observatory could extensively measure radiation hazards.

12.3: Application of Space Environmental Observations to Spacecraft Pre-Launch Engineering and Spacecraft Operations (10:40)

J. L. Barth, M. A. Xapsos
NASA/Goddard, Greenbelt, MD

Efforts to develop and operate "all weather" space systems require robust models of the space environment based on observations of the space environment that are well distributed across several parameters. In addition, the resolution of anomalies requires near-time observations of the local space environment.

12.4: The Inner Magnetosphere: A Near-Earth Sampling of Astrophysical Processes **(11:00)**

J. M. Grebowsky, D. D. Sibeck
NASA Goddard Space Flight Center, Greenbelt, MD

Charged-particle energization and transport are fundamental physical processes occurring in all astrophysical plasmas. Solar flares in the low solar corona, shock waves associated with coronal mass ejections, planetary bow shocks, and the dynamics of charged-particle radiation belts are examples occurring within our heliosphere. The Earth's inner magnetosphere is a unique laboratory for understanding many aspects of these energization and transport processes not only because of their proximity but also because of the plethora of plasma processes that operate (singly and in combination).

LUNCH **(11:30)**

Session 13

ADVANCED ANALOG/DIGITAL FRONT-END PROCESSORS AND COMPONENTS II

Wednesday, 19 March / 10:00 – 11:30 am / Grande Ballroom D

Chair: **Mark Rosker**
DARPA/MTO, Arlington, VA
Co-Chair: **Daniel J. Radack**
Institute for Defense Analyses, Alexandria, VA

13.1: Batch-Fabricated Scalable Millimeter-Wave Electronically Steered Array Transceivers (10:00)

J. Hacker, J. Denatale, C-L. Chen, C. Hillman, B. Brar
Teledyne Scientific Co., Thousand Oaks, CA

M. Rodwell
University of California at Santa Barbara, Santa Barbara, CA

G. Rebeiz
University of California, San Diego, CA

A 44-GHz transceiver-array architecture that integrates all required functionality from silicon digital beam control and rf beam-forming electronics to InP ultra-high-power amplifiers and sensitive receivers, with wide-scan apertures, into a compact, rugged, micromachined three-dimensional structure will be reported.

13.2: Multilayer W-band Transmit Elements for Scalable Millimeter-Wave Arrays (10:20)

R. Tsai, O. Fordham, D-W. Duan, R. Sandhu, X. Zeng, P. Chang-Chien, K. Tornquist, M. Yajima, S. Shih, J. G. Padilla
Northrop Grumman Corp., Redondo Beach, CA

A five-layer 91–95 GHz (W-band) multi-element vertical transmit integrated circuit that incorporates a four-stage gain and power amplifier, 4-bit phase shifter, and a 4-bit serial-to-parallel digital controller, within an ultra-compact 1.28-mm^3 volume (1.6 x 1.6 x 0.5 mm^3), is demonstrated. For the first time, a compact and heterogeneously integrated three-dimensional (3-D) multilayer module is demonstrated with unprecedented millimeter-wave functional density. The attainment of this technology is anticipated to result in enormous improvement of size, weight, performance, and cost of future military systems that operate at millimeter-wave frequencies.

13.3: High-Performance Silicon Phased Arrays for Scalable Millimeter-Wave Array Technology (SMART) (10:40)

G. Rebeiz
University of California at San Diego, La Jolla, CA

The most complex millimeter-wave silicon ICs ever developed, mainly 16-element 44-GHz phased arrays with < 8° of rms phase error and < 0.5 dB of rms amplitude error between the 16 channels will be presented. The silicon IC has a gain of 15 dB and an output power of -3 dBm per channel, consumes only 220 mW per channel, and occupies an area of 2.6 x 3.2 mm. The chip also contains all the necessary digital CMOS electronics for addressing and control.

13.4: Panel-Based Array Technology for Missile Defense Applications **(11:00)**

M. A. Mitchell
Georgia Tech Research Institute, Atlanta, GA

LtCol. A. Novello
MDA, Washington, DC

M. Walder
NRL, Washington, DC

The Missile Defense Agency (MDA) is developing critical technologies for future panel-based phased-array radars. Several challenges to future radar development are addressed by the move to a panel-based architecture from the current T/R module "brick" architecture, most notably affordability and transportability. The development and results to date for two MDA projects are described in detail: SiGe Single-Chip T/R MMIC and SPEAR (Scalable Panels for Efficient, Affordable Radar).

LUNCH **(11:30)**

Session 14

HIGH-EFFICIENCY HIGH-LINEARITY POWER AMPLIFIERS

Wednesday, 19 March / 10:00 – 11:30 am / Capri 101

Chair: **Paul A. Maki**
Office of Naval Research, Arlington, VA

Co-Chair: **Chris W. Hicks**
Naval Air Systems Command, Patuxent River, MD

14.1: 10-W/mm and High-PAE Field-plated GaN Technology for MMW Applications (10:00)

J. Moon, D. Wong, M. Hu, P. Hashimoto, M. Antcliffe, C. McGuire, M. Micovic, P. Willadesen, D. Chow
HRL Laboratories, Malibu, CA

A scaling of field-plated (FP) GaN technology for millimeter-wave frequency operations, where the scaling of FP GaN HEMTs has been done in terms of both lateral and vertical scaling of the HEMT geometry without increasing the gate-to-drain feedback capacitance and impacting its breakdown voltage, is described. A 10-W/mm power density obtained with a high-PAE at Ka-band and a millimeter-wave MMIC will be reported.

14.2: Millimeter-Wave GaN HEMTs with InGaN Back Confinement Barrier (10:20)

Y. Wu, M. Moore, A. Abrahamsen, S. Heikman, M. Jacob-Mitos
Cree Santa Barbara Technology Center, Goleta, CA

A. Burk
Cree, Inc., Durham, NC

Short-channel GaN HEMTs with an InGaN back-confinement barrier showed significantly improved sub-threshold characteristics. With a 0.25-μm-long field plate for enhanced operation voltages up to 60 V, a power density of 13.7 W/mm was obtained at 30 GHz, the highest for a FET at millimeter-wave frequencies. An excellent power-added efficiency up to 54% was also demonstrated at 35 GHz using a smaller field plate of 0.1 μm and a lower bias of 24 V.

14.3: 48-V Broadband GaN HEMTs for Military Applications (10:40)

W. Nagy, R. Therrien, A. Chaudhari, T. Nichols, P. Rajagopal,
Nitronex Corp., Raleigh, NC

Nitronex has developed 48-V unmatched GaN-on-Si power transistors to be used in broadband high-efficiency linear power amplifiers. The power transistors offer 40–120 W of P3 dB power and >12 dB of gain at 3 GHz. The high power density at 48 V and low output capacitance offered by GaN enable the development of high-power unmatched RF power transistors to be used over octaves of bandwidth.

14.4: High-Voltage GaAs pHEMT Technology Provides Next Step in Power Evolution (11:00)

G. Wilcox
TriQuint Semiconductor, Richardson, TX

The benefits of high-voltage GaAs pHEMT technology developed by TriQuint Semiconductor will be discussed and existing products currently available to support DoD applications will be highlighted. With a 60% increase in power density over conventional 0.25-μm pHEMT at X-band and a 100% increase at S-band, HV pHEMT provides the next step in power evolution without deviating from the industry-proven pHEMT technology. With this improvement in power-handling capability, systems can realize near-term cost advantages by designing smaller apertures or increasing power from the existing form factors. Until GaN achieves compete industry acceptance, HV pHEMT is the present solution that will provide the next-level power capability system integrators are asking for.

BREAK (11:30)

Session 15

EMBEDDED COMMAND AND CONTROL II

Wednesday , 19 March / 10:00 – 11:30 am / Capri 102

Chair: **Kathleen A. Griggs**
Puritan Research Corp., Vienna, VA

Co-Chair: **Deepak Varshneya**
DARPA/STO, Arlington, VA

15.1: Shooter Location Sensor Nets (10:00)

J. Bogdanowicz
Raytheon, El Segundo, CA

Under the DARPA IXO Network Embedded System Technology (NEST) program, Raytheon has developed an enhanced network of acoustic micro-sensors to detect and geo-location small-arms-fire based on a systems concept developed by Vanderbilt University. The system exploits muzzle blast as well as shock-wave information captured from a network of acoustic micro-sensors.

15.2: C2 of Embedded Systems Using PacketHop™ (10:20)

J. Hodges, M. Rippen
SRI International, St. Petersburg, Florida

SRI International's investigation of an application for using PacketHop™ in IEEE 802.14 Physical Layer radios in order to form an advanced small-scale communications system to effect command and control in embedded systems will be outlined. The ultimate goal is to provide a low-speed ubiquitous communications framework for swarms of low-cost low-speed ubiquitous sensor nodes.

15.3: Perimeter Sensing Nets (10:40)

E. T. Rosenbury
Sperient, Livermore, CA

Civilian and Government sensors are needed by the millions for anti-terrorist applications such as border control, force protection, container monitoring, and other security applications. Results from advanced sensor network research and development experiments and field tests will be presented, including the performance of wideband wireless radios, advanced sensors, and self-locating electronics. New sensor technologies including a highly miniaturized radar sensor and a heart-beat detector with 100-m stand-off that was recently demonstrated will be described. An analysis of components and technologies for ad-hoc wireless sensors will also be presented.

15.4: Lobster-Eye Stand-Off X-Ray Imager **(11:00)**

M. Gertsenshteyn, V. Grubsky, T. Jannson, G. Savant
Physical Optics Corp., Torrance , CA

Detecting and identifying organic and metallic targets at distances from 50 to 200 m is difficult for hard X-ray detection devices, especially when targets [such as improvised explosive devices (IEDs), a large amount of explosives, and stowaways] are concealed behind metal (steel) and non-metal (plastic, wood, rocks, soil, etc.) walls. At least two problems are inherent to detection at such long distances: (1) a scattering factor proportional to x4 that comes from the divergence of X-rays propagating from a source to a target and X-rays backscattering from a target and (2) the air attenuation of X-rays, which can be significant for standoff distances up to 200 m (400 m total for round trip). The compensation of these factors by novel lobster-eye hard X-ray optics is analyzed in this presentation. The analysis and the optimization of the hard X-ray lobster-eye lens for realistic parameters are also discussed.

LUNCH **(11:30)**

Session 16

COMPONENT RELIABILITY AND CENTERS OF EXCELLENCE

Wednesday, 19 March / 12:45 – 2:15 pm / Grande Ballroom D

Chair: **Chris Bozada**
AFRL/SND, Wright-Patterson AFB, OH
Co-Chair: **Ken Hunt**
AFRL/VSSE, Kirtland AFB, NM

16.1: Nano-Electronics Physics and Chemistry of Failure and Operational Virtual Center of Excellence (12:45)

J. V. Osborn
The Aerospace Corp., Los Angeles, CA

Silicon-based devices with active-element topographies of <100 nm have great potential for future space programs. The Virtual Center of Excellence (VCE) is an Aerospace-Corporation-led pathfinder to address the fundamental physics and chemistry associated with these technologies for space applications. An overview and status of the effort will be presented.

16.2: Physics and Chemistry of Electronics (PACE) Degradation Program (1:05)

D. Dorsey
AFRL, Materials Directorate, Wright-Patterson AFB, OH

PACE is a service-led pathfinder using compound-semiconductor electronics to investigate the utility and shortfalls of physics- and chemistry-based approaches to determine electronic lifetimes as a function of performance and environment for military requirements. Overview and current status of the effort will be presented.

16.3: Delivery of a Classified Rad-Hard–by–Design ASIC Using a Trusted Supply Chain (1:25)

J. Monk, A. Bent
National Semiconductor Corp., Annapolis Junction, MD

R. Van Art, P. Milliken
Aeroflex Colorado Springs, Colorado Springs, CO

By utilizing a trusted supply-chain methodology, Aeroflex Colorado Springs and National Semiconductor were able to manufacture and deliver classified rad-hard ICs for the AEHF program. The technical results of this effort will be discussed and the trusted supply chain methodology will be summarized.

16.4: Addressing Semiconductor Counterfeiting (1:45)

D. Hatano
SIA, San Jose, CA

By addressing semiconductor counterfeiting, the Semiconductor Industry Association, which represents companies responsible for more than 85% of U.S. semiconductor production, established its Anti-Counterfeiting Task Force (ACTF) last year in response to an increase in counterfeit semiconductors. To respond to the problem, the ACTF is working on a number of fronts. An overview of the counterfeit semiconductor problem to the military and other semiconductor consumers will be provided, and the SIA ACTF's activities to address the problem will be reviewed.

BREAK (2:15)

Session 17

CHIP-SCALE AVIONICS

Wednesday, 19 March / 12:45 – 2:15 pm / Capri 101

Chair: **Michael Fritze**
DARPA/STO, Arlington, VA

Co-Chair: **Daniel J. Radack**
Institute for Defense Analyses, Alexandria, VA

17.1: Chip-Scale Avionics System Considerations for Small VTOL UAS (12:45)

D. Enns, A. Touchberry
Honeywell, Minneapolis, MN

Implications for chip-scale avionics on small vertical takeoff and land unmanned aerial vehicle systems for operation in urban terrain are being considered. The mission is to provide reconnaissance, surveillance, and targeting; in particular, hover and stare. Tradeoffs in vehicle capability versus computation and appropriate sensors will be considered. The biggest challenges for small but capable vehicles have to do with size, power, weight, and cost. Two specific system implementations will be considered. The DARPA/Honeywell Micro Air Vehicle (MAV) is a backpackable ducted fan vehicle that can be used by soldiers for reconnaissance and surveillance. This vehicle satisfies the requirements above except for automated obstacle avoidance. The DARPA/Honeywell Organic Air Vehicle-II is a ducted fan vehicle that is larger than the MAV but includes automated obstacle avoidance and capability for targeting as well as reconnaissance and surveillance.

17.2: 3D Integration Technologies and Architectures for Chip-Scale Avionics Applications (1:05)

V. Ozguz
Irvine Sensors Corp., Costa Mesa, CA

An overview of 3-D integration approaches and architectures is presented in relation to very small flying platforms. Systems-level requirements and size, weight, and power constraints are evaluated with respect to current and near-term technology capabilities. Specific challenges resulting from heterogeneous needs of chip-scale avionics and potential biomimetic architectures are highlighted.

17.3: Chip-Scale Silicon Phased Arrays for Millimeter-Wave Applications (1:25)

G. Rebeiz
University of California at San Diego, La Jolla, CA

Several chip-scale phased arrays will be presented, and how this technology can be applied at millimeter-wave frequencies and beyond will be addressed. Also, planar high-efficiency antennas and the transition between the antennas and the phased array will be discussed. Challenges in wafer-scale integration, such as heat removal and antenna efficiency, will also be addressed.

17.4 Opportunities for Reduced State Avionics in Micro Munitions **(1:45)**

P. Plostins
U.S. Army Research Laboratory, Aberdeen Proving Grounds, MD

Current Military Operations in Urban Terrain (MOUT) require U.S. Forces to engage the enemy precisely with low collateral damage. No handheld precision capability currently exists at the squad and platoon level. To achieve this, a new generation of micro-precision munitions are required. Currently, there is no extensive research ongoing in this area. Key enabling technologies have opened the door to the realization of small-scale guided munitions; 40 mm and less.

BREAK **(2:15)**

Session 18

ENABLING TRUSTED MICROCIRCUIT SOLUTIONS

Wednesday, 19 March / 12:45 – 2:15 pm / Capri 102

Chair: **Daniel G. Both**
National Security Agency, Fort George G. Meade, MD
Co-Chair: **John F. Thibeault**
National Security Agency, Fort George G. Meade , MD

18.1: 2012 Long-Term Strategies and Planning (12:45)

D. J. Radack, B. S. Cohen
IDA/ITSD, Alexandria, VA

There are difficult challenges facing the domestic semiconductor industry and the manufacturing landscale may be very different in the next decade. Ensuring that the DoD has access to trustable semicodnuctor technologies requires both short- and long-term strategies and planning. A study on post-2012 manufacturing and a solution path for trust will be discussed.

18.2: Obtaining End-to-End Trust with Accredited Suppliers (1:05)

D. Pentrack
DMEA, McClellan, CA

Criteria for Category 1A trusted design, aggregation, assembly, and test service providers have been finalized. DMEA is now accrediting suppliers for trust in these parts of the supply chain in addition to photomask and semiconductor manufacturers. End-to-end trust is obtained by the proper use of these accredited suppliers.

18.3: Defining MAC1 Components through a Top-Down Approach (1:25)

W. J. Meyers
SAIC, Columbia, MD

Information Systems Security Engineering (ISSE) principals, as they apply to the MAC 1 requirements for a major DoD system, will be addressed. The "Top Down" approach will provide the overall system viewpoint that is necessary to ensure that the MAC 1 requirements “flow down” to the various segments, elements, and components of the system. Examples will be provided of how and where ISSE principles need to be applied so that the appropriate IA measures are made an integral part of the requirements definition process. Real-world experiences will be drawn from the author’s first-hand knowledge of the DoD MILSATCOM Transformational Satellite (TSAT) program.

18.4: Trusted Microcircuit Solutions with IBM's Advanced ASIC Offerings through TAPO (1:45)

E. Hall, G. Mina, J. Turvey, P. Zuchowski, J. Adams, R. Poratti, G. Bogaczyk
IBM, Essex Junction, VT

P. Farrell
IBM, Columbia, MD

J. Magee
IBM, Poughkeepsie, NY

R. Schwarz
IBM, Raleigh, NC

TAPO's relationship with IBM continues to expand advanced technologies available for Trusted microcircuit solutions. IBM's ASIC methodology will be reviewed, along with the foundry flow, to help guide selection of the most appropriate engagement model. IBM's latest advancements in silicon-on-insulator (SOI) including our 45-nm SOI offering will also be reviewed.

BREAK (2:15)

Session 19

SUB-THRESHOLD OPERATION FOR ULTRA-LOW-POWER CIRCUITRY

Wednesday, 19 March / 2:45 – 4:15 pm / Grande Ballroom D

Chair: **Mark Gouker**
MIT Lincoln Laboratory, Lexington, MA
Co Chair: **Craig Keast**
MIT Lincoln Laboratory Lexington, MA

19.1: Process Variation Tolerant Robust Digital Subthreshold Design **(2:45)**

K. Roy, J. Kulkami, M-E. Hwang, A. Raychowdhury, K. Kim
Purdue University, West Lafayette, IN

Process-variation-tolerant circuit techniques for robust digital subthreshold design is proposed. An 8 × 8 process-tolerant FIR filter, working in both superthreshold and subthreshold regions featuring adaptive-ratio modulation and integrated level converters, will be presented. Ultradynamic voltage scaling (UVDS) enables the filter operation at 85 mV, consuming 40 nW. For memory applications, the Schmitt-Trigger-based SRAM bitcell, exhibiting built-in process variation tolerance, is proposed. Functional SRAM with the proposed memory bitcell is demonstrated at 160 mV in 0.13-µm CMOS technology.

19.2: Energy-Driven Circuit Design for Ubiquitous Sensing Applications **(3:05)**

S. Hanson, B. Zhai, D. Blaauw, D. Sylvester
University of Michigan, Ann Arbor, MI

Recent efforts in designing energy-optimal circuits with application to sensor-based systems will be described. The low-energy design space for digital circuits were analyzed and conclusions regarding how such circuits should be designed will be discussed. The models and guidelines described have been successfully used in the design of a robust ultra-low-energy microprocessor and a sub-200-mV 6T SRAM.

19.3: A Comparison of the Energy Efficiency and Throughput Capability of Sub-Threshold Clock-Based and Asynchronous Logic in a 65-nm Process **(3:25)**

T. H. Friddell, J. R. Mackler
The Boeing Co., Phantom Works, Kent, WA

Achievable throughput and energy efficiency for clock-based logic and null convention logic will be compared. It focuses on low-power subthreshold operation in a 65-nm process, illustrating the impact of high-manufacturing variability. How asynchronous logic's adaptability to temperature and process variations makes it more energy efficient will be described.

19.4: A Subthreshold-Optimized FDSOI Technology for Ultra-Low-Power Applications (3:45)

N. Checka, J. Kedzierski, C. Keast
MIT Lincoln Laboratory, Lexington, MA

A large class of circuit applications have stringent requirements on minimizing power consumption. Such systems are termed energy-starved and can accept the speed penalty associated with operating at ultra-low-power levels. To achieve such low power, standard low-power bulk devices are operated in the subthreshold region at voltages below the threshold voltage of the device. Such devices are optimized for "on" or superthreshold operation and thus do not yield the best speed and power performance achievable in the subthreshold region. A device technology optimized for subthreshold operation using a fully depleted silicon-on-insulator (FDSOI) CMOS technology have been developed. This work was sponsored by the Defense Advanced Research Projects Agency under Air Force contract #FA8721-05-C-0002. Opinions, interpretations, conclusions, and recommendations are those of the author and are not necessarily endorsed by the United States Government.

Session 20

WIDE-BANDGAP OXIDE MATERIALS

Wednesday, 19 March / 2:45 – 4:15 pm / Capri 101

Chair: **Michael D. Gerhold**
Army Research Office, Research Triangle Park, NC
Co-Chair: **William D. Palmer**
Army Research Office, Durham, NC

20.1: Epitaxial Growth of ZnO Thin Films and In-Situ Doping by MOCVD (2:45)

M. Pan, J. Nause
Cermet, Inc., Atlanta, GA

ZnO thin films were epitaxial grown by metal-organic chemical-vapor-deposition (MOCVD) technology. Two-step growth was investigated to improve the crystal quality and film morphology. In-situ doping was performed to achieve n^+-ZnO and p-ZnO. UV and visible emissions were observed from ZnO-based lighting devices.

20.2: Development of All-ZnO Heterojunction LEDs (3:05)

A. Osinsky, J. Xie, B. Hertog, P. P. Chow
SVT Associates, Inc., Eden Prairie, MN

J. Mares, W. Schoenfeld
University of Central Florida, Orlando, FL

J. Muth
North Carolina State University, Raleigh, NC

D. Look
Wright State University, Dayton, OH

Recent developments in the growth and fabrication of ZnO-based LEDs with visible-light emission is reported. The characteristics and quality of the grown material are determined by various measurement techniques. The optical and electrical properties of the LEDs are also discussed.

20.3: ZnO Bulk and Epi Growth for Optoelectronic Applications (3:25)

J. Zhang, G. Cantwell, F. X. Xiu, J. J. Song
ZN Technology, Inc., Brea, CA

ZnO substrates, grown by the Seeded Chemical Vapor Transport process, have been developed with high crystallinity, high purity, and low defects for use in homoepitaxy of ZnO-based LEDs and lasers. p- and n-type ZnO layers have been grown by MOCVD and MBE with hole and electron concentrations as high as $1.5 \times 10^{19}/cm^3$ and $1.2 \times 10^{21}/cm^3$, respectively.

20.4: Optical and Electrical Properties of ZnO Surfaces (3:45)

D. C. Look, B. Claflin, Z-Q. Fang
Wright State University, Dayton, OH

Many proposed ZnO devices, *e.g.*, gas sensors, are dependent on surface properties. Temperature-dependent Hall-effect measurements, high-resolution photoluminescence, and Raman-mapping results have been used along with deep-level transient spectroscopy to study the optical and electrical properties of both as-grown and annealed ZnO surfaces.

Session 21

TRUSTED ELECTRONICS RESEARCH

Wednesday, 19 March / 2:45 – 4:15 pm / Capri 102

Chair: **Dean R. Collins**
DARPA/MTO, Arlington, VA

21.1: TRUST in ICs Program Overview (2:45)

D. Collins
DARPA, Arlington, VA

DARPA TRUST in the Integrated Circuit (IC) program is intended to develop technologies that that will enable ICs to be manufactured by an untrusted (potentially off-shore) foundry yet assured be free from tampering. An overview of this new program will be given.

21.2: An Integrated Approach to TRUST in ICs (3:05)

M. Trainoff, J. Chia
Raytheon, El Segundo, CA

DARPA/MTO's TRUST program will develop and integrate multiple disparate technologies to detect and prevent malicious modifications to ICs developed and fabricated outside of trusted hands. This has the potential to save the government billions of dollars and reduce development time for DoD systems by providing access to off-shore commercial products and services. The state-of-the-art for inspection and reverse engineering of ICs will be advanced.

21.3: Metrics for TRUST in Integrated Circuits (3:25)

D. P. Wilt, R. C. Meitzler, J. P. DeVale
John Hopkins University, Applied Physics Laboratory, Laurel, MD

Metrics approaches adapted for the DARPA TRUST in ICs program are reported. A metrics approach initially focused on the detection of malicious alterations in integrated-circuit die has been adapted for use on FPGA bitstreams and the ASIC design process. Metrics for techniques focused on the prevention of malicious alterations will also be discussed.

21.4: FPGA Threat Opportunity Study (3:45)

B. S. Cohen, D. Goldstein, L. Linholm, V. Sharma
Institute for Defense Analyses, Alexandria, VA

Commercially available field-programmable gate arrays (FPGAs) incorporate security features to protect against theft of intellectual property. This study examined a broader set of security concerns and examines the lifecycles of a FPGA for potential vulnerabilities in their use and application for national infrastructure and defense systems.

THURSDAY, 20 MARCH

Session 22

PROGRESS IN 3D IC TECHNOLOGIES

Thursday, 20 March / 8:30 – 10:00 am / Grande Ballroom D

Chair: **Michael Fritze**
DARPA/MTO, Arlington, VA

Co-Chair: **Daniel J. Radack**
Institute for Defense Analyses, Alexandria, VA

22.1: 3D System-in-a-Stack Technologies **(8:30)**

V. Ozguz, J. Yamaguchi
Irvine Sensors Corp., Costa Mesa, CA

P. Franzon
North Carolina State University, Raleigh, NC

L. Schaper
University of Arkansas, Fayetteville, AR

A. Glezer, Y. Joshi
Georgia Institute of Technology, Atlanta, GA

A 3D system-in-a-stack (SiS) technology that enables the implementation of high-performance heterogeneous systems in a greatly reduced form factor, using off-chip in-plane area-array interconnects supporting high tier-to-tier wiring densities without the need to modify the die is described. Any ICs (COTS or ASICs) of differing sizes and fabrication technologies can be used, including packaged components that allows known-good-die-based implementations. System-level issues including thermal-management techniques and embedded passive components are an integral part of the technology.

22.2: Critical Process Technologies in 3D integration **(8:50)**

A. M. Young, D. C. La Tulipe, L. Shi, K-N. Chen, R. Y. Yu, S. J. Koester
IBM, Yorktown Heights, NY

IBM has been developing process technologies to support high-performance 3D integration for both oxide-to-oxide and copper-to-copper wafer-bonding methodologies. Recent key process technology results will be reported in this presentation.

22.3: Monolithic 3D Integrated Circuits **(9:10)**

S. Wong, A. El Gamal, P. Griffin, Y. Nishi, F. Pease, J. Plummer, K. Saraswat
Stanford University, Stanford, CA

As 2D scaling of integrated circuits (ICs) approaches physical and economical limits, 3D ICs offer an attractive alternative to support further integration of functionalities. There are various approaches to realize 3D ICs. A monolithic 3D approach, which offers a high density of device-dimension vertical interconnects, will be focused upon. The performance advantages of such a technology are demonstrated with a 3D FPGA. Technology challenges of monolithic 3-D are discussed.

22.4: Computer-Aided Design and Application Exploration for 3D Integrated Circuits **(9:30)**

P. D. Franzon, W. R. Davis, M. B. Steer
North Carolina State University, Raleigh, NC

S. Sapatnekar
University of Minnesota, Rochester, MN

L. McIlrath
R3Logic, Boston, MA

P. Chadzynski, T. Doxsee, D. Piette, K. Obermiller
PTC, Boston, MA

3D stacking and integration can provide system advantages. Application drivers and computer-aided design (CAD) for 3D ICs will be explored. Interconnect-rich applications especially benefit, sometimes to the equivalent of two technology nodes. Another promising application area is that of logic on memory. Critical issues include thermal management.

BREAK **(10:00)**

Session 23

NOVEL TERAHERTZ TECHNOLOGY

Thursday, March 20 / 8:30 – 10:00 am / Capri 101

Chair: **Dwight Woolard**
Army Research Office, Research Triangle Park, NC

Co-Chair: **Joe E. Brewer**
University of Florida, Melrose, FL

23.1: 639-GHz NEP in a Single-Crystal Semimetal-Semiconductor Schottky-Diode Rectifier **(8:30)**

E. R. Brown, A. C. Young, J. E. Bjarnason, A. C. Gossard, A. C. Gossard
University of California at Santa Barbara, Santa Barbara, CA

H. Kazemi, P. McMarr
Teledyne Scientific, Thousand Oaks, CA

The first experimental results for noise-equivalent power (NEP) of single-crystal ErAs/InGaAlAs zero-bias rectifier diodes in the THz region at room temperature will be reported. At a frequency of 639 GHz, an optical NEP of 3.7×10^{-12} W/Hz$^{1/2}$ is measured with the rectifier coupled quasi-optically to a quasi-plane-wave coherent source. The Johnson-Nyquist-limited electrical NEP of the device is 1.4×10^{-13} W/Hz$^{1/2}$, so there is vast room for improvement through better radiation coupling.

23.2: Data Encoding on THz Signals for Communication and Sensing **(8:50)**

L. Moller, C. Xie, R. C. Giles
Alcatel-Lucent, Crawford Hills, NJ

J. Federici, A. Sinyukov, H-C. Lim
New Jersey Institute of Technology, Newark, NJ

Data modulation of THz signals in the 1-Mbit/sec range will be demonstrated and analyzed. THz pulse trains are phase and amplitude encoded with pseudo-random binary data, transmitted over a short distance and detected. Different modulation formats are generated. From the experimental results, the maximum data rates for an optimized system will be estimated.

23.3: THz Soliton and Plasmonic Science and Technology **(9:10)**

W. Andress, X. Li, D. Ham
Harvard University, Cambridge, MA

Several THz technologies are being developed. The effort takes place in two areas: (1) on-chip electrical soliton oscillators for picosecond-pulse self-generation and (2) characterization and exploitation of plasmonic waves in one-dimensional conductors such as carbon nanotubes and two-dimensional graphene from low THz down to hundreds of GHz.

23.4: Nanometer Silicon MOSFET Detectors of Terahertz and Subterahertz Radiation **(9:30)**

M. Shur
Rensselaer Polytechnic Institute, Troy, NY

High-field electron transport in nanometer-scale silicon MOS is completely different from that in longer-channel devices. An effective electron-field-effect mobility that decreases with gate length and a negative differential mobility in high electric fields are some novel features of such transport that becomes important or even dominant in Si MOS with 32 nm or smaller feature size.

BREAK **(10:00)**

Session 24

RADIATION-HARDENED MICROELECTRONICS TECHNOLOGY DEVELOPMENT AND DEMONSTRATION I

Thursday, 20 March / 8:30 – 10:00 am / Capri 102

Chair: **John Franco**
Defense Threat Reduction Agency, Ft. Belvoir, VA

Co-Chair: **Maj. Jason D. Gooch**
DTRA, Ft. Belvoir, VA

24.1: 90-nm Rad-Hard–by–Design Capabilities and Demonstration (8:30)

W. Snapp, M. Baze, A. Amort, R. Brees, B. Hughloch
The Boeing Co., Seattle, WA

Rad-hard techniques have been implemented in a robust design flow for 90-nm CMOS. Characterization results for RHBD digital logic, SRAM, PLL, and other IP are presented. A multi-core 50-GFLOP processor demonstration design illustrates the application of these elements with chip-level single-event hardening and illustrates the typical penalties incurred in hardening microcircuits.

24.2: A Rad-Hard SONOS 1-Mbit EEPROM for Space Applications (8:50)

D. Adams, M. Fitzpatrick, E. Folk, W. Hand, P. Shea, J. Smith,
Northrop Grumman Corp., Baltimore, MD

J. Sheehy
AMTEC Corp., Huntsville , AL

M. White
Lehigh University, Bethlehem, PA

J. Murray
Sandia National Laboratories, Albuquerque, NM

A rad-hard 1-Mbit (128k x 8) EEPROM for space applications using SONOS (silicon oxide nitride – oxide silicon) technology is described. Based on an extensive 1-Mbit EEPROM memory retention study, a rigorous (100%) screen has been identified that guarantees all products will exceed 10-year memory retention at +125ºC.

24.3: Advanced Rad-Hard SRAM Development and Hardware Test Results (9:10)

S. Doyle
BAE Systems, Manassas, VA

Electrical and radiation test results on a deep-submicron rad- hard 16-Mbit SRAM IC will be presented. The significant technology development and device design challenges will be chronicled from initial SEE modeling to testchip hardware to final electrical characterization and radiation test validation. Model-to-hardware correlation results and model validation will be described. These results pave the way for further sub-100-nm device development.

24.4: Radiation Test Results for a Six-Processor Chip Using IBM's 130-nm 8SF Process **(9:30)**

J. Rooks
AFRL, Rome, NY

D. Alexander
AFRL, Kirtland AFB, NM

L. Weyna
ITT Corp., Rome, NY

Results from total-dose testing and proton testing on a six-processor die that included 12 Mbytes of embedded DRAM are presented. The six-processors run as two triplets. Memory is protected with an error detection and correction code. Output messages have frame check sequences for protection.

BREAK **(10:00)**

Session 25

LOW-PROFILE ANTENNAS USING METAMATERIALS

Thursday, 20 March / 10:30 am – 12:00 pm / Grande Ballroom D

Chair: **Steven Weiss**
Army Research Laboratory, Adelphi, MD
Co-Chair: **Eric D. Adler**
Army Research Laboratory, Adelphi, MD

25.1: Metamaterials: A Look at the Technology from the Army's Aspect **(10:30)**

J. Rock
U.S. Army AMRDEC, Huntsville, AL

An overview of Metamaterials, the evolution of the technology, and a short history of the term “Metamaterial” will be given The areas of interest in Metamaterials at the Aviation and Missile Research, Development, and Engineering Center at the Redstone Arsenal in Huntsville, Alabama, will be discussed. An overview of possible applications in the areas of electromagnetic, acoustic, mechanical, chemical, and electrical as they would apply in a military environment will be presented.

25.2: Embedded-Circuit and Reactive Impedance Surface Metamaterials for Antenna Miniaturization **(10:50)**

K. Sarabandi
The University of Michigan, Ann Arbor, MI

An overview of applications of engineered materials to enhance performance of antennas is provided. Concepts of embedded-circuit metamaterial and reactive impedance meta-substrates for antenna element miniaturization and superdirective arrays are presented.

25.3: Classes of Metamaterial Based Antennas **(11:10)**

A. Lai, T. Itoh
UCLA, Los Angeles, CA

Antennas based on negative-index-type metamaterials developed or being developed will be reviewed. Ultra-compact antennas and leaky wave antennas with unique properties are based on the composite right/left handed (CRLH) transmission structures. Another type of leaky wave antennas is made of dielectric-resonator (DR) based left-handed structures.

25.4: Scalar and Tensor Artificial Impedance Surfaces for Conformal Antennas **(11:30)**

D. Sievenpiper, J. Colburn, B. Fong, J. Ottusch, J. Visher, P. Herz
HRL Laboratories, Malibu, CA

Approaches to realize scalar and tensor artificial impedance surfaces using simple printed metal patterns have been developed. These structures have been fabricated on flat and curved surfaces, and conformal antennas with control over both the radiation pattern and the polarization have been demonstrated.

LUNCH **(12:00)**

Session 26

IDENTIFICATION AND MANIPULATION OF RF ELECTRONICS

Thursday, 20 March / 10:30 am – 12:00 pm / Capri 101

Chair: **Michael B. Steer**
North Carolina State University, Raleigh, NC

Co-Chair: **William D. Palmer**
Army Research Office, Durham, NC

26.1: Exploiting Device-Circuit-Field Interactions in the Time-Frequency Domain (10:30)

M. Steer, G. Mazzaro, J. Wilkerson, K. Gard
North Carolina State University, Raleigh, NC

A. Walker
Vadum, Raleigh, NC

Standoff inverse analysis and manipulation of electronic systems has lead to new concepts of device-circuit-filed interactions. Deep understanding enables the phenomena to be modeled, leading to the design of enhanced exploitation capabilities. Lessons learned in the probing of electronics and the interaction of electronics in electromagnetic environments is presented.

26.2: A Methodology for Tackling the Multi-Scale Spatial and Temporal Complexity of Electromagnetic Interactions in RF Electronic Systems (10:50)

A. Cangellaris
University of Illinois at Urbana-Champaign, Urbana, IL

Comprehensive, computer-aided analysis of electromagnetic interactions in packaged high-frequency electronic systems mounted on their operating platforms is hindered by the multiple spatial scales involved in the development of the discrete model and the multiple time scales necessary for the accurate prediction of the system response. Without a systematic methodology in place for representing in a compact, yet accurate, manner the multi-scale spatial complexity of the model, and without the implementation of efficient numerical integration schemes for tackling the multiple temporal scales involved, predictive numerical analysis of such systems is computationally prohibitive. This presentation will describe a systematic methodology for addressing this computational challenge.

26.3: Characterization of RF Circuits Using Linear Chirp Signals (11:10)

A. F. Martone, E. J. Delp
Purdue University, West Lafayette, IN

A method for the forensic characterization of RF circuits using linear chirp signals is described. When transmitted to an RF device, the linear chirp signal is affected by non-linear circuit components. The non-linear components cause harmonic distortion to the input signal. Features of the harmonic distortion are used to construct a device fingerprint. The fingerprint is then used to characterize the device so that it can be identified from other RF devices.

26.4: Time-Frequency Characterization of Nonlinear Phase and Amplitude Distortion in RF Front-End Circuits **(11:30)**

K. G. Gard, J. Hu, M. B. Steer
North Carolina State University, Raleigh, NC

A time-frequency perspective on the measurement and characterization of frequency-dependent intermodulation distortion generated in RF front-end circuits is presented. Front-end circuits exhibit unique phase and amplitude intermodulation responses when modulated RF signals are applied. Recovery of the phase and amplitude intermodulation distortion information from measurements is important in determining what non-linear and linear circuits are eliciting the measured response; however, this requires a high-dynamic-range comparison of the input and output signals using cross-correlation techniques.

LUNCH **(12:00)**

Session 27

RADIATION-HARDENED MICROELECTRONICS TECHNOLOGY DEVELOPMENT AND DEMONSTRATION II

Thursday, 20 March / 10:30 am – 12:00 pm / Capri 102

Chair: **John Franco**
Defense Threat Reduction Agency, Ft. Belvoir, VA

Co-Chair: **Maj. Jason D. Gooch**
DTRA, Ft. Belvoir, VA

27.1: Radiation Testing, Characterization and Qualification Challeges for Modern Microelectronics and Photonics Devices and Technologies **(10:30)**

K. LaBel
NASA, Greenbelt, MD

The objective of this paper is to discuss the various issues associated with radiation testing, characteriazation, and qualification of advanced microelectronics and photonic semiconductor technologies for use in high-reliability space and missile systems that must operated in radiation environments.

27.2: The Path and Challenges to 90-nm Rad-Hard Technology **(10:50)**

N. Haddad, E. Chan, S. Doyle, R. Lawrence
BAE Systems, Manassas, VA

A rad-hard 90-nm CMOS technology offers a substantial advantage over today's capability in terms of density, power, and performance. Achieving the hardness objectives, however, will not be without significant challenges, especially in the area of single-event-effects hardening. The effort to evaluate a commercial 90-nm CMOS technology and investigate hardening approaches will be discussed.

27.3: Multiple Bit Upsets and Error Mitigation in Ultra Deep Submicron SRAMs **(11:10)**

D. Mavis, P. Eaton, M. Sibley, E. Smith, K. Avery
Micro-RDC, Albuquerque, NM

R. LaCoe
Aerospace Corp., El Segundo, CA

Recent MBU cross-section measurements in nano-scale SRAM designs indicate that 12-transistor SRAM cell designs will loose effectiveness in mitigating heavy-ion-induced errors. The dominance of the MBU cross section dictates the use of specialized EDAC techniques employing block-based architectures with widely separated critical nodes.

27.4: Mixed-Mode Modeling of Radiation Effects with Nuclear Reactions in Nanoscale Electronics **(11:30)**

M. Turowski, A. Fedoseyev, A. Raman,
CFD Research Corp., Huntsville, AL

K. M. Warren, M. L. Alles
Vanderbilt University, Nashville, TN

The new CFDRC mixed-mode simulator which combines 3D TCAD device models and advanced compact transistors models is described. Key features include an interface and adaptive meshing to allow simulations of single-event radiation effects with nuclear reactions and secondary particles computed by Vanderbilt's MRED/Geant4 tools.

LUNCH **(12:00)**

Session 28

POWER ELECTRONICS I

Thursday, 20 March / 1:30 – 3:00 pm / Grande Ballroom D

Chair: **Fritz Kub**
Naval Research Laboratory, Washington , DC
Co-Chair: **Allen Hefner**
NIST, Gaithersburg, MD

28.1: SiC Power Device Technology for High Power Electronics Applications **(1:30)**

D. Grider, A. Agarwal, J. Palmour
Cree, Inc., Durham, NC

Recent rapid advances in SiC power devices technologies and their impact on next-generation high-power electronics applications will be reviewed. These SiC power device technologies, which are capable of operation up to 10 kV and higher, include DMOSFETs and IGBTs, as well as JBS and PiN diodes.

28.2: Silicon Carbide DMOSFETs for Advanced Power Systems at 13.8 kV **(1:50)**

R. S. Howell, S. Buchoff, S. Van Campen, T. McNutt, H. Hearne, B. Nechay, M. Sherwin
Northrop Grumman Corp., Linthicum, MD

R. Singh
GeneSiC Semiconductor, Inc., South Riding, VA

The successful demonstration of 10-kV SiC MOSFETs with die sizes up to 1 cm^2 and 5–50 A of on-current is reported. These MOSFETs demonstrate excellent, stable subthreshold characteristics as a function of operating temperature (200°C) and are excellent candidates for use in 13.8-kV solid-state power substations.

28.3: 1200-V 50-A Silicon Carbide Vertical Junction Field-Effect Transistors for Power Switching Applications **(2:10)**

V. Veliadis, T. McNutt, M. McCoy, H. Hearne
Northrop Grumman Corp., Linthicum, MD

1200-V and low-voltage SiC VJFETs of 0.19 and 0.15 cm^2 areas were manufactured with no epitaxial regrowth, a single ion-implantation event, and seven photolithographic levels. The VJFETs were connected to form normally off cascode switches, which output 34 A at a voltage drop of 4 V.

28.4: 600- and 1200-kV SiC VJFET Technology for High-Power and High-Temperature (300°C) Switching Applications **(2:30)**

D. C. Sheridan, I. Sankin, M. S. Mazzola, L. Cheng, J. B. Casady
SemiSouth Laboratories, Inc., Starkville, MS

J. D. Scofield
AFRL, Wright-Patterson AFB, OH

A high-power and high-temperature-capable 600- and 1200-V SiC VJFET technology which is suitable for demanding military and aerospace power applications has been developed. Both normally off and normally on VJFET devices with low-specific on-resistance are shown to be fully scalable and easily paralleled to enable state-of-the-art multi-kW power modules.

BREAK **(3:00)**

Session 29

ELECTRONICS FOR EXTREME ENVIRONMENTS

Thursday, 20 March / 1:30 – 3:00 pm / Capri 101

Chair: **Elizabeth A. Kolawa**
Jet Propulsion Laboratory, Pasadena, CA

Co-Chair: **Mohammad M Mojarradi**
Jet Propulsion Laboratory, Pasadena, CA

29.1: Extreme-Temperature Invariant Circuitry through Adaptive dc Body Biasing (1:30)

W. S. Pitts, J. Damiano, P. D. Franzon
North Carolina State University, Raleigh, NC

V. Devasthali
North Carolina State University, Raleigh, NC

The design, modeling, and simulation of extreme-environment analog circuits for distributed electronics will be discussed. A quadrature 435-MHz voltage-controlled oscillator was used as the test element for a temperature range from -250 to +200ºC in CMOS partially depleted silicon-on-insulator technology. The room-temperature VCO was tuned into operation for extreme environments using the body node, a fourth transistor terminal, and a voltage source to apply a dc "correction" bias which negated these extreme temperature effects.

29.2: High-Temperature (300°C) SOI/SiC Based DC/DC Converter (1:50)

B. A. Reese, B. McPherson, R. Shaw, J. Hornberger, R. M. Schupbach, A. B. Lostetter
APEI, Inc., Fayetteville, AK

A suite of high-temperature (300°C) dc/dc converters developed using silicon carbide (SiC) power devices (*i.e.*, power switches and diodes) and high-temperature HTMOS devices will be presented.

29.3: Vacuum Microelectronics and Miniature Instruments Based on Application-Specific Electrode-Integrated Nanotube Cathodes (ASINCs) (2:10)

H. Manohara, M. J. Bronikowski, R. Toda, E. Urgiles, M. Mojarradi
Jet Propulsion Laboratory, Pasadena, CA

JPL has developed high-performance cold cathodes using arrays of carbon-nanotube bundles that routinely produce > 15 A/cm^2 at applied fields of 5–8 V/µm. Results of monolithic electrode-integration vacuum packaging that employs solder reflow process and performance as vacuum electronics and electron source components for various applications will be presented.

29.4: MEMS Ohmic Latching Relay **(2:30)**

D. A. Czaplewski, M. S. Baker, C. D. Nordquist, K. R. Pohl, G. M. Kraus
Sandia National Laboratories, Albuquerque, NM

A microelectromechanical systems (MEMS) latching relay that operates at low voltage (< 5 V), during shock events (>7000 g), and during extreme radiation doses (100 Mrad/sec) have been developed. Stable contact resistance through similar relays for greater than 1 x 109 cycles have been measured.

BREAK **(3:00)**

Session 30

POWER ELECTRONICS II

Thursday, 20 March / 3:30 – 5:00 pm / Grande Ballroom D

Chair: **Fritz Kub**
Naval Research Laboratory, Washington, DC

Co-Chair: **Allen Hefner**
NIST Gaithersburg, MD

30.1: High-Voltage AlGaN/GaN HFETs for Power Switching Applications (3:30)

N. Tipirneni, V. Adivarahan, Y. Deng, A. Khan
University of South Carolina, Columbia, SC

A 1600-V 3.4-m Ω-cm^2 AlGaN/GaN HFET immersed in fluorinert liquid and 900-V 2.43-mΩ-cm^2 SiO_2-encapsulated AlGaN/GaN HFETs for power-switching applications will be reported. The approaches to suppressing surface flashover in HFETs by using solid encapsulation materials as well as the approach to reducing current collapse will be presented.

30.2: Overview of Pulsed-Power Research at the Army Research Laboratory (3:50)

H. O'Brien, C. J. Scozzie, S. B. Bayne
Army Research Laboratory, Adelphi, MD

W. Shaheen
Berkeley Research, Beltsville, MD

In the area of pulsed power, the Army Research Laboratory (ARL) is involved in evaluating and contributing to the design of high-power components intended for Army survivability and lethality applications. Devices under study include silicon Super-GTOs, silicon carbide p-i-n diodes and GTOs, and high-energy-density capacitors.

30.3: SiC-Based Power Electronics Research at ORNL (4:10)

B. Ozpineci, M. Chinthavali
ORNL, Knoxville, TN

L. Tolbert, H. Zhang
The University of Tennessee, Knoxville, TN

The characterization of several different SiC devices (Schottky diodes, JFETs, MOSFETs) and their behavior models will be presented. The static and dynamic behavior of the devices will be analyzed to extract device parameters to simulate their impact on system performance. A 55-kW hybrid (Si IGBT SiC Schottky diode) inverter system will be used to validate the simulation results.

30.4: Performance Analysis of 10-kV 100-A SiC Half-Bridge Power Modules (4:30)

A. Hefner
NIST, Gaithersburg, MD

R. Raju
GE Global Research, Niskayuna, NY

The DARPA Wide Bandgap Semiconductor Technology, High Power Electronics program is developing SiC device and module package technology to meet specific program objectives for a 13.8-kV 2.7-MVA solid-state power substation as well as other applications benefiting from this transformational technology. The performance of modules made using these new technologies will be evaluated for their electrical and thermal performance in switch-mode power-conversion applications. Electro-thermal simulations using validated physics-based models for the SiC device and package technologies will also be used to demonstrate expected performance in representative power-converter circuit topologies.

Session 31

COMMMUNICATIONS ARCHITECTURE AND ELECTRONICS ISSUES FOR CONDITION BASED MAINTENANCE

Thursday, March 20 / 3:30 – 5:00 pm / Capri 101

Chair: **Mou-Hsiung (Harry) Chang**
U.S. Army Research Office, Raleigh, NC
Co-Chair: **Paul M. Amirtharaj**
U.S. Army Research Laboratory, Adelphi, MD

31.1: Real-Time Solder-Joint Fault Detectors for Use in a Condition-Based Maintenance (3:30)

J. P. Hofmeister, J. Judkins, E. Ortiz
Ridgetop Group, Tucson, AZ

P. Lall, D. Panchagade
CAVE, Auburn University, Auburn, AL

T. A. Tracy
Raytheon Missile Systems, Tucson, AZ

N. Roth
Daimler, Sindelfingen, Germany

Soldier-Joint BIST and Monitor are new methods for detecting faults in the solder-joint networks of field-programmable gate arrays (FPGAs) for use in condition-based maintenance.

31.2: Nostra: Power System Condition Monitoring and Prognostics (3:50)

B. Adams, C. Vogt
iRobot, Burlington, MA

N. Roy
MIT, Cambridge, MA

The Nostra project aims to predict battery failures for the iRobot PackBot unmanned ground vehicle (UGV). A dynamic Bayes network, built from a combination of domain expertise and data from long-term experiments, combined with real-time data, provides the basis for inference about potential failures.

31.3: Support Vector Machines for Health Monitoring and Prognostics on an Avionics System Application (4:10)

V. A. Sotiris, M. Torres, M. Pecht
University of Maryland, College Park, MD

The use of support-vector machines (SVMs) to detect and predict the health of multivariate systems based on training data representative of healthy operating conditions will be discussed. A novel approach to SV classification (SVC) and regression (SVR) through the use of a principal component projection pursuit is also investigated.

31.4: Data-Driven Prognostics and Condition Monitoring of On-board Electronics (4:30)

M. Azam, S. Ghoshal
Qualtech Systems, Inc., Wethersfield, CT

S. Kumar, V. Sotiris, M. Pecht
University of Maryland, College Park, MD

Complexity of modern electronic systems poses formidable challenges in predicting, tracking, and identifying the trends and sources of degradations and failures in them. To prevent proliferation of technology, manufacturers and designers closely guard the analytical models of electronic systems, which add to the difficulty in fault diagnostics and prognostics (FDP). Absence of analytical models leaves data-driven techniques as the only viable means for FDP in such systems. In this work, we pursue a data-driven approach for health-condition monitoring and forecasting in complex onboard electronic systems.

GENERAL POSTER SESSION

Thursday, 20 March / 9:00 am – 12:00 pm / Grande Ballroom A/B

Chair: **Chris W. Hicks**
Naval Air Systems Command, Patuxent River, MD

32.1: Long-Term Degradation Mechanisms in AlGaN/GaN HFETs

M. Shur, A. Koudymov
Rensselaer Polytechnic Institute, Troy, NY

K. Chu, P. C. Chao
BAE Systems, Nashua, NH

J. Jimenez, T. Balistreri
TriQuint Semiconductor, Dallas, TX

The AlGaN/GaN performance stability model that includes all relevant degradation mechanisms will be presented. The model (validated using our experimental stability data) is based on analytical solution of the current continuity and Poisson equations for the device active region and ungated spacings, and therefore accurately accounts for possible design related and material-defect-based non-ideal effects.

32.2: Steady-State Evaluation of SiC Bipolar Devices for High-Temperature Power-Electronics Application

A. Ogunniyi, S. Kaplan, R. Green, T. Griffin, G. Koebke, M. Morgenstern
Army Research Laboratory, Adelphi, MD

Static characteristics of a 4H-SiC BJT at high temperature is reported. The experimental data show that SiC BJT exhibits positive on-resistance temperature coefficients and negative temperature coefficient. Results show that although gain degradation is still an issue with SiC BJT, improvements to the overall gain performance as a function of temperature has been made based on previous work that have been reported.

32.3: Enabling Derivative Analog and Mixed Signal Technologies in IBM's Trusted Foundry

B. M. Dufrene, J. Dunn, S. Mellinger, L. Nelson, B. Wong
IBM, Essex Junction, VT

IBM's Trusted Foundry will present the current status on emerging derivative technologies in its 200-mm Burlington facility. IBM expands its portfolio of analog and mixed-signal offerings with the addition of CMOS 7RF silicon-on-insulator (SOI) SiGe BiCMOS 5PAe with through-silicon via technology and CMOS8RF with non-volatile memory (NVRAM).

32.4: Trusted ASIC Design: A Case Study – 2

C. L. Lizzo, P. A. Labrie, G. T. Griffin, J. F. Weiland
Abraxas Corp., McLean, VA

DoD and Abraxas Corp. (which acquired Intrinsix Federal Systems) jointly designed and developed the first test-case ASIC to use the IBM Trusted Design Center. The test case was a prototype for an ultra-high-speed communications device. The experience of interfacing with the IBM Trusted Design Center and Trusted Foundry, including ASIC design flows, division of responsibilities, tools/training required, and a general overview of the ASIC will be described.

32.5: Extremely High-Permittivity Materials for Capacitors

J. Talvacchio, T. T. Braggins, D. J. Knuteson, J. M. Murduck, S. Gurkovich, A. E. Berghmans, M. E. Sherwin, N. B. Singh, R. C. Clarke, J. D. Adam
Northrop Grumman Corp., Baltimore, MD

The large and temperature-independent permittivity of Ca-Cu-Ti-O (CCTO) with a relative dielectric constant as large as 100,000 is the key to potential reductions in size and weight for pulsed-power circuits. Record-high energy densities have been demonstrated in low-voltage CCTO thin-film capacitors and high-voltage CCTO tape-cast ceramic capacitors.

32.6: Fabrication and Characterization of GaN HEMTs on 100-mm-Diameter Semi-Insulating SiC Substrates

T. Anderson, A. Gupta, A. Souzis, M. Yoganathan, I. Zwieback
II-VI Wide Bandgap Materials, Pine Brook, NJ

I. Eliashevich, S. Guo
IQE-RF, Somerset, NJ

High-electron-mobility transistors (HEMTs) are being developed on 100-mm semi-insulating SiC substrates in collaboration between II-VI Inc. (SiC substrate growth and fabrication), IQE-RF (epitaxial growth of GaN-based structures), and AFRL Sensors Directorate (HEMT fabrication and testing). Material and device characterization data will be presented and analyzed.

32.7: High-Q Quartz Microfabricated Resonators for Inertial Sensing

R. L. Kubena, R. J. Joyce, D. T. Chang, P. R. Patterson, F. P. Stratton
HRL Laboratories, Malibu, CA

A. D. Challoner
Boeing Satellite Development Center, El Segundo, CA

R. T. McCloskey, D. Kim
UCLA, Los Angeles, CA

High-performance Coriolis-based inertial sensors require high-Q resonators for obtaining low-bias drift operation for a given precision of the manufacturing process. It has been shown that a MEMS quartz disk resonator can provide Q's beyond the state of the art for microsensors.

32.8: Commercial MMIC Packaging Options for High-Performance Military Products

J. Beall , B. Velsher, G. Brehm, K. Decker, D. Drury, L. Giacoma, D. White, J. Baldwin
TriQuint Semiconductor, Richardson, TX

High-performance GaAs MMICs are being packaged in a variety of different package types for commercial telecommunication infrastructure requiring high reliability and 100% RF test at the package level. These packaging approaches should provide practical alternatives for military systems.

32.9: Five-Level MEMS Technology with Integrated n-MOS Electronics

P. J. Resnick, M. Okandan, B. L. Draper, W. D. Cowan
Sandia National Laboratories, Albuquerque, NM

The Sandia SUMMiT technology is a five-layer planarized silicon surface micromachining process for fabricating microelectromechanical systems (MEMS). A simple modification of the SUMMiT process flow allows for simultaneous fabrication of n-MOS devices that can be used for applications such as digital switching and on-chip charge amplification.

32.10: A Quantum-Accurate Two-Loop Data Converter

Q. P. Herr, D. L. Miller, A. A. Pesetski, J. X. Przybysz
Northrop Grumman Corp., Baltimore, MD

A superconducting two-loop delta-sigma ADC modulator with a quantum accurate feedback is reported. At 5-GHz sampling, an SNDR of 81 dB with 10-MHz BW and a TOI of +27 dBsat was measured. Noise shaping in this initial demonstration agrees perfectly with our analytic model. A redesign is consistent with 20 years beyond the state of the art.

32.11: Multi-Layer Micro-Coaxial Phased Arrays

D. Filipovic, S. Rondineaur, M. Lukic
University of Colorado, Boulder, CO

G. Potvin, D. Fontaine
BAE Systems, Nashua, NH

C. Nichols, J-M. Rollin, D. Sherrer
Rohm and Haas, Blacksburg, VA

E. Adler
Army Research Laboratory, Adelphi, MD

J. Evans
DARPA, Arlington, VA

Micromachined components constituting of new multi-layered integrated Ka-band phased arrays were designed and demonstrated. Eleven-strata two-level rectangular coaxial lines, Wilkinson and Gysel power dividers and power combining networks, wide-band cavity-backed slotted patch antennas, and various interconnects including the delay lines were processed and hybridly integrated in a final brick-type phased array.

32.12: Energy-Efficient Pulsed-UWB Transceiver for Insect Light Control

D. C. Daly, M. Bhardwaj, P. P. Mercier, J. Voldman, A. P. Chandrakasan
MIT, Cambridge, MA

F. S. Lee
Rambus, Los Altos, CA

D. D. Wenztloff
University of Michigan, Ann Arbor, MI

Hybrid-insect research is aimed at developing tightly coupled machine–insect interfaces by placing electronic and micromechanical systems on and within insects. A highly integrated low-power ultra-wide-band transceiver chipset suitable for a hybrid-insect flight-control system using moths will be discussed.

32.13: Three-Dimensional Integration Technology for Advanced Focal Planes

C. Keast, B. Aull, J. Burns, C. Chen, J. Knecht, K. Warner, B. Wheeler, V. Suntharalingam, P. Wyatt, D. Yost
MIT Lincoln Laboratory, Lexington, MA

Over the last several years, MIT Lincoln Laboratory (MITLL) has developed a three-dimensional (3-D) circuit-integration technology that exploits the advantages of silicon-on-insulator (SOI) technology to enable wafer-level stacking and micrometer-scale electrical interconnection of fully fabricated circuit wafers. Some of the application areas where this technology has been applied along with their results will be described.

RAD-HARD POSTER SESSION

Thursday, 20 March / 9:00 am – 12:00 pm / Grande Ballroom A/B

Chair: **Chris W. Hicks**
Naval Air Systems Command, Patuxent River, MD

33.1: Analog and Mixed-Signal Libraries In 150-nm Rad-Hard Semiconductor Technologies

D. Hogue, J. Clement, J. Braatz, J. Killens, J. Tostenrude, Z. Johnson
The *Boeing Co., Seattle, WA*

Under the Defense Threat Reduction Agency Radiation Hardened Microelectronics program, Boeing Solid State Electronics Development (SSED), in conjunction with the University of Idaho and the University of Tennessee, has developed rad-hard ultra-deep-submicron mixed-signal mixed-voltage low-power libraries for advanced hardened processes. The library is comprised of functions that are ubiquitous in rad-hard systems for strategic and space applications. Each of the 42 functions in the libraries has been designed, built, and tested. Functions include voltage references, ADC, DAC, comparators, and opamps. These cells were developed using the EDA environment for rad-hard integrated-circuit design that was created by SSED, resulting in IP that enables SOC development for radiation environments. This paper covers all the aspects of the libraries, including the CMOS technology, the hardening techniques used, the EDA environment, the testing, and the applications.

33.2: RHBD Sequential Logic SEU Error Rates in Space Are Limited by Ions Incident at Grazing Angles

B. Hughlock, M. Baze
The *Boeing Co., Kent, WA*

K. Warren
Vanderbilt University, Kent, WA

SEU RHBD techniques have greatly reduced SEU rates in space applications. The dominant remaining SER contribution is due to ions incident at grazing angles to the surface of the device. This limits the applicability of DICE latches and places minimum spacing limitations on TMR and increases EDAC-protected SRAM refresh rates.

33.3: An Investigation of Leakage Mechanisms in Commercial 90-nm Technology with Implications for Hardend-by-Design

M. Sibley, P. Eaton, E. Smith, K. Avery, D. Mavis
Micro-RDC, Albuquerque, NM

Several surprising TID results relating to RHBD layout techniques were discovered. The RHBD techniques previously used in older technologies were able to prevent adverse effects of circuit operation at 2000 krad(Si). Recent experiments have shown that different layout techniques will have to be implemented to mitigate TID effects.

33.4: Characterization of a 130-nm Library for Electrical Performance and Radiation Effects

**M. Lahey, H. Gardner, C. Hafer,
D. Harris, A. Jordan,**
Aeroflex Colorado Springs, Colorado Springs, CO

M. Johnson
NASA GSFC, Greenbelt, MD

As CMOS technologies shrink, characterization of integrated-circuit performance as a function of temperature, voltage, TID, and SEE is necessary for aerospace applications. As part of a three-phase program funded by NASA GSFC, data collected from both a digital cell library and discrete devices fabricated in a 130-nm process will be presented.

33.5: Ultra-High-Speed Radiation-Tolerant Ternary SERDES for Intra-System Communications

**V. Katzman, V. Bratov, S. Woyciehowsky, J. Binkley,
A. Bratov, A. Gryunshpan**
ADSANTEC, Rancho Palos Verdes, CA

G. Rakow
NASA, Greenbelt, MD

J. Lyke
Air Force Research Laboratory, Kirtland AFB, NM

C. Tabbert
Jazz Semiconductors, Irvine, CA

A novel serial interconnect technique based on the utilization of overhead synchro pulses for easy clock recovery without special data encoding, which provides low-power and high-speed bit-transparent operation, will be presented. The rad-hard implementation of transmitters and receivers in a SiGe BiCMOS technology is ideally suitable for space electronics.

33.6: Carbon Nanotubes (CNTs) Based Devices for Space Applications

**J. W. Ward, G. Derderian, Q. Ngo,
M. Hornbeck, A. Robinson, D. Brock, J. Egerton**
Nantero, Manassas, VA

C. Bertin, R. Smith, B. Segal
Nantero, Woburn, MA

Carbon-nanotube (CNT) fabric-based molecular micro-switches (MMS) for space and other extreme radiation environments are being developed. The current status with respect to technology development and RAD capabilities will be presented.

33.7: Accurate Modeling of Single-Event Multiple Upsets in BiSER Protected Logic Circuits in 90-nm Technology

K. Lilja, A. Azarenok
Robust Chip, Inc., Pleasanton , CA

P. Relangi, S. Mitra
Stanford University, Palo Alto, CA

By using a new modeling technique, which allows for a detailed, accurate simulation of single-event charge collection, including multiple-node collection, it was shown that a BiSER protected latch, with appropriate layout, cannot be upset by a vertical single-event impact, and LET limits for various special events (such as grazing angle directions) which can generate a latch upset will be discussed. The accuracy and capacity of the modeling technique is also discussed.

33.8: Analog Design Technique for SET-Tolerant RHBD PLL and VCO

M. Denham
Micro-RDC, Bend, OR

Frequency-Synthesis Ring-Oscillator PLL circuits provide the "heartbeat" of nanoscale ICs. A SET event in the voltage-controlled oscillator (VCO) can stall the PLL with possible catastrophic effects. An analog rad-hard–by–design technique is presented which mitigates VCO SET effects and has general mixed-signal applicability. Simulation, modeling, and test-chip data will be presented.

33.9: Space Instrument for High-Accuracy Total-Ionizing-Dose Measurements

J. A. Nelson, M. Campola, H. J. Barnaby
Arizona State University, Tempe, AZ

E. R. Long
Longhill Technologies, Inc., Waynesboro, VA

A board-level experiment, capable of characterizing the effectiveness of a new shielding technology for electronic components in the space-radiation environment, was designed, assembled, and tested. The experiment measures the degradation of p-channel MOSFET dosimeters as a function of shielding thickness, bias current, and temperature.

STUDENT POSTER SESSION

Thursday, 20 March / 9:00 am – 12:00 pm / Grande Ballroom A/B

Chair: **Chris W. Hicks**
Naval Air Systems Command, Patuxent River, MD

34.1: Ultrasensitive-Broadband Passive Intermodulation Measurement Techniques

A. Christianson, J. Henrie, W. J. Chappell
Purdue University, West Lafayette, IN

A frequency-agile highly sensitive passive intermodulation measurement system was developed using tunable filtering. This allows the measurement of frequency-dependent effects as electrothermal generation as well as the measurement of many higher orders of intermodulation. This measurement capability supports the development and verification of root-principle passive intermodulation models.

34.2: Efficient Electrothermal Simulation of Three-Dimensional Integrated Circuits Using Compact Modeling: Version 2

T. Harris, S. Luniya, M. B. Steer
North Carolina State University, Raleigh, NC

As circuit density has increased, thermal effects have become primary design considerations. The fREEDA multiphysics simulator has been employed to model the electrothermal performance of a CMOS inverter. Electrothermal modeling of the inverter is an integral preliminary step in useful modeling of VLSI systems.

34.3: Autonomous Vision Processing and 3D Scene Reconstruction

W. S. Pitts, M. Vaidya, M. Kadambi, S. Malkani, P. D. Franzon
North Carolina State University, Raleigh, NC

Processing data from multiple sensors and implementing previously linear software algorithms into parallel hardware algorithms will be addressed. This presentation is focused on the ongoing research portion of a global plan for developing a method for multi-sensor 3-D scene reconstruction.

34.4: Broadband High-Dynamic-Range Inverse Standoff Analysis

J. R. Wilkerson, K. G. Gard, M. B. Steer
North Carolina State University, Raleigh, NC

Co-site interference is a limiting factor in the dynamic range of inverse standoff analysis systems. Broadband removal of this interference, obtained through automated feed-foward methods yielding at least 25 dB of cancellation, is reported. The resulting detection system has over 95 dB of dynamic range.

34.5: Optimal Finite-Difference-Based Transient Modeling of Guided Wave Propagation Using Gaussian Spectral Rules

A. Ramachandran, A. Cangellaris
University of Illinois at Urbana-Champaign, Urbana, IL

An algorithm for the generation of optimal non-uniform finite-difference grids for the analysis of electrically long-wave propagating structures such as multiconductor transmission lines (MTLs) and waveguides is presented. The methodology is based on a Padé-Chebyshev approximation of the input impedance computed on an equidistant grid and makes use of the Lanczos procedure, resulting in a compact multi-port frequency-dependent representation of the discretized segment. A dramatic reduction in computational cost is enabled by generating a discretization with just over two points per wavelength.

34.6: Extraction of Behavioral Models for Power Amplifiers with Memory Effects Using Vector Signal Analysis and a Dynamic Time-Frequency Signal

J. Hu, K. G. Gard , M. B. Steer
NC State University, Raleigh, NC

A system-level behavioral model for RF power amplifier (PA) with memory effects is presented. The amplitude and phase of distortion components is characterized as a function of the modulation frequency, using a Vector Signal Analyzer (VSA) and a dynamic frequency two-tone signal. Envelope frequency-dependent transfer function is then extracted to develop a behavioral model based on the parallel-cascade linear and nonlinear system.

34.7: Use of Parametric Ultrasonic Arrays for Standoff Analysis and Detection

G. Garner, III, M. Skeen
North Carolina State University, Raleigh, NC

The use of sound as a means to gather information about our environment has been developed with limited scope over the past decades. The primary application of this technology has been ultrasound and ultrasonic ranging. Recent developments in non-linear acoustics have proven that two-tone measurements and directional high-frequency parametric arrays can extract much more information about the size, shape, and density of objects under inspection. A novel approach using two-tone nonlinear effects to determine the size and composition of an object under inspection will be discussed. Such technology could have a significant impact in areas such as landmine detection and non-destructive testing.

34.8: Environment for Experimental Development of Wire-on-Ground Detection Methods

D. Patrick, K. G. Gard, M. B. Steer
North Carolina State University, Raleigh, NC

P. M. Buff
Vadum, Raleigh, NC

A compact experimental model is described for in-laboratory investigations of offset detection of wires lying on the surface of soil is described.

34.9: Remote Electronic Device Detection using Switched-Tone Probes

G. Mazzaro, M. Steer, K. Gard,
North Carolina State University, Raleigh, NC

K. Ranney
Army Research Laboratory, Adelphi, Maryland

A. Walker
Vadum, Raleigh, NC

A novel method for detecting RF front-ends using switched-tone probes will be presented. The reflective and re-radiative properties of antenna-filter bandpass networks are exploited in order to identify the presence of a wireless device and classify its communications band.

34.10: A Multiscale Approach to the Numerical Simulation of Complex Electronic Systems

A. Ramachandran, A. Cangellaris
University of Illinois at Urbana-Champaign, Urbana, IL

A methodology is described to address the multiscale transient simulation of complex systems. The technique combines SPICE-compatible models of detailed electromagnetic structures with FDTD modeling of transmission lines and backward Euler integration of standard circuitry. In addition, each of these components is simulated at a time scale that is appropriate to capture the dynamics of that component. Examples are given showing the application of this methodology to realistic problems.

34.11: Cancellation of Passive Intermodulation Distortion in Microwave Networks

J. Henrie, A. Christianson, W. J. Chappell
Purdue University, West Lafayette, IN

A circuit model enabling estimation of passive intermodulation distortion by point non-linearities in high-frequency networks is reported. Using this circuit model with standard sources of passive intermodulation (PIM), the residual sources of PIM within a system can be identified and cancelled, increasing system sensitivity.

34.12: Behavioral Modeling of Microwave RF Power Amplifiers

J. Lowry, M. Steer, K. Gard,
North Carolina State University, Raleigh, NC

Microwave ICs are ever growing in complexity. Behavioral models are great tools in abstracting out circuit behavior allowing for ease of simulation, and currently a major issue in system level simulation is the behavioral model of the RF PA and the ability to model spectral regrowth in the form of IMD and ACPR/ACLR.

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