GOMACTech-10

Government Microcircuit Applications and Critical Technology Conference

PROGRAM

"Microelectronics for Net Enabled and Cyber Transformational Technologies"

March 22 – 25, 2010

The Peppermill Hotel
Reno, Nevada

GOMACTech-10
FINAL PROGRAM
CONTENTS

WELCOME

The GOMACTech-10 Technical Program Committee is pleased to welcome you to this year's conference in Reno, Nevada. GOMACTech is the pre-eminent conference for the review of developments in microcircuit applications for government systems. GOMACTech was established in 1968 and is an Unclassified Export-Controlled event that requires all participants to be U.S. Citizens or legal U.S. Permanent Residents. Historically, the Conference has been the venue to announce major government microelectronics initiatives such as VHSIC, MIMIC, as well as others. This year also marks a new milestone for the technical breath of GOMACTech. We welcome the participation of this technical community.

This year's conference theme, ***"Microelectronics for Net-Enabled and Cyber-Transformational Technologies,"*** provides a forum that highlights the concept of net-enabled operations as a cornerstone for our national-defense posture. The underlying assumption of this vision is the availability of robust, reliable, secure information and communications infrastructures. As government and civilian activities develop net-enabled technologies, the national-defense communications infrastructure becomes an increasingly attractive target for adversary nation states in both covert and overt operations. The demand for microelectronics is imperative for developing trustworthy, high-bandwidth, and high-speed nano-scaled electronics to realize the vision. GOMACTech-10 provides a forum for discussing and demonstrating advanced microelectronics that can provide the transformational leap-ahead technologies to protect our communications networks from cyber attacks. Topics that support this vision are highlighted at this year's conference.

The conference will follow the successful format used over the past several years, including both technical and topical sessions. The technical sessions comprise contributed and solicited papers, including oral presentations and a Thursday morning poster session. A special section on student poster papers and competition will highlight the work of student contributors. The topical sessions will focus on a broad range of developments and accomplishments ranging from components to systems within selected ongoing government-sponsored programs. Some of this year's topical session themes include:

Microelectronics for Trustworthy Information Systems
Wireless Communications and Network Technologies
Nanoelectronics and Nanosensors
Wide-Bandgap Electronics
Ultra-Low-Power Electronics and Sources
Electro-Optical Technologies
Analog-to-Digital Components and Systems
Broadband Multifunction RF Systems
Circuits and Devices
Advanced Packaging and Interconnect Technologies
Radiation-Hardened Microelectronics Technologies
Power Electronics
Reconfigurable Electronics
Sensor C-SWAP
Advanced Antenna Arrays
Space-Environment Modeling and Monitoring
Metamaterials

The first of three scheduled tutorials is the first national Trusted Suppliers meeting. The objective is to gather members of industry and government agencies representing the interests of integrated-circuit and electronics producers who are focused on serving defense and aerospace applications which are trusted. This

summit is organized by Harry Kellzi of Teledyne. This day-long event will bring together suppliers who have been accredited as trusted in order to discuss critical issues facing this emerging community. Some of the key issues to be discussed include accreditation activity and criteria, emerging defense policy and demand for trusted supplies, trust solutions, and opportunities for industry to work together and with government for further progress in this area.

The early part of the day will focus on government representatives providing the status and updates on DoD policy, the accreditation process, and programmatic initiatives. Later in the morning, industry representatives will discuss their capabilities and services that serve the industry OEMs as well in supplying prime contracts to the defense and aerospace marketplace. The afternoon session will present a moderated panel discussion, representing both industry and government, which will take on topics that are frequently being asked by industry participants.

Organizations that are accredited by the time of the Summit are invited to participate as presenters at the Summit. Although the summit is open to all attendees, suppliers who are planning to become a certified Trusted Supplier are urged to attend because this event will be of utmost interest and beneficial to your organization in understanding, promoting, and networking with the Trusted Suppliers community.

In addition, two outstanding tutorials are offered on Monday with the cost included as part of the conference registration fee. The first tutorial titled, ***"Anti Tamper,"*** is organized by Dr. Robert Cunningham, Information Systems Technology Group, MIT Lincoln Laboratory, and Dr. Ted Lyszczarz, Submicrometer Technology Group, MIT Lincoln Laboratory. Tamper-resistant systems and anti-tamper techniques are important for ensuring that systems, the data they collect, and the control signals they emit are used as intended. The U.S. requires anti-tamper technology for military systems that we sell to our closest allies, to ensure that the ally can use the system, but not duplicate it. Commercial applications are important as well -- ATMs, satellite-TV boxes, cellular telephones, and video-game consoles are only a few examples. In both DoD and commercial applications, designers, producers, and operators need to cooperate to thwart potential reverse-engineering attacks. This half-day seminar will cover an approach to protect systems and the data they process and produce. The approach rests on a combination of policy, legal, and technical techniques. We will discuss some of the policy and legal issues, and focus on the technical techniques. The tutorial will motivate the need for anti-tamper techniques, drawing from commercial and DoD systems that have been attacked and illustrating the level of effort adversaries will invest in reverse-engineering. The tutorial also covers threat modeling, cryptography and side-channel attacks, and approaches to determine what needs to be done to protect the system from attack. The tutorial will conclude with a discussion of gaps in the space.

The second tutorial titled, ***"The Re-emerging Need for 'MIL-SPEC' Parts: Escalated Design Costs,"*** is organized by John Penn, Army Research Laboratory, Adelphi, Maryland The primary enabling technology for C4ISR over the past 40 years has been integrated electronics. However, the decisions made over 15 years ago to leverage commercial-off-the-shelf (COTS) parts nearly eliminated the demand for integrated circuits specialized for the military environment. Holding less than 1% of the global market for ICs, the majority of production capital and design intellectual property has migrated offshore. Nonetheless, the need remains for critical portions of the electronic design to be performed in a custom manner. In the meantime, design tool costs have continued to escalate as feature size and device densities have increased. Reconciling these cost challenges with design criticality and

throughput will initiate opportunities for novel business/ enterprise strategies.

The conference formally opens on Tuesday morning with an outstanding Plenary Session including a Keynote presentation by Dr. David A. Honey, Director of Research, Office of the Director, Defense Research and Engineering. Following the Keynote, there will be three Kilby Lecture speakers: Mr. Greg Gardner, Deputy Chief Information Officer, United States Intelligence Community; Dr. Wilfried Haensch, Senior Manager Advanced Si Devices and Explorative Technologies, IBM T. J. Watson Research Center; Col. Barry Shoop, Assistant Professor of Electrical Engineering and Deputy Head of the Department of Electrical Engineering and Computer Science at the United States Military Academy.

The Plenary, Technical, and Topical Sessions are the major venues for information exchange at the conference. Other opportunities for technical interaction are provided through the Exhibit Program that includes major IC manufacturers and commercial vendors of devices, equipment, systems, and services for nearly all facets of the electronics business. The exhibition opens on Tuesday at noon and runs through Wednesday at 4:00 pm. On Tuesday evening, attendees can mix in a relaxing atmosphere of food and good spirits at an Exhibitors' Reception. The Wednesday Luncheon Keynote speaker will be Dr. Kevin Kit Parker, Thomas D. Cabot, Associate Professor of Applied Science, Associate Professor of Biomedical Engineering, School of Engineering and Applied Sciences, Harvard University. Wednesday evening features the conference banquet, which this year will be held at the National Automobile Museum, followed by a show by the world-renowned "Galileo Players." On Thursday morning, there will be a Poster Session and for the first time a student poster competition. The Thursday Luncheon Keynote speaker will be Mr. James Gosler, Fellow, Sandia National Laboratories, formerly the Director of the Clandestine Information Technology Office at the CIA.

This year's strong technical program reflects the hard work and enthusiasm of the GOMACTech-10 Technical Program Committee. The committee members aggressively sought out particular topics and areas for presentations, and the quality of the conference certainly reflects this effort. It is our hope and belief that GOMACTech-10 will be a rewarding experience for all participants. We appreciate your support.

Chris Lesniak
Conference Chair

John Franco
Technical Program Chair

REGISTRATION

All GOMACTech-10 sessions will be held at The Peppermill Hotel in Reno, Nevada. Both check-in and on-site registration will take place in the hotel's Tuscany Ballroom Foyer.

Conference check-in and on-site registration hours:

Monday, 22 March – 7:00 am – 8:30 am (Tutorial 1 only)
Monday, 22 March – 9:00 am – 5:00 pm (General Check-in)
Tuesday, 23 March – 7:00 am – 5:00 pm
Wednesday, 24 March – 7:00 am – 5:00 pm
Thursday, 25 March – 7:00 am – 5:00 pm

SECURITY PROCEDURES

The GOMACTech Conference is an Unclassified, Export-Controlled event that requires participants to be U.S. Citizens or legal U.S. Permanent Residents. All registrants must provide proof of U.S. Citizenship or Permanent Resident status prior to being permitted entry into the conference. Additionally, a signed **Non-Disclosure Statement** will be required.

You may prove U.S. citizenship with any of the following:
U.S. Passport
Birth Certificate **AND** valid government-issued photo ID
Naturalization Certificate **AND** valid government-issued photo ID

The following are NOT proof of citizenship:
Voter registration card
Driver's license

GOMACTech TUTORIALS

Three tutorials of interest to the GOMACTech community are a special feature of the conference. The tutorials are all being held on Monday, 22 March. There is no additional fee for the Tutorials 2 & 3, but individuals must be registered for the Conference and must indicate their intention to attend a specific tutorial on their registration form. Tutorial 1 includes a lunch. The fee for Tutorial 1 is $20.

Tutorial 1: Trusted Suppliers Summit Tutorial

Monday, 22 March, 8:30 am – 5:00 pm
Peppermill Hotel, Tuscany 9

Organizer:
Harry Kellzi, Teledyne

The first national Trusted Suppliers meeting will gather members of industry and government agencies representing the interests of integrated-circuit and electronics producers focused on serving trusted Defense and Aerospace applications. This daylong event will bring together suppliers who have been accredited as trusted in order to discuss critical issues facing this emerging community. Some of the key issues to be discussed include accreditation activity and criteria, emerging defense policy and demand for trusted supplies, trust solutions and opportunities for industry to work together and with government for further progress in this area.

The early part of the day will consist of focused government representatives providing status and updates on DoD policy, the accreditation process, and programmatic initiatives. Later in the morning, industry representatives will discuss their capabilities, services that serve the industry OEMs, as well in supplying prime contracts to the Defense and Aerospace marketplace. The afternoon session will convene with a moderated panel discussion representing both industry and Government that will take on topics that are frequently being asked by industry participants.

Organizations that are accredited by the time of the Summit are invited to participate as presenters at the Summit. Although the summit is open to all attendees, suppliers who are planning to become a certified

Trusted Supplier are urged to attend because this event will be of utmost interest and beneficial to your organization in understanding, promoting, and networking with the Trusted Suppliers community

Tutorial 2: Anti-Tamper Tutorial

Monday, 22 March, 1:00 – 5:00 pm
Peppermill Hotel, Tuscany 11

Organizers:

Dr. Robert Cunningham, Information Systems Technology Group, MIT Lincoln Laboratory
Dr. Ted Lyszczarz, Submicrometer Technology Group, MIT Lincoln Laboratory

Tamper-resistant systems and anti-tamper techniques are important for ensuring that systems, the data they collect, and the control signals they emit are used as intended. The U.S. requires anti-tamper technology for military systems that we sell to our closest allies to ensure that the ally can use the system, but not duplicate it. Commercial applications are important as well – ATMs, satellite TV boxes, cellular telephones, and video-game consoles are only a few examples. In both DoD and commercial applications, designers, producers, and operators need to cooperate to thwart potential reverse-engineering attacks. This half-day seminar will cover an approach to protect systems and the data they process and produce. The approach rests on a combination of policy, legal, and technical techniques. We will discuss some of the policy and legal issues and focus on the technical techniques. The tutorial will motivate the need for anti-tamper techniques, drawing from commercial and DoD systems that have been attacked and illustrating the level of effort adversaries will invest in reverse-engineering. The tutorial also covers threat modeling, cryptography and side-channel attacks, and approaches to determine what needs to be done to protect the system from attack. The tutorial concludes with a discussion on gaps in the space.

Tutorial 3: The Re-emerging Need for "MIL-SPEC" Parts: Escalated Design Costs

Monday, 22 March, 1:00 – 5:00 pm
Peppermill Hotel, Tuscany 12

Organizers:

John Penn, Army Research Laboratory, Adelphi, MD

The primary enabling technology for C4ISR over the past 40 years has been integrated electronics. However, the decisions made over 15 years ago to leverage commercial-off-the-shelf (COTS) parts nearly eliminated the demand for integrated circuits specialized for the military environment. Holding less than 1% of the global market for ICs, the majority of production capital and design intellectual property has migrated offshore. Nonetheless, the need remains for critical portions of the electronic design to be performed in a custom manner. In the meantime, design tool costs have continued to escalate as feature size and device density have increased. Reconciling these cost challenges with design criticality and throughput will initiate opportunities for novel business/enterprise strategies.

LUNCH SPEAKERS

Lunch will be provided on all three days. Both the Wednesday and Thursday lunches will include presentations of interest to the GOMACTech community. The Wednesday Luncheon speaker will be Dr. Kevin Kit Parker, Thomas D. Cabot Associate Professor of Applied Science, Associate Professor of Biomedical Engineering, School of Engineering and Applied Sciences, Harvard University. The Thursday Luncheon speaker will be Mr. James Gosler, Fellow, Sandia National Laboratories – formerly the Director of the Clandestine Information Technology Office at the CIA.

EXHIBITION

An exhibition comprised of commercial vendors exhibiting products of interest to the GOMACTech community is an integral part of the conference. All attendees are reminded to visit the exhibitors. The Exhibit Hall is located in the hotel's Tuscany A/B Ballroom. Coffee breaks will be held in the exhibit area when they coincide with the exhibition's hours of operation. On Tuesday evening, an Exhibitors' Reception is planned.

Exhibition hours are as follows:
Tuesday, 23 March 12:00 pm – 8:00 pm
Wednesday, 24 March 9:00 am – 4:00 pm

List of Exhibitors (as of 3/8/2010)
Accel-RF
Aeroflex Colorado Springs
Analog Bits
BAE Systems
Cadence Design Systems, Inc.
CapeSym, Inc.
Cobham
Corwil Technology Corp.
Cypress Semiconductor
DMEA
Honeywell
IBM
Integra Technologies, LLC
ITT
Jazz Semiconductor
Kilopass Technology, Inc.
Maxtek Components Group
Micro-RDC
Midwest MicroDevices
MOSIS Services
Nallatech
National Reconnaissance Office
National Semiconductor Corp.
NNSA's National Secure Manufacturing Center
Northrop Grumman Corp.
ON Semiconductor
Peregrine Semiconductor
Rochester Electronics
Sandia National Laboratories
Silvaco Data Systems
Solid State Scientific Corp.
Synopsys
Tahoe RF Semiconductor, Inc.
Tela Innovations
Teledyne Microelectronics
Teradyne Global Systems
The Boeing Company
TriQuint Semiconductor
Trusted Access Program Office
Ultra Communications, Inc.
Virage Logic Corp.

WEDNESDAY EVENING SOCIAL

Dinner at Reno's National Auto Museum

The GOMACTech 2010 Special Event is truly a special event. It includes dinner at Reno's National Auto Museum and a performance by the famous Galileo Players.

The National Automobile Museum (The Harrah Collection) is a place where time, culture, beauty, history, human invention, ingenuity, and frivolity merge to fascinate us in the form of cars. The Museum houses an astounding collection, where visitors can explore decades of intriguing automobiles, stroll down period-style street scenes, and stand inches from cars once owned by the rich and famous.

Since the debut of their first original sketch show, 'Foresight is 20/20,' the Galileo Players have turned that investment into a virtual (meaning not yet real) comedic empire – cornering the market on comedy inspired by science and philosophy. The only limit to their ambition is time, space, and Newton's Third Law, which they have always found to be silly.

Buses will leave the hotel at 6:30 pm
Adults $25, Children (12 and under) $15.

HOTEL ACCOMMODATIONS

GOMACTech has reserved a block of rooms at the Peppermill at two special rates. These rates are exclusive of applicable Washoe County room tax of 12% and a $5 resort fee which includes use of the pool, valet, shuttle service to and from the airport, concierge, and local and 800# phone calls.

Peppermill Tower Rooms ($94 single or double) – The Peppermill Tower rooms offer panoramic views of the majestic Sierra Nevada mountains. These richly appointed rooms are designed in a spacious 365-sq.-ft. floor plan that offers smoking or non-smoking rooms. Remodeled throughout 2009.

Tuscan Tower Suites ($149 single or double on Monday through Thursday and $159 single or double on Friday through Sunday) – The Crown Jewel of the hotel's $400 million expansion is represented in the lavish accommodations you will find in the new Tuscan Suites. Hand painted Italian art and private foyers provide an elegant and personal space. From the custom made pillow top king beds and 42-in. plasma TVs to the spacious marble bathroom with a European soaking tub, separate marble shower, and high definition television, you are sure to find true elegance.

Reservations can be made on line at https://reserve2.peppermillcas.com/cgi-bin/lansaweb?PROCFUN+RN+RESNET+PRN+funcparms+UP(A2560)::gmact10;?

Or, by calling the hotel reservations department at 1-866-282-2444. Be sure to note that you are attending GOMACTech.

CONFERENCE CONTACT

Anyone requiring additional information about GOMACTech should contact the Conference Coordinator, Ralph Nadell, GOMACTech, 411 Lafayette Street, Suite 201, New York, NY 10003 (212/460-8090 x203), Rnadell@pcm411.com.

GOMACTech-09 PAPER AWARDS

Paper awards based on audience evaluations from GOMACTech-09 will include the George Abraham Outstanding Paper Award, a Meritorious Paper Awards, Best Poster Paper Award, and Best Student Poster Award. Presentation of these well-deserved awards will be made at the Plenary Session on Tuesday morning in Tuscan C Ballroom. The GOMACTech-09 winners are:

The George Abraham Outstanding Paper Award (24.1)

S. J. Koester, I. Lauer, A. Majumdar, T. P. O'Regan, J. Cai, J. Sleight, and L. Chang, IBM T. J. Watson Research Center, Yorktown Heights, NY
P. Tomasini, and S. G. Thomas, ASM America, Inc., Phoenix, AZ
"Design and Fabrication of Planar Si/SiGe Heterojunction Tunneling Transistors"

Meritorious Paper Award (19.3)

Charlie Kuznia and Chuck Tabbert, Ultra Communications, Inc., Vista, CA
"Board-to-Board Optical Interconnects within Aerospace and Missile/Munitions Systems"

Meritorious Paper Award (26.3)

Aaron D. Franklin, IBM T. J. Watson Research Center, Yorktown Heights, NY
Timothy S. Fisher, Purdue University, West Lafayette, IN
"*Toward Manufacturable Nanoelectronics Using Templated Vertical Carbon Nanotubes*"

Best Poster Paper Award (31.15)

Aleksey E. Bolotnikov, Giuseppe S. Camarda, Yonggand Cui, Anwar Hossain, Ge Yang, and Ralph B. James, Brookhaven National Laboratory, Upton, NY
Stephen Babalola, Fisk University and Vanderbilt University, Nashville, TN
Stephen U. Egarievwe, Brookhaven National Laboratory, Upton, NY and Vanderbilt University, Nashville, TN
"*Material Properties Limiting the Performance of CZT Gamma Ray Detectors*"

Best Student Poster Paper Award (32.10)

Jonmei Yang, University of California, La Jolla, CA
Paul Draxler, Qualcomm, Inc.
Donald Kimball, and Peter Asbeck, University of California, San Diego
"*High Efficiency Envelope Tracking High-Power Amplifier under Average Power Back-Off Operation*"

RATING FORM / QUESTIONNAIRE

Don't forget to vote for your favorite presentation this year before you leave the conference. A rating form/questionnaire is being handed out at conference check-in. To encourage submission of these forms, GOMACTech has a special gift for all attendees submitting a completed form. Please turn your form in at the Conference registration desk when you leave the Conference to receive your gift item.

SPEAKERS' PREP ROOM

The Tuscany 5 is designated as a speakers' preparation room and will be available during the hours the conference registration desk is open. Speakers are encouraged to use the Tuscany 5 facilities to ensure compatibility with the meeting's AV equipment. Speakers having difficulties should request at the conference registration desk to see an AV operator. Speakers are also asked to be at their assigned presentation room 30 minutes before the sessions begins to meet with their session chair. An AV operator will be assigned to each technical session room.

CD-ROM PROCEEDINGS

The GOMACTech CD-ROM Proceedings, containing searchable, condensed versions of submitted papers presented at the Conference will be distributed to all registrants. Additional copies of the CD-ROM can be purchased at the Conference at a cost of $40.00 per CD.

Previously published as the GOMAC Digest of Technical Papers, Volumes I – XXVII, this publication is the only record of the conference. Previous GOMAC Digests will, upon request, be made available to qualified Defense Technical Information Center (DTIC) users. Please call 1-800-225-3842 for bound or microfiche copies. Past Digests can be ordered by calling the above number and identifying the following accession numbers (please note that GOMAC was not held in calendar years 1985 and1995):

GOMAC-84 B113271	-86 B107186	-87 B119187
-88 B129239	-89 B138550	-90 B150254
-91 B160081	-92 B169396	-93 B177761
-94 B195015	-96 B212362	-97 B222171
-98 B235088	-99 B242763	-00 B254138
-01 B264749	-02 B275146	-03 M201604
-04 M201663	-05 M201849	-06 M202011
-07M202134	-08 M202438	-09 M202646

INFORMATION / MESSAGE CENTER

The Information/Message Center will be located adjacent to the GOMACTech Registration Desk in The Peppermill Hotel. The message center telephone number for incoming calls is (775) 826-2121. Callers should ask to be transferred to the GOMACTech Registration Desk.

PARTICIPATING GOVERNMENT ORGANIZATIONS

Participating Government Organizations of GOMACTech-10 include: Department of Defense (Army, Navy, Air Force) ... National Aeronautics and Space Administration ... Department of Commerce (National Institute of Standards and Technology) ... National Security Agency ... Department of Energy (Sandia National Laboratories) ... Department of Energy (National Nuclear Security Administration) ... Defense Logistics Agency ... Department of Health and Human Services ... Defense Threat Reduction Agency ... Defense Advanced Research Projects Agency ... Advisory Group on Electron Devices ... Central Intelligence Agency ... National Reconnaissance Office

GOMACTech WEB SITE

Information on GOMACTech may be obtained through its Web site at www.gomactech.net.

SPONSORS

GOMACTech would like to thank the following companies for their support.

NORTHROP GRUMMAN

BAE SYSTEMS

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HRL LABORATORIES

TUESDAY, 23 MARCH

PLENARY SESSION

Tuesday, 23 March / 8:30 am – 12:00 pm / Tuscany C

Opening Remarks **(8:30–8:45)**

Chris Lesniak, GOMACTech-10 General Chair
Air Force Research Laboratory, Wright-Patterson, AFB, OH

GOMACTech-09 Awards **(8:45–9:00)**

Keynote Address **(9:00–10:00)**

Dr. David A. Honey
Director of Research, Office of the Director, Defense Research and Engineering
U.S. Department of Defense, Washington, DC

"Innovation, Speed, and Agility"

BREAK **(10:00–10:30)**

Jack S. Kilby Lecture Series **(10:30–12:00)**

Greg Gardner
Deputy Chief Information Officer, U.S. Intelligence Community
Office of the Director of National Intelligence, Washington, DC

"Solving 'Wicked Problems'": The Promise of Creative Information Sharing"

Wilfried Haensch
Senior Manager, Advanced Silicon Devices and Explorative Technologies
IBM T. J. Watson Research Center, Yorktown Heights, NY

"Can Devices Help to Mitigate the Power/Performance Problem?"

COL Barry Shoop
Professor and Deputy Head, Department of Electrical Engineering and Computer Science
U.S. Military Academy, West Point, NY

"Photonics for Analog-to-Digital Conversion"

LUNCH **(12:00–1:30)**

Session 1

PHASED-ARRAY ANTENNA TECHNOLOGY I

Tuesday, 23 March / 1:30 – 3:00 pm / Tuscany 9

Chair: **T. W. Dalrymple**
AFRL, Wright-Patterson AFB, OH

Co-Chair: **P. E. Buxa**
AFRL, Wright-Patterson AFB, OH

1.1: A Broadband Eight-Element Phased-Array Antenna Receiver on LC Polymer in the Ka-Band (1:30)

J-C. S. Chieh, A-V. Pham
University of California Davis, Davis, CA

T. W. Dalrymple, K. Aihara
AFRL, Wright-Patterson AFB, OH

D. Kuhl, B. Garber
Berrie Hill Research Corp., Centerville, OH

An integrated phased-array antenna receiver module on liquid-crystal polymer is presented. The designed phased-array module has eight channels and is designed to operate in the Ka-band from 32 to 37 GHz and achieves a ±30° azimuthal beam-steering capability.

1.2: The Purdue Digital-Array-Radar Testbed (1:50)

C. Fulton, W. Chappell
Purdue University, West Lafayette, IN

The digital array radar (DAR) is a 16-element S-band sub-array prototype featuring advanced plastic packaging for high-power RF components, highly integrated transceiver chips to lower the overall IC count, a highly flexible operator interface, and digitization at each element with subsequent programmable digital beamforming for use as a research and demonstration tool for a future low-cost digital phased array.

1.3: Scalable Plug-and-Play Payload Building Blocks (2:10)

A. Jacomb-Hood, B. Martin, S. Robertson, M. Enoch, A. Kaytes, E. Cohen, P. Papula
Lockheed Martin Commercial Space Systems, Newtown, PA

D. Matcovich, C. Pomeroy
Lockeed Martin Missions Systems and Sensors, Newtown, PA

An approach to implementing future space ISR systems using scalable plug-and-play payload building blocks with open standard interfaces will be described. This approach shows promise in providing substantially improved performance for future systems, while reducing development time and overall system cost and improving operational responsiveness.

1.4: First-Generation Transverse-Diode-Array Electronically Scanned Antenna for Radar and Communications **(2:30)**

R. S. Robertson, R. T. Lewis, D. Baker, R. Broas, G. Kulakowski, D. Guiffreda
Raytheon Space and Airborne Systems, El Segundo, CA

W. Henderson
THINKOM, Torrance, CA

D. Baker, D. Ulmer
Raytheon Missile Systems, Tuscon, AZ

B. Pierce
DARPA, Arlington, VA

T. Kastle and T. Morton
AFRL, Wright-Patterson AFB, OH

A low-cost approach to developing microwave and millimeter-wave phased-array antennas will be discussed. The transverse diode array is capable of 1-D and 2-D scanning with reduced complexity at low power and very fast beam-steering response times.

BREAK **(3:00–3:30)**

Session 2

GRAPHENE FET ELECTRONICS

Tuesday, 23 March / 1:30 – 3:00 pm / Tuscany 10

Chair: **M. Fritze**
DARPA/MTO, Arlington, VA

Co-Chair: **C. Lau**
Institute for Defense Analyses, Alexandria, VA

2.1: Graphene Transistors (1:30)

D. Jena, K. Tahy, D. Shilling, Q. Zhang, T. Zimmermann, P. Fay, H. Xing, A. Seabaugh
University of Notre Dame, Notre Dame, IN

P. J. Luxmi, R. Feenstra
Carnegie Mellon University, Pittsburgh, PA

S. Koswatta
IBM T. J. Watson Research Center, Yorktown Heights, NY

Graphene is a new potential material for low-power RF and digital electronics. The potential of 2-D graphene and graphene nano-ribbons for such applications through physics-based modeling and experimental fabrication and characterization has been investigated. The properties of exfoliated and epitaxial graphene for electronic-device applications have been compared.

2.2: Characterization and Modeling of Exfoliated and CVD Graphene FETs (1:50)

S. Banerjee, E. Tutuc, L. F. Register
The University of Texas, Austin, TX

Dual-gated graphene FETs (GFETs) with ALD Al_2O_3 deposited on an oxidized Al nucleation layer had mobility values of 8600 cm^2/V-sec at room temperature. The deleterious effect of line edge roughness on charge transport was established using a non-equilibrium Green's function approach.

2.3: Growth of Epitaxial Graphene/SiC on the C-Face for Graphene FETs (2:10)

V. B. Shields, J. Hwang, S. Shivaraman, M. Kim, M. Chandrashekhar, M. G. Spencer
Cornell University, Ithaca, NY

The growth of few-monolayer graphene on (0001b) silicon carbide has been achieved by using a multistage temperature process consisting of a nucleation phase followed by an adiabatic cool-down phase. Reduction in surface roughness from about 23 to 2 nm was obtained. The corresponding thickness decreased from 30 to about five monolayers.

2.4: Ambipolar RF Electronics Based on CVD-Grown Graphene (2:30)

H. Wang, A. Hsu, J. Wu, J. Kong, T. Palacios
MIT, Cambridge, MA

The combination of the unique properties of graphene with new device concepts and nanotechnology can overcome some of the main limitations in conventional electronics. In this paper, two novel application concepts based on the ambipolar transport properties of graphene are demonstrated: graphene frequency multipliers and graphene ambipolar RF mixers.

BREAK (3:00–3:30)

Session 3

ADVANCES IN WIDE-BANDGAP SEMICONDUCTORS FOR MILITARY APPLICATIONS

Tuesday, 23 March / 1:30 – 3:00 pm / Tuscany 11

Chair: **J. D. Albrecht**
DARPA/MTO, Arlington, VA

3.1: Power Electronics Based on Gallium Nitride (1:30)

U. Mishra
University of California at Santa Barbara,Santa Barbara, CA

GaN has surprised the technical, business, and the defense communities with its ability to perform despite the maetrails problems based on the need for heteroepitaxy on foreign substartes. In particular, the large latttice and TCE mismatch on Si is a remaining hurdle for high-yield large-area devives for high-power applications.on a potentially low-cost substrate. The emergence of GaN subtsrates allows the development of vertical devices such as the CAVET.

3.2: Advances in GaN Technology for Military Applications (1:50)

J. W. Milligan, S. Wood, S. Sheppard, W. Pribble, J. B. Barner, J. Fisher, J. Palmour
Cree, Inc., Durham, NC

The advantages and commercial status of gallium nitride (GaN) HEMTs for use in military and commercial applications will be reviewed. The unique properties of GaN devices offer significant advantages for next-generation military systems. The commercial status of currently available GaN transistors, MMIC products, and foundry services will be reviewed.

3.3: E/D InAlN/GaN Devices with State-of-the-Art Characteristics (2:10)

P. Saunier, H.-Q. Tserng, T-M. Chou, M.-Y. Kao, D. Dumka, J. Jimenez
TriQuint Semiconductor, Richardson, TX

S. Guo, X. Gao
IQE RF LLC, Somerset, NJ

Enhancement- and depletion-mode devices have been fabricated on InAlN/GaN with selective gate recess. 0.2 x 50-µm E-mode devices have a 200-mV threshold voltage with a record 890-mS/mm transconductance and more than 2.0 A/mm. Measured F_t and F_{max} for an E-mode 2 x 50-µm device are 104 and 115 GHz, respectively.

3.4: GaN Electronics for Sub-Millimeter Wave and Mixed Signal Applications (2:30)

M. Micovic, K. Shinohara, H. Kazemi, I. Milosavljevic, A. Kurdoghlian, A. Corrion, S. Burnham, A. Schmitz, J. Li, D. Chow
Hughes Research Laboratories, Malibu, CA

GaN MMIC technology has demonstrated an RF power performance superior to any other MMIC technology up to a frequency of 100 GHz and has excellent potential for sub-mmw power applications. The latest mmw MMIC data will be presented, and the progress toward 800-GHz E- and D-mode GaN transistors under the DARPA NEXT program will be described.

BREAK (3:00–3:30)

Session 4

PHASED ARRAY ANTENNA TECHNOLOGY II

Tuesday, 23 March / 3:30 – 5:00 pm / Tuscany 9

Chair: **P E. Buxa**
AFRL, Wright Patterson AFB, OH

Co-Chair: **T. W. Dalrymple**
AFRL, Wright Patterson AFB, OH

4.1: Transformational Element Level Arrays Testbed (3:30)

M. Longbrake, J. Buck, P. Buxa, T. Dalrymple, J. McCann, R. Neidhard, K. Zeller
AFRL, Wright-Patterson AFB, OH

B. Garber, D. Kuhl
BerrieHill Research Corp., Dayton, OH

By integrating the latest in wideband phased-array antennas, miniaturized RF components, and digital signal processing, the AFRL TELA Testbed serves to demonstrate the latest in multi-channel sensor subsystem technology. An overview of testbed demonstrations will be shown, including analog true time delay and digital beamforming covering a 1–8-GHz bandwidth.

4.2: A 2–20-GHz Low-Noise Amplifier (3:50)

R. Benelbar, R. Mongia, S. Nelson, M. Walker, W. Perkenis, H. Sheehan, R. Cope
Cobham Sensor System, Richardson, TX

A 220-GHz low-noise amplifier (LNA) was designed using a double recess 0.15-µm InGaAs/GaAs power pseudomorphic high-electron-mobility transistor (pHEMT) process. The LNA achieves a noise figure less than 3 dB with 17 dB associated gain across the band at room temperature. Input and output return losses are 20 dB to >18 GHz. The LNA input third-order intercept point is near +12 dBm.

4.3: Multi-User Digital Beamforming for Wideband Array Processing (MUD-WASP) Antenna Development (4:10)

I. Rumsey
FIRST RF Corp., Boulder, CO

K. Aihara, P. Buxa, T. Dalrymple, J. Buck, J. McCann, M. Longbrake, R. Neidhard
AFRL, Wright-Patterson AFB, OH

A wideband (2–18 GHz) dual-polarized wide-scan array has been developed. The array provides eight full-bandwidth selectable-polarization outputs for each column that can be processed by digital or analog techniques to form eight independent beams. The antenna will serve as the front end for the AFRL MUD-WASP system. MUD-WASP system architecture and measured performance of the array will be presented.

4.4: A Miniature Reconfigurable Beamformer for Low-Cost Steerable Beam Antenna Systems (4:30)

M. DeLaquil, C. Baucom
L-3 Communications, Rockwall, TX

By using a hybrid approach incorporating MMIC and board-level delay elements, 4.2 nsec of true time delay is incorporated into a 2.75 x 3.5-in. package. A modular digital control architecture provides scalability and reconfigurability for a wide range of apertures or platforms. Combining this with a low-profile conformal antenna array creates a low-cost lightweight steerable beam antenna.

Session 5

GRAPHENE RF ELECTRONICS

Tuesday, 23 March / 3:30 – 5:00 pm / Tuscany 10

Chair: **M. Fritze**
DARPA/MTO, Arlington, VA

Co-Chair: **C. Lau**
Institute for Defense Analyses, Alexandria, VA

5.1: Top-Gated and Self-Aligned Epitaxial Graphene FETs with a Field-Effect Mobility of 6000 cm²/V-sec and Transconductance of 600 mS/mm (3:30)

J. Moon, D. Curtis, S. Bui, M. Hu
HRL Laboratories, Malibu, CA

K. Gaskill, T. Tedesco, G. Jernigan, B. VanMil, R. Myers-Ward, C. Eddy, Jr., P. M. Campbell
Naval Research Laboratory, Washington, DC

P. Asbeck
University of California at San Diego, San Diego, CA

J. Robinson, X. Weng
Penn State, University Park, PA

Recent breakthroughs in epitaxial graphene n-MOSFETs and p-MOSFETs will be presented. The epitaxial graphene MOSFETs are fabricated on 50-mm wafers with simultaneous world-record performance in key device parameters for the first time: excellent *I–V* saturation behaviors with low output conductance, field-effect mobility of 6000 cm²/*V*-sec for electron with I(on)/I(off) ratio of 19, and a peak transconductance of 600 mS/mm.

5.2: Carbon-Based Graphene Nanoelectronics (3:50)

C.-Y. Sung
IBM T. J. Watson Research Center, Yorktown Heights, NY

Graphene, a two-dimensional material with the highest intrinsic carrier mobility and many desirable physical properties at room temperature, is considered a promising material for ultrahigh-speed and low-power applications. The graphene nanoelectronics progress in synthesizing wafer-scale monolayer-controlled graphene and fabricating high-speed graphene FETs (GFET), with the highest value reported cut-off frequency approaching 100 GHz, will be reported. Bi-layered graphene FETs with I_{on}/I_{off} ratios of 100 and 1600 are demonstrated at T = 300 and 25K, respectively, which suggests graphene for not only analog but also logic device applications.

5.3: Chemical-Vapor-Deposition-Grown Graphene Transistor (4:10)

W. Liu, J. Zhu, B-C. Huang, C-H. Chung, C. Miao, Y. Wang, Y. J. Park, Y-H. Xie, J. Woo
UCLA, Los Angeles, CA

For the application of graphene transistors, a few-layer graphene using a chemical-vapor-deposition method was prepared. By using a low-temperature growth condition, the uniformity of graphene was remarkably improved. After transferring the graphene onto a SiO_2 substrate, the I–V characteristics were measured. Ambipolar conduction was clearly seen from the I_{DS}–V_{GS} curve. The linear relationship of I_{DS}–V_{DS} was observed with a drain voltage of 1 V.

5.4: Observation of Half-Integer Quantum-Hall Effect in Gated Epitaxial Graphene Grown on SiC (0001) (4:30)

P. Ye, T. Shen, J. Gu, M. Xu, Y. Wu, M. Bolen, M. Capano
Purdue University, West Lafayette, IN

L. W. Engel
National High Magnetic Laboratory, Tallahassee, FL

The epitaxial graphene films examined were formed on the Si face of semi-insulating 4H-SiC substrates by using a high-temperature sublimation process. A high-k gate stack on epitaxial graphene was realized by inserting a fully oxidized nanometer thin aluminum film as a seeding layer, followed by an atomic-layer-deposition process. The electrical properties of epitaxial graphene films are retained after gate-stack formation without significant degradation. At low temperatures, the quantum Hall effect in Hall resistance is observed along with pronounced Shubnikov-de Haas oscillations in the diagonal magneto-resistance of gated epitaxial graphene on SiC (0001).

Session 6

HIGH-POWER DIGITAL-TO ANALOG CONVERSION

Tuesday, 23 March / 3:30 – 5:00 pm / Tuscany 11

Chair: **D. S. Purdy**
DARPA, Arlington, VA

Co-Chair: **S. A. Pappert**
DARPA/MTO, Arlington, VA

6.1: Transversal Power DAC-Based Generation of Spectrally Pure High-Power Signals (3:30)

L. E. Pellon
Lockheed Martin, Moorestown, NJ

A new architecture and demonstrated results for bandpass reconstruction of high-power signals, directly from sigma-delta encoded digital signals, will be presented. An array of digital-to-analog converter (DAC) cells were combined and operated as a microwave transverse mixed-signal filter. A GaAs E/D implementation demonstrates S-band generation and –63-dBc intermodulation distortion.

6.2: Progress towards a High-Power Digital-to-Analog Converter (3:50)

R. Elder, C. Grens, W. Fabian, F. Stroili, D. Meharry
BAE SYSTEMS, Nashua, NH

Measured results on high-speed DAC and DDS circuits fabricated from SiGe and InP HBT technologies will be presented. Various technological factors that influence their performance and scalability to higher output power levels, improved power efficiency, and lower spurious output are also discussed.

6.3: Wide Bandwidth and High-Dynamic-Range Class-D Power DAC Based on Time-Encoded Modulation (4:10)

J. M. Cruz-Albrecht, P. Petre, J. F. Jensen, D. A. Hitko, J. Lazar
HRL Laboratories, Malibu, CA

A power digital-to-analog computer (DAC) architecture composed of an asynchronous time-encoder modulator that converts an input digital signal into an asynchronous pulse signal, a switch-mode amplifier that amplifies the pulse signal, and a filter that converts the pulse signal into analog is presented.

6.4: GaN HFET Development for Class-D Power DAC (4:30)

J. S. Moon, J. M. Cruz-Albrecht, P. Petre, J. F. Jensen, D. A. Hitko, J. Lazar, H. Moyer, P. Macdonald
HRL Laboratories, Malibu, CA

GaN switching HFET development for switch-mode amplifiers in high-power DAC architectures, where the high PAE and high C/IM3 can be modeled for targeting highly linear and efficient transmitter applications, will be presented.

WEDNESDAY, 24 MARCH

Session 7

POWER ELECTRONICS TECHNOLOGIES I

Wednesday, 24 March / 8:30 – 10:00 am / Tuscany 9

Chair: **F. J. Kub**
Naval Research Laboratory, Washington, DC

Co-Chair: **A. Hefner**
NIST, Gaithersburg, MD

7.1: Recent Advances and Applications of SiC Power Technology (8:30)

D. Grider, J. Palmour, A. Agarwal, S.-H. Ryu, M. Das, J. Zhang, R. Callanan, J. Richmond, C. Capell
Cree, Inc., Durham, NC

Significant recent advances have been made in the development of SiC power devices, including SiC DMOSFETs from 1200 V up to 10 kV, 1200-V SiC BJTs, as well as 8-kV SiC GTOs. These advances in SiC power device technology and their impact on the next generation of high-power and high-temperature electronics will be reviewed.

7.2: Advances in Normally Off SiC VJFETs with Ultra-Low Switching Energy for High-Efficiency Power-Electronics Applications (8:50)

D. C. Sheridan, A. Ritenour, J. B. Casady
Semisouth Inc., Starkville, MS

S. Mazzola
Mississippi State University, Starkville, MS

J. D. Scofield
AFRL, Dayton, OH

Normally off SiC VJFET devices scaled to >40 A and 1200 V are developed for high-power switching applications. Low specific on-resistances led to record low-switching energies which can significantly increase power system efficiencies.

7.3: Recent Advances in 1.2-kV Class SiC Power MOSFETs for Power Conversion Applications (9:10)

P. Losee, K. Matocha, J. Glaser, J. Nasadoski, S. Arthur, A. Gowda, L. Stevanovic
GE Global Research, Niskayuna, NY

SiC power MOSFETs are expected to replace silicon IGBTs in applications requiring high-temperature or high-density electrical power conversion. GE has developed 1.2-kV class SiC MOSFETs with low on-resistance and with predicted ~100-year gate-oxide reliability. In this work, GE's progress in developing SiC MOSFETs for high-frequency high-density power-conversion applications will be reported.

7.4: Fabrication and Analysis of a Dual 1.2-kV 400-A Silicon-Carbide MOSFET Power Module **(9:30)**

D. Ibitayo, D. Urciuoli, G. Koebke, R. Green
Army Research Laboratory, Adelphi, MD

The ARL Power Components branch recently completed the design and fabrication of an all-SiC 1.2-kV 400-A dual-MOSFET power module in a standard half-bridge configuration with an integrated custom heat sink. The fabrication and packaging techniques used as well as results of electrical testing will be reported.

BREAK **(10:00–10:30)**

Session 8

ADVANCED RF POWER AMPLIFIERS

Wednesday, 24 March / 8:30 – 10:00 am / Tuscany 10

Chair: **C. W. Hicks**
Naval Air Systems Command, Patuxent River, MD

Co-Chair: **P. A. Maki**
Office of Naval Research, Arlington, VA

8.1: High-Power Amplifier for the Mobile User Objective System (MUOS) (8:30)

G. Hegazi, T. Kean, M. Vagher, K. Witte, W. Sorsby
Rockwell Collins, Cedar Rapids, IA

The design of a high-power amplifier (HPA) for the Mobile User Objective System (MUOS) operation will be described. The 135-W HPA meets the linearity requirements of MUOS with an average efficiency of 59% in the 280–320-MHz band. The linearity of the HPA was verified in-band by measuring the notch depth of a special notched WCDMA signal at various drive conditions and out of band by measuring the ajacent channel leakage ratio (ACLR). Other considerations such as VSWR sensitivity, broadband noise, and automatic level control (ALC) will be discussed as well.

8.2: Power Scaling of GaN/Diamond Double Heterostructure HEMT (8:50)

E. L. Piner, J. C. Roberts
Nitronex Corp., Durham, NC

A novel technique has been developed to produce GaN/diamond AlGaN/GaN/AlGaN double-heterostructure HEMTs. The DH has been optimized for performance and the structure has been scaled to take advantage of the diamond thermal characteristics. A 10x scaling factor has been realized over conventional GaN HEMT technologies.

8.3: Linearized Class-E GaN MMIC High-Power Amplifiers for X-Band Operation (9:10)

J. Moon, H. Moyer, P. Macdonald, D. Wong, M. Antcliffe, M. Hu, P. Willadsen, P. Hashimoto, C. McGuire, M. Micovic, M. Wetzel, D. Chow
HRL Laboratories, Malibu, CA

Highly efficient and linear solid-state power amplifiers (SSPAs) are critically important for modern radar and communication systems, especially those with complex waveforms, high data rates, and a reduced thermal budget. Various methods, such as feed-forward and pre-distortion, have been introduced for simultaneously high efficiency and linearity operation at high power levels. For high-efficiency operation at higher output power levels, Class-E MMIC HPAs are designed with laterally scaled wideband-gap GaN HFETs with low on-resistance (< 2 Ω-mm), high breakdown voltages (~100 V), and relatively high f_t (> 55 GHz) and f_{max} (>180 GHz). The X-band Class-E GaN MMIC power amplifiers have an 8.5–12-GHz bandwidth with peak saturated output power of 5.5 and 9.9 W with an in-band variation of 0.8 dB. The peak power-added and drain efficiencies of 60% and 67% are demonstrated with an associated output power of 4.3 W. With an output power of 8.7 W, the associated drain efficiency is 59%, representing state-of-the-art performance.

8.4: W-Band GaN MMIC Power Amplifiers (9:30)

M. Micovic, A. Kurdoghlian, K. Shinohara, S. Burnham, I. Milosavljevic, D. Chow
HRL Laboratories, Malibu, CA

W-band GaN MMIC PAs that produce 77% more power at a frequency of 94 GHz than the highest power reported at this frequency for the best competing technology, InP HEMT, is reported. GaN MMIC technology enables new applications because it produces 10x more RF power at 94 GHz than InP MMICs

BREAK (10:00–10:30)

Session 9

INTEGRATED SILICON RF ELECTRONICS I

Wednesday, 24 March / 8:30 – 10:00 am / Tuscany 11

Chair: **J. E. Brewer**
Kairos Microsystems Corp., Melrose, FL

Co-Chair: **M. Fritze**
DARPA/MTO, Arlington, VA

9.1: Application of Silicon Technology to mm-Wave Transceivers for Gb/s Wireless Communication (8:30)

A. M. Niknejad, E. Alon
University of California at Berkeley, Berkeley, CA

The aggressive scaling of silicon transistors has resulted in mm-wave capability using a low-cost high-volume technology. In this work, the design of a 60-GHz transceiver in 90-nm CMOS technology was highlighted. Measurements of 4-Gbps wirelessly over 1 m at an energy consumption of only 77 pJ/bit demonstrate the capability of this technology.

9.2: Feasibility of Sub-Millimeter Wave CMOS ICs (8:50)

K. K. O
University of Texas, Dallas, Dallas, TX, and University of Florida, Gainsville, FL

D. Shim, C. Mao, R. Han
University of Florida, Gainsville, FL

S. Sankaran, E. Seok
Texas Instruments, Dallas, TX

C. Cao
Media Tek, Hsinchu, Taiwan

W. Knap
GES CNSR-U, Montpellier, France

The feasibility of using foundry logic CMOS to fabricate circuits operating at 100–700 GHz is demonstrated. According to the 2008 ITRS, by 2016 the required f_T and f_{max} of NMOS transistors are 520 and 670 GHz. Such transistors will provide greater flexibility to implement circuits and systems operating near 1 THz.

9.3: On the Development of Millimeter-Wave CMOS Digital Radio for DoD Applications (9:10)

J. Laskar, S. Pinel, S. Sarkar, P. Sen, B. Perumana, D. Dawn, F. Barale, M. Leung, J. Shin, S-W Hsiao P. Vadivelu, G. Iyer, A. Muppalla
Georgia Institute of Technology, Atlanta, GA

The state of the art of millimeter-wave single-chip CMOS digital radio and phased-array solutions, embedded in a standard plastic package, will be presented. The convergence of millimeter-wave CMOS digital-radio phased-array technology, low-power multi-gigabit mixed-signal processing, and phased-array antennas embedded in a standard plastic package will be discussed. This represents a unique opportunity to develop low-power millimeter-wave multi-gigabit radio for communication and sensing, at a similar cost structure as a Bleutooth® radio. These solutions offer the lowest energy per bit transmitted wirelessly at multi-gigabit-rate, reported to date, to meet the very stringent low-power specifications for battery-operated consumer-electronic portable devices as well as Millimeter-Wave Secure Body and Personal Area Networks for war-fighter connectivity.

9.4: Wide-Bandwidth Integrated Radar Architecture with On-Chip Phase Shifters (9:30)

G. Goldman
U.S. Army Research Laboratory, Adelphi, MD

J. Cali, F. F. Dai
Auburn University, Auburn, AL

An architecture for an integrated radar system with low cost, low power, and compact size that can support compressible wide-bandwidth waveforms with an on-chip electronic scanning capability is proposed. The major elements of the radar architecture are a transmitter, receiver, and a multi-phase phase-locked loop (PLL).

BREAK (10:00–10:30)

Session 10

POWER ELECTRONIC TECHNOLOGIES II

Wednesday, 24 March / 10:30 am – 12:00 pm / Tuscany 9

Chair: **A. Hefner**
NIST, Gaithersburg, MD

Co-Chair: **F. J. Kub**
Naval Research Laboratory, Washington, DC

10.1: The Current Pulsed Power Research, Development, and Evaluation at the Army Research Laboratory (10:30)

A. Ogunniyi, H. O'Brien, M. Morgenstern, C. Scozzie, A. Lelis
Army Research Laboratory, Adelphi, MD

W. Shaheen
Berkeley Research Associates, Beltsville, MD

The U.S. Army is currently supporting the development and evaluation of high-power solid-state components that will be utilized for survivability and lethality systems. The current power components being investigated for pulse-power applications are silicon Super-GTOs, silicon-carbide Super-GTOs, and silicon rectifiers. ARL presently has shifted their pulse-power evaluation focus from narrower pulse widths (< 1 msec) to wider pulse widths (> 1 msec).

10.2: Review of GaN Power Switch Technology (10:50)

F. J/ Kub, K. D. Hobart, T. J. Anderson
Naval Research Laboratory, Washington, DC

The status of GaN power switches will be reviewed, including key approaches to achieve normally off operation.

10.3: High-Power-Density, High-Efficiency, Fast-Transient-Response Silicon Carbide (SiC) Based Power Supplies for the Next-Generation of Radars (11:10)

G. Mitchell, E. Cilio, R. Shaw, M. Schupbach, A. Lostetter, J. Hornberger
Arkansas Power Electronics International, Inc., Fayetteville, AR

R. McCann
University of Arkansas, Fayetteville, AR

S. Mazumder
University of Chicago, Chicago, IL

Advances in radar systems are pushing the limits of present power-supply technology. To enable new concepts, such as active array radar systems, significant improvements in radar power-supply technology are required. Such improvements may be achieved through the use of SiC power devices in radar power supplies.

10.4: Void-Sized Process Control During Die Attach of Large-Area High-Power Semiconductor Devices (11:30)

D. Myron
Criteria Labs, Austin, TX

L. Giacoma
Triquint Semiconductor, Richardson, TX

Voiding between a die and thermal spreader significantly limits thermal power transfer. To realize the full potential of increased power densities from GaAs and GaN devices, a method to contain or limit void sizes to less than 0.15 mm during eutectic soldering has been developed.

LUNCH (12:00–1:30)

Session 11

CARBON NANOTUBES ELECTRONICS

Wednesday, 24 March / 10:30 am – 12:00 pm / Tuscany 10

Chair: **L. M. Cohn**
Naval Research Laboratory, Arlington, VA

11.1: An Overview of the NRO Foundational and Communications Technology Division: Carbon-Nanotube-Technology-Based Microelectronics Program **(10:30)**

L. M. Cohn
Naval Research Laboratory, Washington, DC

The NRO Applied Science and Technology Foundational and Communications Technology Division is supporting a number of programs to utilize CNT technology for various circuit applications. These applications include non-volatile memory, logic, low-noise linear amplifiers, and mixed-signal devices. In addition, CNT technology is also being investigated as a replacement for standard aluminum and copper wiring in integrated circuits. An overview of these activities will be given.

11.2: Lockheed Martin Nanosystems' NRAM (Non-Volatile Nanotube Random Access Memory) Development Program for Radiation Hardened Memory **(10:50)**

G. C. Taylor, G. Derderian, M. Meinhold, S. Buffat, J. Egerton
Lockheed Martin Nanosystems., Manassas, VA

CNT Memory can enable new levels of density, speed, unique design, and radiation hardness not available through conventional CMOS. Lockheed Martin is developing a 4-MB NRAM device tailored for deep space that will enable new missions.

11.3: Carbon-Nanotube-Technology Logic and Interconnect Technology Initiatives **(11:10)**

E. J. Egerton, S. Anderson, G. Derderian, D. Etter, M. Hornbeck, J. Nichols, Q. Ngo, M. O'Connor, A. Robinson, J. Ward
Lockheed Martin Nanosystems, Manassas, VA

Lockheed Martin Nanosystems, as part of a program to investigate revolutionary microelectronics technologies for future space-system applications, is investigating the use of CNT structures to replace conventional CMOS technologies. While these structures emulate standard mechanical relay devices, they have the potential to provide CMOS-competitive switching speed, draw no standby power, and should be impervious to ionizing radiation. This briefing will address this development effort and also the use of CNT as a replacement for interconnects and vias.

11.4: Carbon Nanotubes Technology for Mixed-Signal Circuit Applications **(11:30)**

J. Przybysz
NGES, Linthicum, MD

CNT transistors have demonstrated an ability to provide highly linear operation at low excitation voltages. Based on this demonstrated capability, CNT is being pursued for applications that include low-noise linear amplifiers and mixers where low power and high spurious-free dynamic range are very important. The attributes of CNT technology that provide this type of performance will be reviewed, and the status of ongoing programs in this area will be discussed.

LUNCH **(12:00–1:30)**

Session 12

INTEGRATED SILICON RF ELECTRONICS II

Wednesday, 24 March / 10:30 am – 12:00 pm / Tuscany 11

Chair: **M. Fritze**
DARPA/MTO, Arlington, VA

Co-Chair: **J. E. Brewer**
Kairos Microsystems Corp., Melrose, FL

12.1: Tunable DG-MOSFET Circuitry for RF CMOS and Mixed-Signal Systems (10:30)

T. S. Grimes
RNET Technologies, Inc., Dayton, OH

Advancements in the performance of silicon-based technologies have made them appropriate for integration in RF applications. The use of an advanced multi-gate process has enabled “tunable” RF circuit performance not possible using conventional means. Furthermore, practical reductions in circuit area, parasitics, and power are added benefits.

12.2: Direct Sampling Millimeter-Wave RFIC Tuner Development (10:50)

H. L. Levitt
Naval Research Laboratory, Washington, DC

J. L. Libove, B. R. Illingworth, N. S. Seay
Furaxa Corp, Orinda, CA

N. Jain
Anokiwave, San Diego, CA

Monolithic millimeter-wave (mmW) tuner ICs capable of downconverting 18–100-GHz RF signals from on a single chip are being developed by employing several novel circuit topologies, including improved low-noise amplifiers (LNAs), high-repetition-rate selectable-comb microwave samplers, varactorless VCOs, and sampling phase detectors. Recently developed direct RF sampling technology allows sub-harmonic local-oscillator (LO) injection, reducing power dissipation and enabling higher-frequency receiver operation for a given process. The resulting highly integrated mmW tuner architecture permits very wideband receivers capable of operating to at least 100 GHz, produced at very modest cost using commercial SiGe and InP foundry technologies. The design and a comparison of these sampler-based downconversion systems with conventional LO/mixer-based architectures will be described.

12.3: A Single-Chip 24-GHz SiGe BiCMOS Transceiver for FMCW Airborne Radars (11:10)

D. Saunders, S. Bingham, D. Crockett, J. Tor
ViaSat Advanced Microwave Products, Gilbert, AZ

G. Menon, N. Jain,
Anokiwave, San Diego, CA

R. Mende, M. Behrens
Smart Microwave Sensors, Braunschweig, Germany

A. Alexanian, R. N. Tiwari
RFmaker, Somerville, MA

The design and measured results of a highly integrated FMCW radar transceiver are presented. The 24-GHz ISM band transceiver includes a +7-dBm transmitter, dual receivers with 18-dB gain, PLL, 15-bit DAC, and a serial programming interface, all designed to operate from –40 to +125°C at 3.5 V, 275 mA.

12.4: Ultra Compact RF and MMIC Demonstrations (11:30)

M. Florian, A. J. Kleinosowski, R. Bonebright, G. Kromholtz
Boeing Research and Technology, Seattle, WA

Prototype chips which demonstrate the feasibility of ultra-compact radio-frequency and microwave designs for communications systems will be described.

LUNCH (12:00–1:30)

Session 13

RADIATION-HARDENED MICROELECTRONICS: BASIC MECHANISMS

Wednesday, 24 March / 1:30 – 3:10 pm / Tuscany 9

Chair: **L. J. Palkuti**
DTRA, Ft. Belvoir, VA

Co-Chair: **L. W. Massengill**
Vanderbilt University, Nashville, TN

13.1: Impact of Complex Material Systems on the Radiation Response of Advanced Semiconductors (1:30)

R. A. Reed, R. A. Weller, D. M. Fleetwood, N. Dodds, M. A. Clemens, B. Sierawski, A. Dasgupta
Vanderbilt University, Nashville, TN

Changes in materials and structures in modern microelectronic devices present new challenges for understanding radiation effects and developing radiation-tolerant devices and structures. Research advances focused on the basic mechanisms for single-event effects and dose-enhancement will be reported.

13.2: Fundamental Aspects of Radiation Event Generation for Electronics and Engineering Research (1:50)

R. A. Weller, R. A. Reed, M. H. Mendenhall, M. A. Clemens
Vanderbilt University, Nashville, TN

Nuclear-reaction final-state models were examined for their applicability to single-event effects simulation. A comprehensive mathematical framework for single-event rate computation encompassing both Monte Carlo and analytical computations has been established.

13.3: GeV Heavy-Ion-Induced Transient Measurement and Analysis for Next-Generation III-V Structures (2:10)

D. McMorrow, J. B. Boos, J. Warner
Naval Research Laboratory, Washington, DC

S. DasGupta, R. Reed, R. Schrimpf
Vanderbilt University, Nashville, TN

V. Ferlet-Cavrois
European Space Agency, Noordwijk, Netherlands

J. Baggio, P. Paillet, O. Duhamel
CEA/DIF, Bruyères-le-Châtel, France

High-bandwidth (12 GHz) time-resolved heavy-ion-induced charge-collection measurements for irradiation up to 45 GeV/amu are performed on low-power 6.1-A AlSb/InAs and InAlSb/InAs HEMT devices. A device model for the AlSb/InAs HEMT is developed and used to address the charge-collection mechanisms in this technology.

13.4: Nano-Scale Properties of Dielectrics for Radiation-Tolerant DoD Devices (2:30)

G. Lucovsky
North Carolina State University, Raleigh, NC

Nano-scale bonding in SiO_2, Si oxynitrides, and high-k dielectrics that minimizes the generation of electronically active defects after x-ray and gamma irradiation are identified. This study combines the many-electron theory, advanced spectroscopic techniques with experimental results on x-ray and gamma-irradiated films, and MOS capacitor structures to identify radiation-induced defects.

13.5: Modeling Ionizing Radiation Effects in Solid-State Materials and CMOS Devices (2:50)

H. J. Barnaby, I. S. Esqueda
Arizona State University, Tempe, AZ

A comprehensive model which enables the effects of ionizing radiation on bulk and SOI CMOS devices and parasitic structures to be simulated with closed form functions will be presented. An approach whereby defect distributions in these oxides are calculated, incorporated into implicit surface potential equations, and ultimately used to model radiation-induced leakage currents in MOSFET structures and integrated circuits will be described. The features having the greatest impact on the increased radiation tolerance of advanced deep-submicron bulk and SOI CMOS technologies will also discussed.

BREAK (3:10–3:30)

Session 14

TRUSTED SYSTEMS FROM UNTRUSTED COMPONENTS

Wednesday, 24 March / 1:30 – 3:00 pm / Tuscany 10

Chair: **F. W. Sexton**
Sandia National Laboratories, Albuquerque, NM

Co-Chair: **B. S. Cohen**
Institute for Defense Analyses, Alexandria, VA

14.1: Trusted Computing Solution (1:30)

D. M. Deming
Sandia National Laboratories, Albuquerque, NM

A verifiably secure trusted computing solution that addresses the fundamental limitations of commercially available computing resources and simulation tools for use in the development of high-consequence applications that process, store, and share mission-critical information often out of our direct control and/or located in foreign countries has been developed.

14.2: LPC/SPI Analysis Tool (1:50)

T. A. S. Pierce, M. Berg, C. Hoff, B. Kucera
Sandia National Laboratories, Albuquerque, NM

Sandia National Laboratories has created a set of tools to capture and analyze LPC and SPI bus traffic. A custom board can attach directly to the bus headers. Software tools support filtering, parsing, and searching traffic. These prototype tools may help analyze any components that communicate via LPC/SPI.

14.3: The Challenge and Necessity of Circuit Design with Unknown Intellectual Property (IP) Blocks (2:10)

S. Fazzari, C. Maxey
Booz Allen Hamilton, Arlington, VA

The evolving requirements for modern circuit design are requiring more functionality then ever before. The various capabilities needed in a FPGA or ASIC are generally available in the form of a third-party IP block. These blocks are being used more and more with potential risks which must be understood.

14.4: Verifying Trust for Defense-Use Commercial Semiconductors (2:30)

S. Pope
OSD, Industrial Policy, Arlington, VA

B. S. Cohen, V. Sharma, R. Wagner, L. W. Linholm
IDA, Alexandria, VA

S. Gillespie
Potomac Institute for Policy Studies, Arlington, VA

A systematic study identified verification techniques and assessed their effectiveness in identifying counterfeit and tampered integrated circuits from commercial sources acquired for DoD systems. Representatives of government, private industry, and academia helped identify and characterize key verification attributes and their overall effectiveness for each technique.

BREAK **(3:00–3:30)**

Session 15

RF TAGS

Wednesday, 24 March / 1:30 – 3:00 pm / Tuscany 11

Chair: **J. E. Penn**
Army Research Laboratory, Adelphi, MD

Co-Chair: **G. A. Mitchell**
Army Research Laboratory, Adelphi, MD

15.1: Wireless Hive Networks (1:30)

W. Trybula
Trybula Foundation, Austin, TX

H. Potash
Independent, Austin, TX

L. P. Rochemont
Gigacircuits, Inc., Austin, TX

Starting with the definition that Wireless Hive Networks are communities of wireless devices for distributed applications, one can conjure many different type of interesting applications. There has been conjecture that the initial applications will have volume requirements that will greatly outstrip the semiconductor manufacturers' ability to produce the quantity required. The cost of creating and distributing devices for very specialized operations is significant. The power requirements to drive the circuitry currently is supplied by a limited-life battery or by power generated by an RF signal from an interrogating source. The issue always arises on where does the processing occur? At the sensor or at a central receiver? What type of semiconductors is required?

15.2: Advances in Thin Active Microsystems (1:50)

J. A. Payne, K. J. Tracey, R. H. Olsson III, C. A. Apblett
Sandia National Laboratories, Albuquerque, NM

An overview of research activities at Sandia National Laboratories (SNL), directed toward decreasing the overall thickness of self-contained battery-powered microsystems, will be presented. Technical advances covering device interconnect, thin power sources, sensor electronics preparation, and data relay will be reviewed.

15.3: Integrated-Circuit Design for Enhanced Performance of Commercial-Off-the-Shelf RF Transceivers (2:10)

G. Mitchell, J. Penn
Army Research Laboratory, Adelphi, MD

COTS RFIC transceivers have been optimized for low-cost large-volume commercial applications that do not always meet the needs of critical systems. A simple means of enhancing the RF performance, or boosting the capabilities of the COTS RFIC, would be to add (an) additional circuit(s) between the RFIC and the antenna using appropriate technologies to trade-off the size, efficiency, and performance needs of the system with minimal impact. An example of an enhanced booster IC using GaAs technology to provide customized RF performance compatible with existing RFIC COTS circuits is presented. Software and applications using the COTS parts are preserved to minimize the system-level impact (KISS) while optimizing the output power, noise figure, modulation, and RF performance of the overall system.

15.4: Demonstration of a Networked RFID Solution to System-Level Prognostics and Diagnostics (2:30)

G. Mitchell, M. Conn
Army Research Laboratory, Adelphi, MD

Automated data acquisition is paramount to success as the Army moves towards condition-based maintenance for new and legacy platforms. This encouraged the development of a prototype radio-frequency identification tag solution. The demonstration of a network of tags used for health monitoring on an Army platform will be discussed.

BREAK (3:00–3:30)

Session 16

RADIATION-HARDENED MICROELECTRONICS: DESIGN

Wednesday, 24 March / 3:30 – 5:10 pm / Tuscany 9

Chair: **B. Wilson**
DTRA, Ft. Belvoir, VA

Co-Chair: **L. J. Palkuti**
DTRA, Ft. Belvoir, VA

16.1: Foundry-Flexible Radiation Hardness by Design for Mission Critical Space Systems (3:30)

A. J. Kleinosowski, T. Amort, W. Snapp, J. Evans, R. Brees, B. Buchanan
Boeing Research and Technology, Seattle, WA

The historical evolution of radiation hardness by design (RHBD) for space systems will be discussed. Examples are given showing how RHBD complements radiation hardness by process. Additional examples show how RHBD can be used with commercial foundries, thereby keeping pace with microelectronic scaling and capturing the performance and integration density available in contemporary commercial device technologies.

16.2: Recent Advances in Radiation-Hardened-by-Design Analog and Mixed-Signal Design (3:50)

W. T. Holman, L. W. Massengill, B. L. Bhuva, A. F. Witulski, D. Loveless
ISDE / Vanderbilt University, Nashville, TN

Recent advances in the mitigation of single-event transients (SETs) in analog and mixed-signal circuits can reduce SET cross-section by more than an order of magnitude with minimal area and performance penalties. This tutorial provides an overview of new RHBD techniques and a discussion of future research directions.

16.3: Single-Event Hardening of High-Speed Mixed-Signal Circuits (4:10)

T. D. Loveless, L. W. Massengill, W. T. Holman, B. L. Bhuva
Vanderbilt University, Nashville, TN

Primary challenges and successes regarding single-event hardening of mixed-signal circuits will be discussed. Novel, technology independent approaches for transient mitigation in phase-locked-loop circuits are provided along with design examples and guidelines for hardened-by-design phase-locked-loop circuits.

16.4: Honeywell 150-nm SOI ASIC Results (4:30)

J. Graebel, D. K. Nelson, J. Hobbs
Honeywell Aerospace, Plymouth, MN

Honeywell's 150-nm rad-hard HX5000 ASIC family and wafer technology QML qualification data will be briefly summarized. Also discussed will be new development activities for a number of features being added to these platforms and the addition of a newly structured array product using the same wafer technology.

16.5: New Test and Analysis Approaches for SEE Characterization **(4:50)**

D. G. Mavis, P. H. Eaton, M. D. Sibley, J. Castillo, D. Elkins, R. Floyd
Microelectronics Research Development Corp., Albuquerque, NM

New test hardware, data acquisition software, and analysis techniques will be described. Multiple-bit upset identification methods and the impact on error detection and correction are discussed. Also, new raster-scanning approaches, with spatial error isolation as small as 10 μm, can isolate dominant circuit susceptibilities in complex modern microcircuits.

Session 17

MICROWAVE SYSTEMS DIAGNOSTICS

Wednesday, 24 March / 3:30 – 5:00 pm / Tuscany 10

Chair: **M. B. Steer**
North Carolina State University, Raleigh, NC

Co-Chair: **W. D. Palmer**
Army Research Office, Durham, NC

17.1: Time-Frequency Effects in Wireless Communication Systems **(3:30)**

G. J. Mazzaro
Army Research Laboratory, Adelphi, MD

M. B. Steer, K. G. Gard
North Carolina State University, Raleigh, NC

Time-frequency effects in wireless communication systems caused by narrow-band resonances and coupled with device non-linearities are revealed as new sources of intersymbol interference and intermodulation distortion. These effects are exploited for the metrology of bandpass circuits.

17.2: The Causality Enforcement in Numerically or Experimentally Obtained Microwave Network Transfer Function **(3:50)**

J. H. Chung, A. C. Cangellaris
University of Illinois, Urbana-Champaign, IL

An approach is proposed for rendering the impulse response of a passive, microwave multi-port described in terms of a band-limited network transfer function matrix obtained either through numerical modeling or measurement. The proposed approach eliminates the need for enforcing passivity of the rational function fits commonly used for the incorporation of such network transfer functions in general-purpose non-linear network analysis simulators.

17.3: The Effect of External Magnetic Field on Passive Intermodulation in Ferrogmagnetic-Containing Microwave Components **(4:10)**

J. Henrie, A. Christianson, W. J. Chappell
Purdue University, West Lafayette, IN

It was found that a strong external DC magnetic field will reduce the passive intermodulation distortion generated by microwave components which contain ferromagnetic material. This reduction in distortion can be as much as 40 dB. Because of the penetrating nature of magnetic fields, this effect can be useful for mitigating passive intermodulation in electrically shielded components such as coaxial connectors.

17.4: Forensic Circuit Analysis Using Reflected Filter Response Characteristics (4:30)

A. K. Mikkilineni, D. King-Smith, S. B. Gelfand, E. J. Delp
Purdue University, West Lafayette, IN

A general framework for forensic characterization of RF devices will be presented. When a device is excited by a specially designed RF probe signal, a portion of the probe energy is re-emitted and is known as the reflected response of the device. The reflected response contains features that are specific to the type of filter contained in the RF front-end. By using feature derived from the reflected response, the RF devices can be uniquely determined.

Session 18

PiezoMEMS

Wednesday, 24 March / 3:30 – 5:10 pm / Tuscany 11

Chair: **R. G. Polcawich**
Army Research Laboratory, Adelphi, MD

Co-Chair: **R. D. DelRosario, Jr.**
Army Research Laboratory, Adelphi, MD

18.1: Piezoelectric MEMS for Defense Applications (3:30)

D. Polla
DARPA, Arlington, VA

Piezoelectric materials have been available to the microsystems community for years, yet there remain substantial challenges with regards to successfully integrating piezoelectric materials and high-performance silicon electronics. Multiple unmet requirements for DoD applications necessitate the incorporation of piezoelectric material capabilities with CMOS integrated circuits. Significant opportunities exist for realizing large-force large-displacement MEMS actuators; low-impedance resonators; low-power low-noise sensors; low-loss ultra-capacitors; and most recently energy harvesters. The fundamental unsolved technical problem of attaining good IC-compatible piezoelectric materials despite the thermal-processing constraints presents significant challenges.

18.2: Processing of High-Strain Piezoelectric Films for MEMS (3:50)

S. Trolier-McKinstry
Pennsylvania State University, University Park, PA

Materials such as $PbZr0_{0.52}Ti0_{0.48}O_3$ offer large piezoelectric constants for MEMS applications, but at the expense of complexity in deposition and patterning. Among the challenges currently facing the field are the high process temperatures associated with crystallizing high-quality ferroelectric materials, which precludes integration with temperature-sensitive substrates (including polymers and CMOS), the large capacitance of lead-based ferroelectrics (which can be challenging in energy harvesting applications), and difficulties in patterning complex oxides. Three approaches to circumventing these difficulties – (1) the design of the piezoelectric itself to maximize the property coefficients for particular MEMS applications, (2) damage-free patterning of lead-based piezoelectrics using microcontact printing, and (3) use of laser annealing to decrease crystallization temperatures below 400°C – will be discussed.

18.3: Design and Fabrication of PiezoMEMS Devices for Communications, Radar, and mm-Scale Robotics Applications (4:10)

J. Pulskamp, R. G. Polcawich, G. Smith
Army Research Laboratory, Adelphi, MD

Key areas for PiezoMEMS, including communications, radar, and small-scale robotics applications, will be outlined. The key enabling feature of the technology is a fabrication technology capable of creating a wide array of structures and devices using thin-film PZT and combinations of surface and bulk micromachining.

18.4: Ferroelectric Integration and Contamination Control Methods Developed for Ferroelectric Memories (4:30)

G. R. Fox
Fox Materials Consulting, LLC, Colorado Springs, CO

Many of the FeRAM processing methods and materials compatibility constraints are portable to MEMS device development. A FeRAM technology overview for processes ranging from 1 to 0.13 µm CMOS nodes will be presented while attempting to reveal techniques that can be directly applied to MEMS device development and manufacturing.

18.5: Multi-Frequency Aluminum Nitride Micro-Filters for Advanced RF Communications (4:50)

R. H. Olsson III, K. E. Wojciechowski, M. R. Tuck, J. E. Stevens, C. D. Nordquist
Sandia National Laboratories, Albuquerque, NM

An AlN MEMS resonator technology has been developed, enabling massively parallel filter arrays on a single chip. Low-loss filter banks covering the 10 MHz–10 GHz frequency range have been demonstrated, as has monolithic integration with inductors and CMOS circuitry. The high level of integration enables miniature multi-band, spectrally aware, and cognitive radios.

THURSDAY, 25 MARCH

Session 19

TRUSTED DEFENSE SYSTEMS

Thursday, 25 March / 8:30 – 10:00 am / Tuscany 9

Chair: **E. D. Maynard**
ODUSD(S&T), Washington, DC

Co-Chair: **B. S. Cohen**
Institute for Defense Analyses, Alexandria, VA

19.1: Implementing DTM 08-048: Supply Chain Risk Management (8:30)

W. J. Meyers
SAIC, Linthicum, MD

The recently released/updated (Feb 09; update in pre-coordination staffing Sept. 09) Directive Type Memorandum from the Deputy Secretary of Defense titled "Supply Chain Risk Management (SCRM) to Improve the Integrity of Components Used in DoD Systems" will be addressed. The policies, applicability, and responsibilities of the various DoD components will be explained and discussed. A specific example of implementation of these policies in a major acquisition program will be detailed.

19.2: 300-mm Wafer-Scale-Integrated Processing Capability for Research and Development on Novel Materials and Device Concepts (8:50)

M. Liehr, C. Borst
College of Nanoscale Science and Engineering
State University at Albany, NY

The 300-mm process capabilities for state-of-the-art semiconductor and 3-D integration at the College of Nanoscale Science and Engineering in Albany, New York, are described. The outlook is to develop an option for collaboration support in derivative development off a standard CMOS base.

19.3: Integrated Circuit Supply Chain Vulnerabilities (9:10)

B. S. Cohen, V. Sharma, M. R. Stytz, R. R. Wagner, D. J. Goldstein, L. W. Linholm
Institute for Defense Analyses, Alexandria, VA

S. Gillespie
Potomac Institute for Policy Studies, Arlington, VA

A study summarizing previous work characterized the vulnerabilities in the supply chain for integrated circuits. The vulnerabilities were assessed using a vulnerability scoring system and a prioritization was performed identifying selected vulnerabilities that represent particular risks for defense applications.

19.4: Counterfeit Electronic Components in the Supply Chain: Impacts, Factors, and Best Practices (9:30)

M. H. Crawford
U.S. Department. of Commerce, Washington, DC

The presence of counterfeit discrete electronic components and integrated circuit products were increasingly being reported in commercial and defense-system electronic supply chains. The Bureau of Industry and Security at the Department of Commerce undertook a study in 2008 to assess the extent of counterfeit parts being encountered, the factors contributing to the problem, and policies and practices used to combat infiltration of counterfeit parts into U.S. supply chains.

BREAK (10:00–10:30)

Session 20

COMMUNICATIONS AND INFRASTRUCTURE NETWORKS

Thursday, 25 March / 8:30 – 10:00 am / Tuscany 10

Chair: **R. Burk**
Defense Threat Reduction Agency, Ft. Belvoir, VA

20.1: Insights from the Emerging Discipline of Network Science? (8:30)

I. Ponomarev
Penn State University, University Park, PA

R. Burk
Defense Threat Reduction Agency, Ft. Belvoir, VA

The emergence of network science as a distinct discipline, key research results to date, and current research approaches to networked phenomena will be discussed.

20.2: Baseline Survivability of Networks for EMP and IEMI Attacks (8:50)

I. Kohlberg
Kohlberg Associates, Reston, VA

Baseline survivability of today's communications networks differ in several ways from survivability of Cold War networks. The analytic foundations for determining baseline survivability of networks today will be addressed.

20.3: Complexity and Robustness in Stochastic Network Utility Maximization (9:10)

D. Zheng, J. Zhang
Arizona State University, Tempe, AZ

DoD's network-centric operations hinge heavily on the reliability and efficacy of the Internet and wireless ad-hoc/sensor networks, for collecting, processing, analyzing, and managing information in adverse noisy environments. Maintaining consistent availability of quality of services (QoS) is extremely difficult across the Internet and hostile wireless networks. A principal goal of this study is to understand the complexity and robustness in the optimization of stochastic networks. The impact of noise feedback on the primal-dual algorithm is the focus of this paper. The distributed two time-scale algorithms based on primal decomposition were studied, and the impact of noisy feedback on stochastic stability therein was explored. This study enables the comparison of alternative decompositions by the important metric of robustness to noisy feedback.

20.4: Capacity of Large Fading Relay Networks under Random Attacks (9:30)

C. Huang, S. Cui
Texas A&M University, College Station, TX

J. Jiang
Stanford University, Stanford, CA

To understand the network response to large-scale physical attacks, the asymptotic capacity of a half-duplex large fading relay network under random attacks was investigated when the number of relays tends to infnity, where the multiple access cut-set upper bound and the achievable rate for both the amplify-and-forward (AF) and decode-and-forward (DF) strategies, with a focus on analyzing the attack eects, were derived.

BREAK (10:00–10:30)

Session 21

ENERGY SCAVENGING FOR UNATTENDED SENSOR

Thursday, 25 March / 8:30 – 10:00 am / Tuscany 11

Chair: **B. McQuiston**
DARPA, Arlington, VA

Co-Chair: **K. A. Griggs**
Puritan Research Corp., Vienna, VA

21.1: Power Distribution Systems for Distributed Sensor Networks and Pervasive Computing (8:30)

M. Peckerar, M. Dornajafi, Z. Dilli, N. Goldsman, M. Dagenais
University of Maryland, College Park, MD

Distributed sensor networks and computational grids are of prime importance to modern defense technology. These are sensor arrays and low-power computers configured to form a communicating network. Their primary use is in military applications where they assess the nature and magnitude of an on-coming threat. Data on the operation of such a system used with "energy harvesting" components, empowered by light, radio waves, and vibrating sources, will be presented

21.2: Tactical Energy Independence: Creating Energy Abundance, Efficiency and Diversity (8:50)

B. McQuiston
DARPA, Arlington, VA

DARPA's comprehensive research and development is creating technologies that can lead to tactical energy independence. The goal is to generate cost-effective alternative energy technologies for the military, addressing energy generation, conversion, control, and conservation from sustainable sources. By addressing the military's own energy needs and security, larger solutions that are relevant to us all can be proposed.

21.3: Piezoelectric Vibration Energy Scavenging for Unattended Sensors (9:10)

L. M. Miller, E. K. Reilly, R. Fain, P. Wright
University of California at Berkeley, Berkeley, CA

For ubiquitous wireless sensors to be realized, all of the constituents of the device must be directly integratable. An apparent solution lies in the conversion of mechanical energy lies in the conversion of mechanical energy to electrical output via the growth and direct integration of piezoelectric thin-film unimorphs on the standard CMOS silicon platform.

21.4: Power Beaming techniques for NASA's Centennial Challenge (9:30)

R. Winsor, A. Bakos, T. Stone
Lighthouse Development LLC, Rockville, MD

B. Murray
National Space Society, Washington, DC

Concepts for power beaming (wireless power delivery using light) as applied to the 2008 NASA Centennial Challenge along with our specific approach will be presented. The extension of our design to alternate applications of power beaming is presented, extending to longer distances and other beam characteristics such as divergence, power, and wavelength of operation.

BREAK (10:00–10:30)

Session 22

ON-CHIP AUTHENTIFICATION AND IDENTIFICATION

Thursday, 25 March / 10:30 am – 12:00 pm / Tuscan 9

Chair: **D. R. Collins**
DARPA, Arlington, VA

22.1: Countering the Counterfeit Threat: National Semiconductor Unique Number Generator Technology for Die ID Applications **(10:30)**

G. Zawitoski
National Semiconductor Corp., Annapolis Junction, MD

The National Semiconductor UNG Module is a 256-bit self-programmable ROM that uses natural variations in the manufacturing processing to create a unique binary number which essentially functions as a die fingerprint that cannot be duplicated. The Die ID can be read at wafer sort, after assembly, at temperature, and in the field using a custom test board (USB Die ID Reader Board) to ensure that the product being placed into a system is authentic. Theoretically, there are 2.7×10^{67} possible IDs, and the probability of a repeat number is 3.7×10^{-66}%. This technology provides a way to track any important information about the chips life-cycle simply and cost efficiently while providing assurance that the die is authentic.

22.2: Recombination of Physical Unclonable Functions **(10:50)**

M-D. (Mandel) Yu
Verayo, Inc., San Jose, CA

S. Devadas
MIT, Cambridge, MA

Physical Unclonable Function (PUF) circuits have the ability to uniquely identify integrated circuits based on manufacturing variations. From a cryptographic standpoint, most PUFs have naturally biased outputs. Recombination techniques can be used to debias PUF outputs without exploding noise, allow natively non-challengeable PUF to become challengeable, and reduce error correction requirements.

22.3: Using DNA to Safeguard Components in the Military Supply Chain and Protect Against Counterfeiting and Diversion **(11:10)**

J. A. Hayward
Applied DNA Sciences, Inc, Stony Brook, NY

Applied DNA Sciences has developed and patented technology related to the marking of products with DNA markers. These are large, complex, plant-derived, encrypted genomic sequences that can be developed to identify genuine products with absolute confidence.

22.4: Trust in the FPGA Supply Chain Using Physically Unclonable Functions **(11:30)**

J. Graf, J. Hallman, S. Harper
Luna Innovations, Inc., Roanoke, VA

Luna Innovations' Trust in Supply Tool (TST) uses physically unclonable functions to guarantee that Xilinx FPGA devices have not been substituted for counterfeit, downgraded, or alternate parts at any point in the supply chain or life of the FPGA.

LUNCH **(12:00–1:30)**

Session 23

THREE-DIMENSIONAL INTEGRATED CIRCUITS

Thursday, 25 March / 10:30 am – 12:00 pm / Tuscany 10

Chair: **M. Fritze**
DARPA/MTO, Arlington, VA

Co-Chair: **C. Lau**
Institute for Defense Analyses, Alexandria, VA

23.1: 3-D System-in-a-Stack Technologies (10:30)

V. Ozguz, J. Yamaguchi, R. Bindrup,
Irvine Sensors Corp., Costa Mesa, CA

P. Franzon
North Carolina State University, Raleigh, NC

A. Glezer, Y. Yoshi
Georgia Institute of Technology, Atlanta, GA

A 3-D System-in-a-Stack approach is used to demonstrate a computation module consisting of four field-programmable gate arrays and many memory components distributed in four tiers. The module includes integral thermal-management techniques and embedded passive components.

23.2: 3-D IC Hyper-Integration (10:50)

R. Patti
Tezzaron Semiconductor, Naperville, IL

The work that will be discussed relates to a mixed commercial and DARPA-sponsored Multi-Project 3-D integrated-circuit program. This program provides an excellent opportunity to not only demonstrate hereto-unseen 3-D integration capabilities with equally unique performance gains, but also a vehicle to incubate new data engine architectures.

23.3: Concept-to-Stack Design Flow for 3-D Integrated Systems (11:10)

L. McIlrath, W. Ahmed, J. Cote, K. Moulton, A. Yip
R3Logic, Waltham, MA

3-D integrated systems design presents many challenges that cannot be addressed with standard 2-D tools. A variety of tools for 3-D physical and system-level design, which was created and used within several DoD-funded programs, will be presented and their application in other contexts will be discussed.

23.4: High-Frequency Characterization of 3-D Interconnects for High-Performance Computing Applications (11:30)

S. J. Koester, F. Liu, A. M. Young, L. Shi, R. R. Yu, K. A. Jenkins, Y. Liu, S. Purushothaman, W. Haensch
IBM T. J. Watson Research Center, Yorktown Heights, NY

M. Lorsung, P. Zabinski, B. Randall
Mayo Clinic, Rochester, MN

Recent progress on the parasitic parameter extraction of the interlayer interconnects for two different wafer-to-wafer 3-D integration schemes developed at IBM will be presented.

LUNCH (12:00–1:30)

Session 24

SPACE POWER SYSTEMS

Thursday, 25 March / 10:30 am – 12:00 pm / Tuscany 11

Chair: **M. N. Lovellette**
Naval Research Laboratory, Washington, DC

Co-Chair: **J. P. Egan**
National Reconnaissance Office, Chantilly, VA

24.1: Lithium Ion: The Third Generation of Spacecraft Battery Technology (10:30)

S. A. Verzwyvelt
National Reconaissance Office, Chantilly, VA

The USG seeks to establish a trusted and assured supply of domestic lithium-ion battery cells for its spacecraft. The lithium-ion system will be the third generation of rechargeable batteries used on USG satellites. This paper will cover some satellite basics, contrast the lithium-ion system to previous nickel cadmium, and present nickel hydrogen systems. The ongoing lithium-ion program will also be described.

24.2: Modeling of Lithium Ion Cells and Batteries (10:50)

L. Cai, R. E. White
University of South Carolina, Columbia, SC

Physic-based mathematical modeling of a lithium-ion cell can be used to predict the life of that cell. It can also be used to predict the life of the battery pack using using such cells. The details of such models will be presented.

24.3: Carbon Nanotubes for Space Power Systems (11:10)

R. P. Raffaelle
National Renewable Energy Lab, Golden, CO

N. Harris
Rochester Institute of Technology, Rochester, NY

Next-generation nanotechnology-enabled power-system components have been developed, including such things as high specific power, Li-ion battery technology that employs carbon nanotubes (CNTs) for the anode material; high-efficiency solar cells using quantum-dot technology; and low-mass very-high-strength CNT-based wires and ribbons for thermal, electrical, and RF shielding applications. Near-term flight experience will be gained by integrating these components into a form suitable for a cube-sat demonstration.

24.4: NGAS Power Converter Achieves Record Efficiency (11:30)

F. D. Tan, T. Hsia, K. Yi, A. Paglinawan, T. Nye
Northrup Grumman Aerospace Systems, Redondo Beach, CA

A record 99% power efficiency for a 3.3-V output DC-to-DC converter has been demonstrated in an optimized point-of-load breadboard demonstration conducted by Northrup Grumman Aerospace Systems. Optimal electrical-energy-transfer results in reduced spacecraft power and thermal requirements. Employing this new technology could reduce power-distribution system losses by as much as 60% compared to current flight hardware.

LUNCH **(12:00–1:30)**

Session 25

TERAHERTZ TECHNOLOGIES

Thursday, 25 March / 1:30 – 3:00 pm / Tuscany 9

Chair: **M. J. Rosker**
DARPA/MTO, Arlington, VA

Co-Chair: **D. J. Radack**
IDA/ITSD, Alexandria, VA

25.1: THz Bipolar Transistors: Design and Process Technologies (1:30)

M. J. W. Rodwell, V. Jain, E. Lobisser, A. Baraskar, U. Singlsett, G. J. Burek. B. J. Thibeault, A. C. Gossard
University of California at Santa Barbara, Santa Barbara, CA

M. A. Wistey
University of Notre Dame, Notre Dame, IN

E. J. Kim, P. C. McIntyre
Stanford Universtity, Stanford, CA

B. Yu
Intel Corp., Santa Clara, CA

P. Asbeck, Y. Taur
University of California at San Diego, San Diego, CA

The device design, scaling laws, and process technologies for 64-nm (1-THz target f_t, 2-THz target f_{max}) InP heterojunction bipolar transistors will be reviewed.

25.2: Progress and Approach for Active Terahertz Electronics (1:50)

W. Deal, G. Mei, D. Scott, V. Radisic, K. Leong, S. Sarkozy, R. Lai, A. Gutierrez
Northrop Grumman Aerospace Systems, Redondo Beach, CA

The demonstration of THz transistors will transform the operating frequencies and capabilities of electronics systems. Concepts and data for THz InP HEMT and HBT transistors and measurements of a 0.48-THz amplifier will be presented.

25.3: Power Amplifier Development at 220 and 670 GHz (2:10)

K. Kreischer, M. Basten, D. Gallagher, J. Tucek
Northrop Grumman Corp., Rolling Meadows, IL

Northrop Grumman is developing compact power amplifiers based on vacuum-electronic technology. The goals are output powers of at least 50 W at 220 GHz, and 60 mW at 670 GHz. A review of the fabrication challenges will be presented.

25.4: Extended Interaction Klystrons for Terahertz Power Amplifiers (2:30)

D. Chernin, A. Burke, I. Chernyavskiy, J. Petillo
SAIC, McLean, VA

R. Dobbs, A. Roitman, P. Horoyski, M. Hyttinen, D. Berry
Communications and Power Industries, Georgetown, Ontario, Canada

K. Nguyen, V. Jabotinsky, D. Pershing, E. Wright
Beam-Wave Research, Inc., Bethesda, MD

T. Gaier, A. Skalare
Jet Propulsion Laboratory, Pasadena, CA

M. Blank
Communications and Power Industries, Palo Alto, CA

J. Calame, B. Levush
Naval Research Laboratory, Washington, DC

N. S. Barker, R. Weikle
University of Virginia, Charlottesville, VA

J. Neilson
Lexam Research, Redwood City, CA

J. Booske
University of Wisconsin, Madison, WI

Extended interaction klystrons (EIKs) have been demonstrated at frequencies up to 218 GHz, and the technologies on which they are based are poised to advance into the THz regime. This presentation will describe efforts to develop EIKs operating at 670, 850, and 1030 GHz, while meeting demanding requirements for gain, bandwidth, and efficiency.

Session 26

ULTRA-LOW-POWER SILICON ELECTRONICS

Thursday, 25 March / 1:30 – 3:00 pm / Tuscany 10

Chair: **M. Fritze**
DARPA/MTO, Arlington, VA

Co-Chair: **C. Lau**
Institute for Defense Analyses, Alexandria, VA

26.1: REESES: Rapid Efficient Energy Scalable Electronics (1:30)

B. H. Calhoun, S. Arrabi, S. Khanna, K. Craig, Y. Shakhsheer, J. Ryan, J. Lach
University of Virginia, Charlottesville, VA

REESES combines multi-VDD and dynamic voltage scaling to provide near-optimal energy savings when performance requirements vary. This paper will explain how the low overhead of REESES allows substantial power reduction in a data-flow processor and could improve efficiency for next-generation ultra-low-power 3-D FPGAs or multi-core processors.

26.2: Ultra-Low-Power Circuits with Autonomous, Data-Driven Power Supply Control (1:50)

G. Ansel, R. Jorgenson, L. Sorensen, D. Leet, M. Hagedorn, D. R. Lamb
Camgian Microsystems Corp., Starkville, MS

P. Ljung, C. Lage
Codetronix LLC, Oakland, CA

Subthreshold operation in CMOS circuits offers the potential for large energy savings. However, the uncertainty in timing in subthreshold is a major challenge for clocked designs. Clockless logic design techniques are presented, which can exploit the power-performance tradeoffs from subthreshold to normal mode while retaining ultra-low-power operation.

26.3: Demonstration of a Sub-1-V CMOS Compatible Ultra Low Energy Non-Volatile Memory Technology for Use in Discrete or Embedded Applications (2:10)

N. Derhacobian, S. Hollmer
Adesto Technologies, Sunnyvale, CA

A fully CMOS integrated non-volatile memory technology based on a reversible switching element that can be tuned to operate at voltages compatible to subthreshold CMOS for use in ultra-low-power applications is demonstrated. The physics of the cell operation will be presented along with characterization data on fully decoded arrays.

26.4: Demonstration of Optimized FDSOI Subthreshold Transistors with TiN Metal Gates for Ultra-Low-Power Operation (2:30)

S. A. Vitale, J. Kedzierski, N. Checka, P. W. Wyatt, C. L. Keast
MIT Lincoln Laboratory, Lexington, MA

FDSOI subthreshold operation transistors with TiN metal gates were fabricated to enable ultra-low-power circuits. Transistor engineering was optimized by device simulations, allowing significant capacitance reduction with modest speed impact. Through TiN gate work-function tuning, transistors were fabricated with narrow V_t distributions, I_{off}<10 pA/μm, and a subthreshold slope of 70 mV/decade.

Session 27

WIDE-BANDGAP OXIDE OPTOELECTRONICS AND DEVICES

Thursday, 25 March / 1:30 – 3:00 pm / Tuscany 11

Chair: **M. D. Gerhold**
Army Research Office, Durham, NC

Co-Chair: **W. D. Palmer**
Army Research Office, Durham, NC

27.1: Wide-Bandgap Oxide Optoelectronic Devices (1:30)

H. Lee
Tanner Research, Inc., Monrovia, CA

D. Wang
University of California, San Diego, La Jolla, CA

The vertical nanowire array enables light-absorption enhancement that improves the photoresponse of nanowire photodetectors. The substrate-independent growth promises great potential of integrating nanowire-based devices — intra-chip interconnects, single-photon detectors, and medical sensors and imagers — directly into CMOS technology and Si photonics. The development of vertical ZnO-nanowire UV-sensitive visible blind photosensors with high sensitivity will be presented.

27.2: BeZnO Solar-Bind UV Detectors (1:50)

H. W. White, Y. R. Ryu
MOXtronics, Columbia, MO

ZnO and its alloys have unique properties. These properties make ZnO and its alloys used for novel transparent/conductive oxide (TCO) electronic/optical devices. Radiation-hardness/high-frequency/high-power FETs, highly efficient LEDs/LDs, and solar/visible-blind UV photodiodes are among ZnO-based devices.

27.3: ZnO Bulk Growth, Thin-Film Epitaxy, and Device Applications (2:10)

J. Zhang, G. Cantwell
ZN Technology, Inc., Brea, CA

J. J. Song
ZN Technology, Inc., Brea, CA
and
University of California. San Diego, La Jolla, CA

Progress in the development of ZnO light emitters from ZN technology is reported, covering bulk, epitaxy, and devices. New approaches were investigated to further improve ZnO bulk crystals. ZnO LEDs have been fabricated based on improved p-type doping, and ZnMgO and ZnCdO ternaries were grown for heterostructure LEDs and LDs.

27.4: ZnO-based Optoelectronic Devices (2:30)

J. Nause
Cermet, Inc., Atlanta, GA

The recent advances in melt-grown ZnO substrate technology in both undoped and doped form will be presented. The optical properties of melt-grown ZnO will be presented, showing the high photoluminescent efficiency of this material. Epitaxial techniques used to grow ZnO emitter structures will be reviewed and the electrical properties of n- and p-type ZnO will be presented. MgZnO and ZnCdO alloy structures grown by these epitaxial techniques will be presented. Lastly, light-emitting diodes, incorporating ZnO, with various emission wavelengths will be presented.

Session 28

GENERAL POSTER SESSION

Thursday, 25 March / 9:00 am – 12:00 pm / Tuscany 7/8

Chair: **J. A. Franco**
Defense Threat Reduction Agency, Ft. Belvoir, VA

28.1: 17-GHz Instantaneous Bandwidth GaAs MMIC Power Amplifier

R. W. Zienkewicz, C. D. Grohndal, J. C. Pyon
ViaSat, Inc., Gilbert, AZ

A 17-GHz instantaneous bandwidth millimeter-wave (mmW) high-power-amplifier (HPA) MMIC using 0.15-µm GaAs technology is presented. Measured performance shows >2 W of output power and >25 dB of linear gain across 17 GHz of bandwidth with a peak output power of >5 W. This industry-leading design demonstrates excellent performance from 29 to 46 GHz and allows for multi-function operation in mmW SATCOM, RADAR, and other communications systems.

28.2: Honeywell 150-nm Rad-Hard Memory Products

G. Roosevelt, A. Kohil, J. Hobbs
Honeywell Microelectronics, Plymouth, MN

Honeywell has developed new 150-nm memory products to address the radiation-hardened marketplace and has a roadmap to continue to bring enhanced memory products to market. All of the memories are hardened both by design and by Honeywell's S150 150-nm SOI QML rad-hard process. This paper reviews the currently available memory product family's recent qualification and radiation test results. A summary of the roadmap to future enhanced products is included.

28.3: Wideband Phased-Array Demonstration

B. Garber, D. Kuhl
BerrieHill Research Corp, Centerville, OH

P. Buxa, T. Dalrymple, P. Watson, J. Buck, J. McCann, M. Longbrake, R. Neidhard,
AFRL, Wright-Patterson AFB, OH

A 16-element wideband (1–8-GHz) phased-array antenna has been assembled and tested as part of the AFRL Transformational Element Level Arrays (TELA) testbed. Integrating the Harris MCWESS antenna with novel element-level time-delay MMIC modules for beamsteering, the array demonstrates significantly broader instantaneous bandwidth than phase-shifter-based designs. The AFRL-developed array calibration technique will be described.

28.4: Built-In Self-Test (BIST) for Test Cost Reduction, In-field Testing, and Test-based Self-Calibration of High-Performance Analog and Mixed-Signal Systems

B. K. Vasan, J. Duan, C. Zhao, D. Chen, R. Geiger
Iowa State University, Ames, IA

A new method of extracting parametric test results from code density data from a fully integrated solution to testing high-performance ADCs using simple on-chip non-linear signal generators is introduced. Results show that the performance exceeds that of the best known BIST alternative while achieving a significant reduction in on-chip hardware complexity.

28.5: Simulation Study of Optically Triggered GaN/4H-SiC Heterostructure Vertical NPN Device

S. Bose, S. K. Mazumder
University of Illinois at Chicago, Chicago, IL

GaN and SiC have great potential for high-temperature and high-power electronics applications because of their attractive material properties, such as large bandgap energies, high breakdown fields, and high thermal conductivities. An attempt was made to study the turn-on/off characteristics and gain of an optically triggered GaN/4H-SiC heterostructure vertical NPN devices, and the results are compared with an optically triggered 4H-SiC structure. ATLAS device-simulation software package has been used for the above study. It was found that the GaN/4H-SiC heterostructure provides high current and fast switching.

28.6: Graphene Synthesis for Hall Bars and Field-Effect Transistors

S. Howell, L. Biedermann, T. Friedmann, C. Gutierrez, K. Leung, K. McCarty, T. Ohta, W. Pan, A. Ross, D. Wheeler
Sandia National Laboratories, Albuquerque, NM

Graphene layers are synthesized using both Ar-mediated epitaxial growth on SiC(0001) substrates and thermal decomposition of ethylene onto metal substrates. Photolithography is used to fabricate graphene Hall bars and graphene field-effect transistors. Preliminary electronic characterizations of these structures will be presented.

28.7: Rad-Hard Enabling Technologies

R. Dondero, C. Sumpter, P. Dodd, B. Draper, M. Shaneyfelt, D. Savignon, G. Patrizi, R. Olsson, T. Hill, T. Zipperian
Sandia National Laboratories, Albuquerque, NM

SNL manufactures ASICs in an SOI rad-hard CMOS technology realizing digital, analog, and mixed-signal circuits. This capability is enhanced with rad-hard NVM, high-voltage rad-hard FETs, point-of-load integrated controller chips, high-voltage rad-hard HBTs, MOS RadFETS, integrated waveguides, and silicon-microring resonators and AlN microresonators. The Design Center and Foundry are Trusted suppliers.

28.8: Integrated Wideband Millimeter-Wave Passive Front-Ends

J. Mruk, D. Filipovic
University of Colorado, Boulder, CO

H. Levitt
Navy Research Laboratory, Washingtonn, DC

Micromachined components constituting new multi-layer, integrated, Ku- to W-band receiver front-ends have been developed. This work demonstrates the highest degree of wideband millimeter-wave T/R integration with a potential of scaling into THz domain.

28.9: 3-D Spectral Sensor for Staring Communications

M. K. Yu, D. L. Abbey, H. Sasmazer, J. E. Landenberger, J. C. Ginther
Rockwell Collins, Cedar Rapids, IA

R. H. Olsson, S. L. Shinde
Sandia National Laboratories, Albuquerque, NM

A novel staring receiver architecture of 256-channel 3-D RF front-end spectral sensor covering 0.03–6.0 GHz is introduced. It is highly integrated and miniaturized using 3-D wafer-stacking technology and advanced RF signal processing and signal recovery. This implementation is envisioned to be a viable topology to process such a vast number of channels in parallel in a most compact spectral processor and is a promising technology for next-generation staring radio.

28.10: Photonic Crystal Based Demultiplexing at 1550 nm Using Alternating-Defect Coupled-Cavity Waveguides

J. W. Zeller
Naval Undersea Warfare Center, Newport, RI

F. C. Jain
University of Connecticut, Storrs, CT

A photonic-crystal-based demultiplexer incorporating alternating-defect coupled-cavity waveguides (AD-CCWs) will be presented. This demultiplexer design is significantly more compact than conventional arrayed-waveguide grating (AWG) devices. The simulation for six-channel demultiplexers operating at 1550 nm exhibited narrow spectral output linewidths ranging from 0.93 to 1.52 nm.

28.11: SLS: Compliant Miniature Wireless Networks for Defense and Homeland Security

T. Jannson, K. Walter, T. Forrester, K. Degrood, K. Nguyen, K. Lee, E. Gans
Physical Optics Corp., Torrance, CA

The proposed Secure Omni-(OSI) Layer Energy-Centric Information Carriers (SOLEICs) are miniature wireless devices such as network nodes, unmanned sensors, *etc.*, that combine System-Level-Solution (SLS) integration level (compliant with recent commercial devices) with unique synthesis of critical features highly exceeding the state of the art.

28.12: Thermal Considerations in Low-Cost T/R Module Design

J. Fiala, M. Overholt, S. Motakef
CapeSym, Inc., Natick, MA

D. Carlson
M/A-COM Technology Solutions, Lowell, MA

Commercial manufacturing technologies are being exploited to realize the T/R Module and Line Repeating Unit (LRU) for a prototype for the FAA Multifunction Phased Array Radar (MPAR) system. Thermal simulations with SYMMIC are used to evaluate the maximum total output power and duty cycle which can be achieved with this manufacturing technology.

28.13: Quantum-Dot Gate 3-state InGaAs FETs for Multi-Valued Logic Circuits and Advanced ADCs

F. Jain, S. Karmakar, F. Alalmoody, E. Suarez, M. Gogna, P.-Y. Chan, J. Chandy, B. Miller
University of Connecticut, Storrs, CT

E. Heller
RSoft Design Group, Ossining, NY

Experimental characteristics exhibiting intemediate “i” state in quantum-dot gate Si and InGaAs FETs is presented. Three-state FETs generally comprise two layers of cladded quantum dots (*e.g.*, GeOx-cladded Ge or SiOx-cladded Si dots). Application of three-state FETs is presented in the implementation of multi-valued logic and ADC circuits, resulting in significantly reduced device count.

28.14: Advanced Digital Beamformer using Silicon Germanium Technology

T. Quach, J. Buck, P. Buxa, M. Casto, G. Creech, T. Dalrymple, K. Groves, T. James, M. Longbrake, A. Mattamana, R. Neidhard, P. Orlando
Air Force Research Laboratory, Wright-Patterson AFB, OH

L. Johnson, R. Drangmeister, A. Messier
MIT Lincoln Laboratory, Lexington, MA

B. Kormanyos, R. Bonebright
The Boeing Company, Seattle, WA

A four-channel/X-band digital beamforming array has been demonstrated by employing advanced silicon germanium (SiGe) technology. The testbed demonstration is enabled by the development and integration of SiGe receiver modules that allow for coherent multichannel down-conversion to final IF at L-band and subsequent digitization and beamforming. Receiver module details and overall array performance will be described.

28.15: Characterization and Failure Mode Effects Analysis of High-Reliability Flip-Chip Attachment for Space Applications

S. Popelar, S. Thorne, D. Wilkin,
Aeroflex Colorado Springs, Inc., Colorado Springs, CO

Standards for the usage of flip-chip attachment in space electronics currently do not exist. The result of a design of experiment and physics-of-failure analysis of flip-chip attachment, leading to the identification of issues relevant to qualification of flip-chip attachment for space applications, will be presented.

28.16: BAE Systems' Diverse Microelectronics Capabilities: Two Trusted Foundries, One Mission

L. L. Gunter, S. Danziger, P. Chao, A. Pomerene, L. Bode, T. Bach
BAE Systems, Manassas, VA

BAE Systems strives to "Protect Those Who Protect Us" by providing our military with the best technology, the best equipment, the best training, and the best support in the world. The company's mission success is attained through utilization of its two trusted foundries to develop and deliver advanced electronic and optical components which are able to provide solutions to various application needs from smaller, lighter, focal-plane arrays for thermal weapon sights to novel, nonvolatile memory for space-based applications. The capabilities of each foundry and the diverse, advanced technologies currently being developed to provide our warfighters with solutions that will continue to give them the advantage in combat will be discussed.

28.17: Updated Total-Dose-Radiation Test Results for IBM's 130-nm 8SF Process

J. W. Rooks
AFRL/RI, Rome, NY

L. Weyna
ITT Corp., Rome, NY

D. Alexander
AFRL/RVSE, Kirtland AFB, NM

Updated results from total-dose testing on a six-processor die that included 12 Mbytes of embedded DRAM will be presented. The hardness of IBM's 130-nm 8SF CU-11 standard cells, SRAMS, inputs, outputs, and DRAM was determined. These are the new results from the Future Work section of GOMAC 2008 paper 24.4.

28.18: High-Performance Electronics Integration in Flexible Technology

R. Chaney, D. Hackler
American Semiconductor, Inc., Boise, ID

A new flexible, ultra-low-power (ULP), silicon-on-polymer (SOP) technology for low-cost high-performance CMOS will be presented. This technology is useful in 3-D circuit integration and solves problems facing flexible electronics where high-temperature processing and flexible requirements preclude the use of standard CMOS and performance requirements preclude the use of organic thin-film transistors or other exotic metal-oxide materials.

28.19: Radiation Hardness by Design Demonstrations Using 45-nm SOI

A. Kleinosowski, T. Amort, W. Snapp
Boeing Research and Technology, Seattle, WA

Prototype chips have been designed, fabricated, and tested using commercial 45-nm SOI device technology. These prototypes demonstrate the feasibility of radiation hardness by design with nano-scale floating-body transistors.

28.20: V-Qualified Strategic Rad-Hard Technology for the Present and Future

S. Doyle, J. Ross, D. Pirki, J. Rodgers, N. Haddad, E. Chan
BAE Systems, Manassas, VA

Technology status and qualification test results on a deep submicron rad-hard technology featuring a 16-MB SRAM family, ASIC Library, and SERDES will be presented.

Session 29

STUDENT POSTER SESSION

Thursday, 25 March / 9:00 am – 12:00 pm / Tuscany 7/8

Chair: **J. A. Franco**
Defense Threat Reduction Agency, Ft. Belvoir, VA

29.1: Characterization of Control Bit Errors in the MIPS R2000 Microprocessor

D. B. Limbrick, E. J. Ossi, C. T. Toomey, W. H. Robinson, B. L. Bhuva
Vanderbilt University, Nashville, TN

Soft errors can alter the correct execution of code within a microprocessor, particularly if control logic is compromised. The vulnerability of the control logic of a MIPS R2000 processor through software-based fault injection were determined. Results showed that over 25% of the injected faults were visible at the output.

29.2: Qualitative Analysis of Single-Event Latchup Trends in 180-nm Bulk CMOS Using 2-D TCAD Simulation

C. A. Dinkins, J. S. Kauppila, L. W. Massengill
Vanderbilt University, Nashville, TN

TCAD simulations at the 180-nm CMOS technology node show high latchup dependence on V_{DD} bias. General qualitative latchup trends are analyzed for this node with an emphasis on bias across LET, angle, and with and without mitigation techniques.

29.3: Interfacing Metamaterials and HEMT Technologies in the THz Regime

D. Shrekenhamer, W. Padilla
Boston College Physics, Chestnut Hill, MA

Metamaterials with resonant response in the THz regime have been integrated with HEMT technologies to provide a new form of control and tunability. The potential of this device suggests capability of reaching state-of-the-art modulation and find usage in wide variety of applications.

29.4: Volumetric Switched Beam Array at the 60-GHz Band for High-Data-Rate Connectivity

W. F. Moulder, W. Khalil, J. L. Volakis
The Ohio State University, Columbus, OH

A 60-GHz volumetrically scanning switched beam network for high-data-rate wireless communication is proposed. The network allows scanning in multiple spatial planes with only a single switching stage. It is mated with an array of stacked patch elements and operates across the entire unlicensed band.

29.5: Bias Adaptation Loadline Analysis for Adaptable Power Amplifiers

D. L. Ryan, M. A. Reece
Morgan State University, Baltimore, MD

Output power and efficiency of a communication system's transmitter are two dynamic requirements that can be improved with an adaptable communication system. Bias adaptation updates the transmitter DC bias to optimize efficient use of power in the transmitter. Mathematical analysis was performed to assist in identifying a more efficient bias.

29.6: Passive Intermodulation Distortion in Antennas

J. R. Wilkerson, M. B. Steer
North Carolina State University, Raleigh, NC

Passive intermodulation distortion (PIM) dependencies on antenna width, length, thickness, and substrate parameters are analyzed resulting in design guidelines for low-distortion antennas. A 1-GHz rectangular patch antenna is manufactured on a sapphire substrate and is characterized for PIM dispersion, exhibiting excellent agreement with the derived model.

29.7: Robust Automated Modeling of Distributed Microwave Circuits Using Genetic Algorithms

C. S. Saunders, M. B. Steer
North Carolina State University, Raleigh, NC

Accurately modeling the behavior of a distributed microwave circuit or communications channel within a circuit simulator is critical when analyzing the transient performance and dynamic range of the incorporating circuit. Often, these models need to be generated from measured responses which may be significantly corrupted by noise. The utilization of a genetic algorithm is proposed as a solution to address the constraints imposed by fitting a model to measured data.

29.8: Signature-Based Detection of Hardware Trojans with Voltage Stepping

T. Reece, W. H. Robinson, B. L. Bhuva
Vanderbilt University, Nashville, TN

Signatures for detecting hardware Trojans can be generated from the change in shape of the transient current response as supply voltage is reduced. These are compared with responses of physical chips with questionable content to identify trusted chips. Simulation results show significant differences between circuits with and without Trojans despite large induced variations.

29.9: Passive Intermodulation Mitigation Techniques

A. Christianson, J. Henrie, W. J. Chappell
Purdue University, West Lafayette, IN

Several methods of mitigating passive intermodulation distortion are presented. First, a cancellation method using multiple PIM sources will be described. Then, the placing of PIM-producing non-linearities in current standing-wave minima will be described. Lastly, the mitigating effect of a DC magnetic field on the PIM produced by ferromagnetic components will be examined.

29.10: High-Voltage/High-Power Amplifier Implementation with 0.12 μm SiGe HBTs

T. J. Farmer
Army Research Laboratory, Adelphi, MD

M. E. Zaghloul
The George Washington University, Washington, DC

A. Darwish
The American University in Cairo, New Cairo, Egypt

A two-stage high-voltage/high-power (HiVP) power amplifier has been designed and implemented using a 0.12-μm SiGe HBT process. The purpose of this work is to provide a first implementation of the HiVP device configuration using silicon germanium (SiGe) heterojunction bipolar transistors (HBTs) at millimeter-wave frequencies. The HiVP configuration allows for very large output voltage swings leading to high output power. The intention of this paper is to (1) provide a broad framework for simulation of a HiVP in any millimeter-wave capable technology and (2) to discuss a 0.12-μm SiGe HBT implementation of the HiVP at the millimeter-wave frequency of 30 GHz.

29.11: Parametric Approach to Determining the Optimum Geometry for PZT MEMS Switches Intended for Digital Applications

R. Proie Jr., M. Zaghloul
The George Washington University, Washington, DC

R. Polcawich, J. Pulskamp
Army Research Laboratory, Adelphi, MD

PZT MEMS switches were designed for low-frequency digital applications. The devices were fabricated with a variety of design variables, including actuator length/width, contact dimensions, actuator/contact geometries, and contact metallurgy (Au/Pt, Au/Ru, or Au/Au). The yield, actuation voltage, switching speed, and contact resistance were measured to determine each design's performance.

29.12: Third-Order Distortion of Sound Fields

G. Garner, J. R. Wilkerson, M. B. Steer
North Carolina State University, Raleigh, NC

Measurements for two ultrasonic tones mixing in air, producing highly directional third-order intermodulation tones, will be presented. Hermite-Gaussian spreading of the two fundamental beams produces extremely narrow (3°) overlapping peaks where fundamental pressures become high enough to generate third-order terms. By modeling Hermite-Gaussian spreading, it is possible to predict the propagation direction and amplitude of intermodulation tones for applications in covert communications and acoustic probing.

29.13: Single-Event Characterization of a 90-nm Bulk CMOS Digital Cell Library

N. M. Atkinson, A. F. Witulski, W. T. Holman, B. L. Bhuva, L. M. Massengill, J. D. Black
Vanderbilt University, Nashville, TN

This work describes the basic methodology and results of a characterization of single-event transients in the DARPA/DTRA-supported Boeing RHBD digital cell library, with about 500 cells. Worst-case single-event transients are simulated in logic cells using TCAD. The results give insight into single-event sensitivities of logic cell design.

29.14: Radiation Hardened Quantum-Dot Floating-Gate Nonvolatile Memory

E. Suarez, M. Gogna, F. Al-Amoody, S. Karmakar, J. Ayers, F. Jain
University of Connecticut, Storrs, CT

E. Heller
RSoft Design Group, Ossining, NY

Preliminary data on GeOx-cladded Ge quantum-dot gate nonvolatile memories using SiO_2 as well as lattice-matched ZnS/ZnMgS/ZnMgSSe tunnel insulators will be presented. Electrical characteristics for both structures show threshold shifts after "Writing" using drain pulse. Preliminary data on fabricated rad-hard silicon-on-insulator quantum-dot gate-memory devices will also be presented.

29.15: Carbon Nanotube Gate Si FET for Protein Sensing Applications

R. Croce, R. Setya, P.-Y. Chan, F. Jain
University of Connecticut, Storrs, CT

A carbon-nanotube gate silicon FET sensor for the detection of proteins will be presented. Here, carbon nanotubes form the gate where proteins are functionalized, via amine-terminated single-stranded DNA (ssDNA) aptamers employing carbodimide chemistry on carboxylated CNTs.

29.16: Cell-based Electro-Thermal Simulation of a Digital 3-D IC Using an Extracted Physical Network

T. R. Harris, S. Priyadashi, S. Melamed, M. B. Steer, R. Davis, P. Franzon
North Carolina State University, Raleigh, NC

C. Ortero
Cornell University, Ithaca, NY

Transient electro-thermal simulation of a three-dimensional circuit is reported that uses a cell-based simulation to provide selected transistor thermal profile while providing advantages of hierarchical simulation. Simulations are compared favorably to measurements for a 3-D IC clocking at a maximum of 6 GHz.

29.17: 3-D Integrated SAR Processors

T. Thorolfsson, P. Franzon
North Carolina State University, Raleigh, NC

The use of 3-D integration to reduce the power consumption and increase the memory bandwidth of synthetic aperture radar processors will be presented. The two systems, one using SRAM and the other using DRAM, that do so in different ways will be described.

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