GOMACTech-11

Government Microcircuit Applications and Critical Technology Conference

PROGRAM

"Securing the Future through Rapid Technology Insertion"

March 21 – 24, 2011

DoubleTree Hotel
Orlando, Florida

www.gomactech.net

GOMACTech-2011
FINAL PROGRAM
CONTENTS

WELCOME

The GOMACTech-11 Program Committee warmly welcomes you to this year's conference in Orlando, Florida. GOMACTech is the pre-eminent conference for the review of developments in microcircuit applications for government systems. GOMACTech, established in 1968, is an unclassified, export-controlled event that requires all participants to be U.S. Citizens or legal U.S. Permanent Residents.

This year, our conference theme, *"Securing the Future through Rapid Technology Insertion"* focuses on the technologies available in CONUS fabs where a portion of the production flow can be secured. While electronics have given the U.S. primary advantage entering the 21st century, an unintended consequence of a fully globalized commercial sector has arisen, where economic and military adversaries can access comparable technologies. Our intent is to highlight emerging circuit and device technologies that can provide leap-ahead capability for government interests but with compatibility to pertinent commercial IP.

The conference follows an established format, with specific "tracks" resulting from substantial discussion from this year's Technical Program Committee. The technical sessions comprise contributed and solicited papers, including oral presentations and a Thursday morning (March 24) Poster Session. We will highlight the work of student contributors in a special competition section of the Student Poster Session.

The tracks for GOMACTech-11 include:

- RF integrated circuits, where commercial markets are driving many aspects of the area, but where substantial gains for government applications can be made as many of the critical figures-of-merit translate to clear increases in capability.
- Graphene, as a representative of novel materials, with the subsequent question of how best to integrate heterogeneous materials to glean the maximum advantage for each respective material, whether within the confines of an individual device or in the context of a 3D integrated circuit.
- Power consideration of the system layout with the inclusion of power design at the inception of projects has become an engineering imperative with the drive for fielded lifetime manifesting itself as a requirement for 21st-century embedded systems.
- Trust in the IC supply chain will continue as a major area of discourse.

The topical sessions will focus on developments and accomplishments, ranging from components to systems within selected on-going government-sponsored programs. Specific sessions include:

- Graphene (Electronics & RF Electronics)
- 3DIC I & II (session II comprises a multi-paper session covering the Lincoln Labs wafer suite)
- Emerging Semiconductor Tech I & II
- Adaptive RF / BiST and Calibration
- Advanced RF/Mixed Signal Circuits
- RF Circuits for Wireless Sensors
- Trusted Electronics Research
- Trust in ICs
- Trusted Electronics Applications I & II
- Antenna Applications
- Phased-Array Beamforming Technology
- Advanced Power Amplifiers (RF to mm-wave)
- GaN Reliability

- Power Electronics (I & II)
- Power Management for RF Electronics
- Radiation-Hardened Microelectronic Design
- Non- Silicon Rad-Hard Microelectronic Technologies
- Fault-Tolerant Computing for Space Systems
- Space Computing
- Extreme Environment Systems
- Nanowire- and CNT-Based Electronics
- N/MEMs Relays for Micromechanical
- Sub-Millimeter-Wave Vacuum Electronics
- Optical Interconnects for Military Platforms

The first tutorial is the second national *Trusted Suppliers Summit*. Our objective is to gather members of industry and government agencies representing the interests of integrated-circuit and electronics producers who are focused on serving defense and aerospace applications that are trusted. This summit is organized by Harry Kelzi from Teledyne. Some of the key issues include accreditation activity and criteria, emerging defense policy and demand for trusted supplies, trust solutions, and opportunities for industry to work together and with government for further progress in this area. The program begins with status and updates on DoD policy, the accreditation process, and programmatic initiatives. Later, industry representatives will discuss their capabilities. In the afternoon session, a moderated discussion, with panelists representing both industry and government, will take on topics that are frequently being asked by industry participants.

The second tutorial, *SOI-Enabled Technologies for 3D Circuit Integration and Ultra-Low-Power Applications*, will discuss how the unique attributes of silicon-on-insulator (SOI) technology are being exploited to enable complex three-dimentional (3D) circuit integration. The first half will include discussion of the factors driving 3DIC development, approaches to implementation, and realized examples. The second portion will discuss how ultra-low-power electronics can expand the technological capability of hand-held and wireless devices by dramatically improving battery life and portability for applications such as space-based sensors, unattended ground-based sensors, and embedded medical devices. We will discuss ultra-low-power process optimization, show device and simple circuit results and talk about future scaling issues along with proposed solutions to sub-40-nm gate lengths.

The third tutorial, *Securing the Full End-to End Flow of Electronics: Technical Policy & Acquisition Implications*, will convene with a moderated panel discussion of the primary issues in design, fab, packaging & test, and reliability, as they pertain to leading-edge electronics and the constraints on domestic availability for critical USG applications. Within the context of a fully globalized market for production and research, the aim of this tutorial is to document recommendations that will counter the exodus overseas of technical leadership within microelectronics.

The conference formally opens on Tuesday morning (March 22) with an outstanding Plenary Session including a Keynote presentation by The Honorable Zachary Lemnios, Director, Defense Research and Engineering, Department of Defense. Following the Keynote, there will be three Kilby Lecture speakers:

- ***Dr. Eli Yablonovitch***, *Nortel Distinguished Professor and Director of the Center for Energy Efficient Electronics Science, University of California, Berkley*
- ***Dr. Robert Trew***, *Division Director, Electrical, Communications, and Cyber Systems, National Science Foundation*
- ***Mr. Keith Uebele***, *Principal Strategist, Intel Labs, Strategy & Planning*

The Plenary, Technical, and Topical Sessions are the major venues for information exchange at the conference. Other opportunities for technical interaction are provided through the Exhibit Program that includes major IC manufacturers and commercial vendors of devices, equipment, systems, and services from nearly all facets of the electronics business. The exhibition opens on Tuesday at noon and runs through Wednesday (March 23) until 4:00 pm. On Tuesday evening, attendees can mix in a relaxing atmosphere at the Exhibitors' Reception. The Wednesday Luncheon Keynote speaker will be **Mr. Dave Davis**, *Chief, Systems Engineering Division, Air Force Space and Missile Center, Los Angeles Air Force Station, California.* Wednesday evening features the conference banquet, which will be held at the ***House of Blues*** followed by a performance by ***Cirque du Soleil***. On Thursday morning (March 24), there will be a Poster Session that includes our inaugural student poster competition. The Thursday Luncheon Keynote speaker will be ***Mr. Don Parman,*** *Chief, Strategic Planning, Defense Threat Reduction Agency, Ft. Belvoir, Virginia.*

This year's strong technical program reflects the hard work and enthusiasm of the GOMACTech-11 Technical Program Committee. The committee members aggressively sought out and selected particular topics and areas for presentations, and the quality of the conference certainly reflects this effort. It is our hope and belief that GOMACTech-11 will be a rewarding experience for all participants. We appreciate your support.

John Franco
Conference Chair

Romeo Del Rosario
Technical Program Chair

REGISTRATION

All GOMACTech-11 sessions will be held at the DoubleTree Hotel in Orlando, Florida. Both check-in and on-site registration will take place in the hotel's Convention Center lobby.

Conference check-in and on-site registration hours:

Monday, 21 March – 7:00 am – 8:00 am (Tutorial 1 only)
Monday, 21 March – 8:00 am – 5:00 pm
Tuesday, 22 March – 7:00 am – 5:00 pm
Wednesday, 23 March – 7:00 am – 5:00 pm
Thursday, 24 March – 7:00 am – 3:00 pm

SECURITY PROCEDURES

The GOMACTech Conference is an Unclassified, Export-Controlled event that requires participants to be U.S. Citizens or legal U.S. Permanent Residents. All registrants must provide proof of U.S. Citizenship or Permanent Resident status prior to being permitted entry into the conference. Additionally, a signed **Non-Disclosure Statement** will be required.

You may prove U.S. citizenship with any of the following:
U.S. Passport
Birth Certificate **AND** valid government-issued photo ID
Naturalization Certificate **AND** valid government-issued photo ID

The following are NOT proof of citizenship:
Voter registration card
Driver's license

GOMACTech TUTORIALS

Three tutorials of interest to the GOMACTech community are a special feature of the conference. The tutorials are all being held on Monday, 21 March. There is no additional fee for the Tutorials 2 & 3, but individuals must be registered for the Conference and must indicate their intention to attend a specific tutorial on their registration form. Tutorial 1 includes a lunch. The fee for Tutorial 1 is $20.

Tutorial 1: 2nd National Trusted Suppliers Summit Tutorial

Monday, 21 March, 7:00 am – 4:00 pm
DoubleTree Hotel, Universal Center

Organizer:
Harry Kelzi, Teledyne

The 2nd National Trusted Supplier Summit will gather members of industry and government agencies representing the interests of integrated circuit and electronics producers focused on serving trusted Defense and Aerospace applications. Some of the key issues to be discussed include accreditation activity and criteria, emerging defense policy and demand for trusted suppliers, trusted solutions, and opportunities for industry to work together with the Government for further progress in this area.

The Trusted Supplier Steering Committee has been actively organizing this event throughout the year leading up to the Summit in order to provide improved visibility and raise awareness within the Defense and Industry community.

The 2nd National Trusted Supplier Summit will be addressing the concerns and requests of both industry and government agencies that were raised in the first Summit. This will be the opportunity to reconvene and better address those concerns and attempt to further define and provide solution oriented road map.

The early part of the day will consist of appropriate government representatives providing status and updates on DoD policy, the accreditation process, and programmatic initiatives. Later in the morning, an industry panel will address issues and concerns relating to the Trusted Supplier Program. The afternoon session will convene with a moderated panel discussion representing both industry and government and will take on topics frequently asked by Industry accredited suppliers.

Organizations that are accredited by the time of the Summit are invited to participate. Suppliers who are planning to become a certified Trusted Supplier are urged to attend because this event will be of utmost interest and beneficial to your organization in understanding, promoting, and networking within the Trusted Supplier community.

Agenda

7:00 am	Registration/Continental Breakfast
8:00 am	Opening/Introduction *Harry Kellzi, Teledyne*
8:15 am	Government Welcome & Trusted Foundry Program *Sonny Maynard, DDRE*
8:30 am	Supply-Chain Risk Management (SCRM) *Kristen Baldwin, DDRE* (Invited)
9:00 am	Navy SCRM Efforts *Debra Gookin, SPAWAR*
9:30 am	Defense Microelectronics Activity *David Pentrack, DMEA*
9:50 am	**BREAK**
10:05 am	NSA Perspective *Tony Chernoske, NSA*
10:30 am	Trusted Supplier Steering Group Presentation *Harry Kellzi, Teledyne*
11:00 am	**Trusted Supplier Steering Group Panel** *Harry Kellzi, Teledyne,* ***Moderator*** **Panelists** *Peter Behrens, National Semiconductor* *Wayne DeCarlo, Photronics* *Michael Fitzpatrick, Northrop Grumman* *Greg Panning, Honeywell International* *Stewart Ocheltree, BAE Systems* *Roger Van Art, Aeroflex*
12:00 pm	**Lunch**
1:30 pm	Industry OEM Perspective
2:30 pm	**Break**
2:45 pm	**Government Panel Discussion** *Charles Cerny,* ***Moderator***
4:00 pm	Wrap-up/Adjourn

Tutorial 2: Securing the Full End-to-End Flow of Electronics: Technical Policy & Acquisition Implications

Monday, 21 March, 1:00 – 5:00 pm
DoubleTree Hotel, Goldcoast Room

Organizer:
Paul Amirtharaj, Army Research Laboratory

Trusted foundry is the first step. What about the rest of the flow? This panel session will discuss the primary issues in the four major sections of IC flow: design, fab, packaging & test, and reliability, as they pertain to leading-edge electronics and the constraints on domestic availability for critical USG applications. (within a fully globalized market for production and research).

Presenters:
Paul Amirtharaj, *Army Research Laboratory*
Romeo delRosario, *Army Research Laboratory*
John Penn, *Army Research Laboratory*
Bill Spaeder, *Berkeley Design Associates*
Mike Liehr, *CNSE/IBM*
Ken Decker, *Triquint Seminconductor*
Doug Goodman, *Ridgetop*

Tutorial 3: SOI-Enabled Technologies for 3D Circuit Integration and Ultra-Low Power

Monday, 21 March, 1:00 – 5:00 pm
DoubleTree Hotel, Sun and Surf Room

Organizers:
Les Palkuti, DTRA

This two-part Tutorial will discuss how the unique attributes of silicon-on-insulator (SOI) technology are being exploited to enable complex three-dimentional (3D) circuit integration and to realize a CMOS process technology optimized ultra-low-power operation.

The first presentation will begin with a discussion of the factors driving the development 3D circuit-integration technologies and provide a broad overview of the many different 3D integration approaches currently being explored throughout the semiconductor industry. The presentation will then focus on one of these approaches: a 3D circuit-integration technology that exploits the advantages of SOI technology to enable wafer-level stacking and micrometer-scale electrical interconnection of fully fabricated circuit wafers. The presentation will conclude with some examples of advanced focal planes and 3D circuits and microsystems which have been realized in this technology.

Presenters:
Craig L. Keast, *MIT Lincoln Laboratory*
Steven A. Vita, *MIT Lincoln Laboratory*

LUNCH SPEAKERS

Lunch will be provided on Tuesday, Wednesday, and Thursday. Both Wednesday and Thursday lunches will include presentations of great interest to the GOMACTech community. The Wednesday Luncheon Keynote speaker will be Dave Davis, Chief, Systems Engineering Division, Air Force Space and Missile Center, Los Angeles Air Force Station, California. Thursday's Luncheon speaker will be Don Parman, Chief, Strategic Planning, Defense Threat Reduction Agency, Ft. Belvoir, Virginia.

EXHIBITION

An exhibition comprised of commercial vendors exhibiting products of interest to the GOMACTech community is an integral part of the conference. All attendees are reminded to visit the exhibition when they have some free time. The Exhibit Hall is located in the hotel's Citrus Crown Ballroom. Coffee breaks will be held in the exhibit area when they coincide with the exhibition's hours of operation. On Tuesday evening, an Exhibitors' Reception, where attendees can mix in a relaxing atmosphere of food and good spirits, will be held. Exhibition hours are as follows:

Exhibition hours are as follows:

Tuesday, 23 March	12:00 pm – 8:00 pm
Wednesday, 24 March	9:00 am – 4:00 pm

List of Exhibitors

Aeroflex Divisions
Analog Bits
BAE Systems
Boeing
Cobham
Coherent Logix
Corwil Technology Corp.
Cypress Semiconductor
Endicott Interconnect Technologies, Inc.
Evans Analytical Group
Honeywell
HRL
IBM
Integra Technologies, LLC
Interconnect Systems, Inc.
Kilopass Technology, Inc.
M/A-COM Technology Solutions
Mobile Semiconductor Corp.
MOSIS
National Reconnaissance Office
National Semiconductor Corp.
NNSA's National Manufacturing Office
Northrop Grumman Corp
ON Semiconductor
Peregrine Semiconductor
Photronics, Inc.
Rochester Electronics
RTI International
Sandia National Laboratories
Silvaco Data Systems
SVTC Technologies
Synopsys, Inc.
Tahoe RF Semiconductor, Inc.
TAPO (Trusted Access Program Office)
Tektronix Component Solutions
Tela Innovations, Inc.
Teledyne Microelectronics
Teradyne Global Services
Tower Jazz
TriQuint Semiconductor

WEDNESDAY EVENING SOCIAL

Dinner at the House of Blues

Performance of "La Nouba, Cirque du Soleil"

The GOMACTech 2011 Special Event is truly a special event. It includes dinner at The House of Blues -- southern-inspired cuisine -- at the Walt Disney World Resort. Dinner will be followed by a performance of *La Nouba, Cirque Du Soleil*. The show name "La Nouba" originates from the French phrase "faire la nouba," which means to party, to live it up. It is a world where dreams and reality intertwine as the urban and circus worlds meet on stage. Blending acrobatics, dazzling choreography, whimsical characters and live music, La Nouba stimulates our imagination from beginning to end.

Buses will leave the DoubleTree Hotel at 6:00 pm
Tickets should be purchased in advance along with your conference registration:
Adults $25, Children (13 and under) $15.

HOTEL ACCOMMODATIONS

Steps from the Universal Orlando Resort, the Doubletree Hotel is a short drive from Orlando's world-famous theme parks, shops, restaurants, golf courses, entertainment and sports venues, and exciting attractions, such as Universal Studios, City Walk, Walt Disney World, SeaWorld Orlando, Discovery Cove, and the Orange County Convention Center. The Doubletree Hotel is less than 10 minutes from the Mall at Millenia, Festival Bay Mall, and prime outlets.

GOMACTech has reserved a block of rooms at the hotel at a special rate of $104 single or double. These rates are exclusive of applicable state and local taxes.

Reservations may be made on line at http://doubletree.hilton.com/en/dt/groups/personalized/M/MCOUNDT-GOM-20110319/index.jhtml?WT.mc_id=POG

Or by calling the hotel reservations department at 407/351-1000. Be sure to note that you are attending GOMACTech.

The deadline for reservations from the GOMACTech block is Friday, 25 February 2011.

CONFERENCE CONTACT

Anyone requiring additional information about GOMACTech should contact the Conference Coordinator, Glenys Natera, GOMACTech, 411 Lafayette Street, Suite 201, New York, NY 10003 (212/460-8090 x217), gnatera@pcm411.com.

GOMACTech-10 PAPER AWARDS

Paper awards based on audience evaluations from GOMACTech-10 will include the George Abraham Outstanding Paper Award, a Meritorious Paper Awards, and a Best Poster Paper Award. Presentation of these well-deserved awards will be made at the Plenary Session on Tuesday morning in Universal Center. The GOMACTech-10 winners are:

The George Abraham Outstanding Paper Award (26.2)
W. T. Holman, L. W. Massengill, B. L. Bhuva, A. F. Witulski, and D. Loveless, *ISE/Vanderbilt University*
"*Recent Advances in Radiation-Hardened-by-Design Analog and Mixed-Signal Design*"

Meritorious Paper Award (1.2)
C. Fulton and W. Chappell, *Purdue University*
"The Purdue Digital-Array-Radar Testbed"

Best Poster Paper Award (28.8)
J. Mruk and D. Filipovic, *University of Colorado*
H. Levitt, *Navy Research Laboratory*
"Integrated Wideband Millimeter-Wave Passive Front-Ends"

RATING FORM / QUESTIONNAIRE

Don't forget to vote for your favorite presentation this year before you leave the conference. A rating form/questionnaire is being handed out at conference check-in. To encourage submission of these forms, GOMACTech has a special gift for all attendees submitting a completed form. Please turn your form in at the Conference registration desk when you leave the Conference to receive your gift item.

SPEAKERS' PREP ROOM

The St. Johns Room has been designated as the speakers' preparation room and will be available during the hours the conference registration desk is open. Speakers are encouraged to use the St. John Rooms facilities to ensure compatibility with the meeting's AV equipment. Speakers having difficulties should request, at the conference registration desk, to see an AV operator. **Speakers are also asked to be at their assigned presentation room 30 minutes before the sessions begins to meet with their session chair.** An AV operator will be assigned to each technical session room.

CD-ROM PROCEEDINGS

The GOMACTech CD-ROM Proceedings, containing searchable, condensed versions of submitted papers presented at the Conference will be distributed to all registrants. Additional copies of the CD-ROM can be purchased at the Conference at a cost of $40.00 per CD.

Previously published as the GOMAC Digest of Technical Papers, Volumes I – XXVII, this publication is the only record of the conference. Previous GOMAC Digests will, upon request, be made available to qualified Defense Technical Information Center (DTIC) users. Please call 1-800-225-3842 for bound or microfiche copies. Past Digests can be ordered by calling the above number and identifying the following accession numbers (please note that GOMAC was not held in calendar years 1985 and1995):

GOMAC-84 B113271	-86 B107186	-87 B119187
-88 B129239	-89 B138550	-90 B150254
-91 B160081	-92 B169396	-93 B177761
-94 B195015	-96 B212362	-97 B222171
-98 B235088	-99 B242763	-00 B254138
-01 B264749	-02 B275146	-03 M201604
-04 M201663	-05 M201849	-06 M202011
-07M202134	-08 M202438	-09 M202646

INFORMATION / MESSAGE CENTER

The Information/Message Center will be located adjacent to the GOMACTech Registration Desk at the DoubleTree Hotel. The message center telephone number for incoming calls is 407/351-1000. Callers should ask to be transferred to the GOMACTech Registration Desk.

PARTICIPATING GOVERNMENT ORGANIZATIONS

Participating Government Organizations of GOMACTech-10 include: Department of Defense (Army, Navy, Air Force) ... National Aeronautics and Space Administration ... Department of Commerce (National Institute of Standards and Technology) ... National Security Agency ... Department of Energy (Sandia National Laboratories) ... Department of Energy (National Nuclear Security Administration) ... Defense Logistics Agency ... Department of Health and Human Services ... Defense Threat Reduction Agency ... Defense Advanced Research Projects Agency ... Advisory Group on Electron Devices ... Central Intelligence Agency ... National Reconnaissance Office

GOMACTech WEB SITE

Information on GOMACTech may be obtained through its Web site at www.gomactech.net.

TUESDAY, 22 MARCH

PLENARY SESSION

Tuesday, 22 March / 8:30 am – 12:00 pm / Universal Center

Opening Remarks **(8:30–8:45)**

John Franco, GOMACTech-11 General Chair
Defense Threat Reduction Agency, Ft. Belvoir, VA

GOMACTech-10 Awards **(8:45–9:00)**

Keynote Address **(9:00–10:00)**

The Honorable Zachary J. Lemnios
Director, Defense Research and Engineering, U.S. Department of Defense, Washington, DC

"Department of Defense Strategy for Microelectronics"

BREAK **(10:00–10:30)**

Jack S. Kilby Lecture Series **(10:30–12:00)**

Dr. Eli Yablonovitch
Nortel Distinguished Professor and Director of the Center for Energy Efficient Electronics Science, University of California at Berkeley, Berkeley, CA

"Nano-Photonic Silicon Circuits as a Commercial Technology"

Dr. Robert Trew
Division Director, Electrical, Communications, and Cyber Systems, National Science Foundation, Arlington, VA

"Next-Generation Electronic Devices for Advanced Systems"

Mr. Keith Uebele
Principal Strategist, Strategy and Planning, Intel Labs, Hillsboro, OR

"The Future of Silicon"

LUNCH **(12:00–1:30)**

Session 1

GRAPHENE RF ELECTRONICS

Tuesday, 22 March / 1:30 – 3:00 pm / Space Coast

Chair: **M. Fritze**
DARPA/MTO, Arlington, VA

Co-Chair: **C. Lau**
Institute for Defense Analyses, Alexandria, VA

1.1: Graphene-on-SiC and Graphene-on-Si MOSFETs with Record Mobility on 75-mm Wafers (1:30)

J. S. Moon, D. Curtis, S. Bui, D. Wheeler, S. Kiim, T. Marshall
HRL Laboratories, LLC, Malibu, CA

D. K. Gaskill, P. M. Campbell
Naval Research Laboratories, Washington, DC

P. Asbeck
University of California at San Diego, La Jolla, CA

G. Jernigan, B. VanMil, R. Myers-Ward, C. Eddy, Jr.
Naval Research Laboratories, Washington, DC

Recent progress in epitaxial graphene (n,p)-MOSFETs on both SiC and Si substrates for graphene-on-SiC and graphene-on-Si technologies fabricated on 75-mm wafers will be discussed. Several prototype RF circuits including multipliers and mixers will be presented.

1.2: Post Si CMOS Graphene Nanoelectronics (1:50)

C. Y. Sung
IBM T. J. Watson Research Center, Yorktown Heights, NY

IBM's epitaxially grown graphene (1–2 layers) FET yields the highest cut-off frequency value reported to date (~170 GHz), which is well above the Si MOSFET $f_T - L_g$ trend shown at the 2008 International Roadmap for Semiconductors (ITRS). Bi-layered graphene FETs with I_{on}/I_{off} ratios of 100 and 1600 were demonstrated at T = 300 and 25K, respectively, which suggests graphene for not only analog but also logic device applications. A novel reconfigurable graphene p-n junction based logic device is also introduced.

1.3: Radio-Frequency Graphene Transistor Technology Using Large-Area Chemical Vapor Deposited Graphene (2:10)

O. M. Nayfeh, T. Marr, T. Ivanov, J. Wilson, R. Proie, M. Dubey
Army Research Laboratory, Adelphi, MD

Recent advances in the design fabrication, characterization, and modeling of a transistor technology based on large-area CVD graphene will be presented. In particular, (1) top-gate transistors that exhibit the first high-frequency performance for CVD graphene with as-measured RF current cut-off frequency >1 GHz without back-biasing; (2) measurements and modeling under vacuum and anneal conditions to understand important aspects of the carrier transport; (3) interfacing of the graphene for the first time with advanced dielectrics, such as (piezo) AlN for enhanced performance and techniques for direct ALD of high-k dielectrics for efficient gate-coupling; and (4) lastly, novel advanced device concepts and circuits that exploit its tunable property such as tunable oscillators and low/no power switches.

1.4: Graphene Devices for Communications and Sensing **(2:30)**

T. Palacios, H. Wang, A. Hsu, K. Kang Kim, D. Antoniadis, J. Kong
Massachusetts Institute of Technology, Cambridge, MA

The use of graphene grown by chemical vapor deposition in the fabrication of transistors and frequency multipliers operating at gigahertz frequencies will be described. The first compact model of graphene devices, a fundamental step towards the demonstration of complex graphene circuits for RF communications and sensing, will be introduced.

BREAK **(3:00)**

Session 2

EMERGING SEMICONDUCTOR TECHNOLOGIES I

Tuesday, 22 March / 1:30 – 3:00 pm / Gold Coast

Chair: **J. Ibrecht**
DARPA/MTO, Arlington, VA

Co-Chair: **D. J. Radack**
Institute for Defense Analyses, Alexandria, VA

2.1: High-Frequency Power-Amplifer Circuit Capabilities above 100 GHz Based on sub-50-nm InP HEMT Transistor Technology **(1:30)**

R. Lai, V. Radisic, W. Deal, K. Leong, X. B. Mei, S. Sarkozy, B. Gorospe
Northrop Grumman, Redondo Beach, CA

Recent advances in sub-50-nm InP HEMT technology has significantly raised the state-of-art capability and potential of solid-state MMIC and S-MMIC power amplifiers above 100 GHz. Recent technology advances and latest performance capabilities at 220 and 340 GHz will be discussed.

2.2: THz Transistors and Integrated Circuits **(1:50)**

W. R. Deal, K. Leong, S. Sarkozy, V. Radisic, X. B. Mei
Northrop Grumman, Redondo Beach, CA

In the last few years, InP HEMTs have reached an estimated maximum frequency of oscillation (fMAX) greater than 1.2 THz, which therefore enables integrated circuits operating at significantly higher frequencies. This paper deals with both the transistor technology that makes this innovation possible, as well as presenting operating circuit results at 0.67 THz, including low-noise amplifiers and power amplifiers.

2.3: InP HBT Technology for THz Monolithic Integrated Circuits (TMICs) **(2:10)**

M. Urteaga, M. Seo, J. Hacker, Z. Griffith, A. Young, R. Pierson, P. Rowell
Teledyne Scientific Co., Thousand Oaks, CA

A. Skalare
Jet Propulsion Laboratory, Pasadena, CA

M. Rodwell
University of California Santa Barbara, Santa Barbara, CA

An InP HBT technology with an f_{max} >800 GHz has been developed for integrated circuit demonstrations at the lower end of the THz frequency band (0.3-3.0 THz). Amplifiers, oscillators, frequency dividers, and mixers have all been demonstrated operating at >300 GHz. Larger-scale-integrated receivers (amplifier, mixer, and oscillator) and phase-locked-loop circuits have also been realized.

2.4: Integration of III-V Transistors and Si CMOS on Silicon Substrates: A Path to Adaptable, Reconfigurable, High-Performance Integrated Circuits (2:30)

T. E. Kazior, J. R. LaRoche, W. Hoke
Raytheon Integrate Defense Systems, Andover, MA

E. A. Fitzgerald, M. Bulsara
Massachusetts Institute of Technology, Cambridge, MA

M. Urteaga, J. Bergman, M.-J. Choe, K.-J. Lee, M. Seo, T. Seong, A. Yen
Teledyne Scientific Co., Thousand Oaks, CA

D. Lubyshev, J. M. Fastenau, A. W. K. Liu
IQE, Inc., Bethlehem, PA

The status of the integration of high-performance III-V devices (InP HBTs, GaN HEMTs) with high-density Si CMOS logic on a common silicon substrate (COSMOS) to create high-dynamic-range converters (DACs and ADCs) and intelligent transceiver ICs whose performance can not be achieved with today's technology will be presented.

BREAK (3:00)

Session 3

TRUSTED ELECTRONICS RESEARCH

Tuesday, 22 March / 1:30 – 3:00 pm / Sun & Surf

Chair: **B. S. Cohen**
Institute for Defense Analyses, Alexandria, VA

Co-Chair: **C. C. Cerny**
Air Force Research Laboratory, Wright Patterson AFB, OH

3.1: Light-Weight Key Generator Using PUFs (1:30)

M.-D. Yu, R. Sowell
Verayo, Inc., San Jose, CA

S. Devadas
Massachusetts Institute of Technology, Cambridge, MA

A light-weight key generator using PUFs is described. Without the use of complex error correction codes, a high level of environmental robustness is achieved. Complexity of the light-weight error correction core will be compared with other schemes, showing large savings in area.

3.2: Verifying Trustworthiness of Integrated Circuits (1:50)

X. Zhang, M. Tehranipoor
University of Connecticut, Storrs, CT

Various vulnerabilities to the IC/IP design and fabrication processes will be presented. Effective techniques will be presented for detecting and locating malicious alterations, *e.g.,* hardware Trojans, during IP core design, wafer probe and/or packaged IC test as a means of improving the level of trustworthiness of the integrated circuits. A comprehensive design methodology to increase the probability of detection of hardware Trojans is presented.

3.3: Trusted FPGA Design Using Non-Integrated and Fully Integrated Embedding of Checking Structures (2:10)

S. Dutt, M. Maggioni
University of Illinois at Chicago, Chicago, IL

The reprogramming capabilities of FPGAs are a threat to application security, opening the original circuit design to malicious modifications. An ECC-structured trust design and checking mechanism for FPGA circuits that empirically show very high detection probability and zero false-alarm probability will be presented. In this context, two types of embedding of the checking logic, non-integrated and fully integrated, are presented and their pros and cons discussed.

3.4: Secure Chip Interconnect (2:30)

F. Kiamilev, S. Janansky, N. Waite, R. McGee
University of Delaware, Newark, DE

Four methods that can be applied individually or as layered defenses to harden security of communication buses between chips on a motherboard has been explored. This work was undertaken because modern, high-performance buses are “insecure” (*i.e.,* they are vulnerable to tapping and Trojan insertion).

BREAK (3:00)

Session 4

GRAPHENE ELECTRONICS

Tuesday, 22 March / 3:30 – 5:00 pm / Space Coast

Chair: **C. Lau**
Institute for Defense Analyses, Alexandria, VA

Co-Chair: **M. Fritze**
DARPA/MTO, Arlington, VA

4.1: **Characterization and Comparison of Devices Fabricated from Epitaxial Graphene on SiC and Electrostatically Transferred Graphene** **(3:30)**

S. W. Howell, T. E. Beechem, L. B. Biedermann, C. Gutierrez, T. A. Friedmann, K. F. McCarty, T. Ohta, W. Pan, A. J. Ross
Sandia National Laboratories, Albuquerque, NM

Recent advancements in the fabrication of devices from epitaxial graphene (EG) on SiC (0001), as well as a method to electrostatically transfer EG onto arbitrary substrates (Si and Pyrex) will be presented. The electronic properties of electrostatically transferred EG with nominally equivalent as-grown EG on SiC will be compared.

4.2: **Gate Dielectric and Transistor Design Considerations for Graphene Electronics** **(3:50)**

J. Robinson, M. Hollander, M. Labella III, R. Cavelero, K. Trumbull, Z. Hughes, E. Hwang, S. Datta, D. Snyder
Penn State University, University Park, PA

The potential of multiple-gate dielectrics for use in graphene FETs will be investigated. How the use of various seed layers and dielectric materials affect Hall mobility, gate leakage current, and transistor performance will be examined. Finally, the performance of gFETs as a function of source, drain, and gate design for the development of robust graphene-based electronics will be discussed.

4.3: **Diffusion Barrier Technology for Transfer-Free Graphene-on-Silicon Device Development** **(4:10)**

C. Howsare, Z. Hughes, K. Trumbull, M. LaBella, D. Snyder, J. Robinson
The Penn State Electro-Optics Center, University Park, PA

Chemical vapor deposition of graphene on Cu/SiO_2/Si substrates has been demonstrated as a potential route toward large-scale graphene device production. The use of various barrier layers to prevent Cu/Si interdiffusion, their effects on the deposited graphene, and the subsequent fabrication and electrical testing of graphene devices have been investigated.

4.4: Graphene Transistors for Digital Applications (4:30)

D. Jena, K. Tahy, T. Fang, P. Zhao, W.-S. Hwang, M. Kelly
University of Notre Dame, Notre Dame, IN

S. Koswatta
IBM T. J. Watson Research Center, Yorktown Heights, NY

K. Gaskill, R. Myers-Ward, J. Tedesco, C. Eddy
Naval Research Laboratory, Washington, DC

H. Xing, A. Seabaugh
University of Notre Dame, Notre Dame, IN

The comparison of the high-field characteristics, the device modeling, and the analytical calculation of graphene nano-ribbon FETs with a lateral p-n junction as the channel, a first step toward the realization of graphene-based TFETs, will be presented. Progress made in large-area CVD graphene growth on Cu will be reported.

Session 5

ADAPTIVE RF / BIST AND CALIBRATION

Tuesday, 22 March / 3:30 – 5:00 pm / Gold Coast

Chair: **S. Raman**
DARPA/MTO, Arlington, VA

Co-Chair: **J. E. Wilson**
Army Research Laboratory, Adelphi, MD

5.1: Tunable Receiver for 6–18 GHz with Autonomous Self-Healing (3:30)

G. Sollner, J. Smolko, S. Lardizabal, R. Molfino, M. Morton, A. Kopa, C. Wang, A. Imhoff
Raytheon Co., Tewksbury, MA

E. Wyers, A. Leonard, S. Lipa, C. T. Kelly, P. Franzon, M. Steer
North Carolina State University, Raleigh, NC

J. Bardin, F. Bohn, H. Wang, K. Dasgupta, A. Hajimiri
California Institute of Technology, Pasadena, CA

Sensors, controls, and healing algorithms that are used to adjust for the wide component variation in 65-nm CMOS is being developed. A first demonstration is a wideband receiver that is tunable between 6 and 18 GHz. This design has been fabricated and test results will be presented.

5.2: Virtual Phase Noise Sensor for Self-Healing Voltage Controlled Oscillators (3:50)

S. Yaldiz, F. Wang, X. Li, L. Pileggi
Carnegie Mellon University, Pittsburgh, PA

A. S. Natarajan, M. A. Ferris, J. Tierno
IBM T. J. Watson Research Center, Yorktown Heights, NY

A virtual phase noise sensor enabling self-healing of VCOs uses response surface modeling and exploits the correlations between the phase noise of the VCO and other performance metrics. Simulation-based results show that the self-healing design yield approaches ideal phase noise parametric yield and can achieve up to 15% reduction in power dissipation.

5.3: Self-Healing 4-Gbit/sec Reconfigurable CMOS Radio-on-a-Chip (4:10)

M.-C. F. Chang, A. Tang, Q. J. Gu
University of California, Los Angeles, Los Angeles, CA

C. Chien
CreoNex Systems, Inc., Westlake Village, CA

The development of scalable circuit-level self-healing techniques to maximize the number of fully operational reconfigurable CMOS Radio-on-a-Chip (RoC) with over-the-air data transmission rates of 4 Gbps from an individual wafer run that meets all performance metrics in the presence of extreme process variations and environmental conditions will be discussed.

5.4: A 20-GHz Six-Port S-Parameter IC for In-Situ Circuit Verification and Self-Tuning Measurements (4:30)

W. R. Eisenstadt, M.-C. Lee
University of Florida, Gainesville, FL

A compact 20-GHz on-chip “six-port” s-parameter network analyzer IC (SPR) built in 0.13-□m IBM 8HP BiCMOS with a 1.25 x 1-mm layout is introduced. The 20-GHz six-port on-chip SPR circuit performance, layout, calibration, and verification measurements will be presented.

Session 6

TRUSTED ELECTRONICS APPLICATIONS I

Tuesday, 22 March / 3:30 – 5:00 pm / Sun & Surf

Chair: **J. A. Meinhardt**
Honeywell FM&T, Kansas City, MO

Co-Chair: **D. G. Both**
NSA, Ft. Meade, MD

6.1: Secure System-on-a-Chip Design **(3:30)**

R. A. Gonzales, D. L. Jensen, G. N. McGovney
Sandia National Laboratories, Albuquerque, NM

Sandia's Key Data Processor (KDP) is a generic System-on-a-Chip processor system. While it is designed to securely host the cryptographic algorithms that ensure the integrity, availability, and confidentiality of the Military GPS for the Selective Availability Anti-Spoofing Module (SAASM), it can host a wide variety of field-programmable application software packages.

6.2: IP Tampering and Prevention Techniques **(3:50)**

S. Ventrone, I. Arsovski, A. M. Chu, K. A. Ford, L. Pickup, C. Reynolds, D. Scagnelli, D. Seitzer, R. Shetty, J. Zimmerman, P. Zuchowski
IBM, Essex Junction, VT

The classes and types of potential tampering will be examined. The second section will deal with the execution and release of the tampering that may be undetected with current methods. The third and final section will discuss potential detection and prevention techniques that may be used and or developed to counter this potential tampering threat.

6.3: Fast Mask Data Recovery to Provide Missing/ Incomplete Technical Data Packages (TDP) for Obsolete ICs and Validating Trust within ICs **(4:10)**

D. J. Weaver, J. Asmuth, L. R. Avery
SRI International Sarnoff, Princeton, NJ

W. Johnson
Defense Logistics Agency, Columbus, OH

H. Hanson
Space and Naval Warfare Systems Center Pacific, San Diego, CA

An electron-beam system has been developed to recover IC design data from physical ICs. Fast verification of ICs trust and the required improvements for the future technologies will be discussed.

6.4: Counterfeit Trends: Increasing Difficulties in Detection **(4:30)**

M. Marshall
Integra Technologies LLC, Wichita, KS

Some of the new and more difficult detection modes to detect devices that are becoming more commonplace will be discussed. Various detection methods will be discussed and their likely success and failure in the detection of new classes of counterfeit components. Examples of counterfeit devices will be presented and discussed as case studies for detection methods. A key point of the discussion will be the need to continuously improve our techniques for detection of counterfeit devices. The counterfeit landscape is changing and shifting and morphing. Detection methods effective today may have diminished success in the future.

WEDNESDAY, 23 MARCH

Session 7

3DIC I

Wednesday, 23 March / 8:30 – 10:00 am / Space Coast

Chair: **M. Fritze**
DARPA/MTO, Arlington, VA

Co-Chair: **C. Lau**
Institute for Defense Analyses, Alexandria, VA

7.1: Three-Dimensional Integrated Circuits (3DIC) Technology for System Applications **(8:30)**

J. U. Knickerbocker
IBM T. J. Watson Research, Yorktown Heights, NY

Three-dimensional integrated-circuit (3DIC) technology offers miniaturization, cost reduction, power savings, and performance-enhancement options for system applications. The enabling-base-technology advancements including (i) TSVs, (ii) high-bandwidth low-power I/O channels, (iii) high-density die-stacking technology, (iv) wafer-level test and fine-pitch test technology, and (v) power delivery and cooling solutions will be discussed. 3DIC test vehicle results will highlight technology advancements and demonstrations.

7.2: 3D Field-Programmable Gate Array **(8:50)**

Y. Yang-Liauw, F. Crnogorac, E. Chen, W. S. Jung, W. Kim, S. I. Park, Z. Zhang, C.-Y. Che, P. Griffin, A. El Gamal, F. Pease, J. Plummer, K. Saraswat, S. S. Wong
Stanford University, Stanford, CA

The architecture and design of 3-D FPGA will be presented. A monolithically stacked 3-D FPGA can achieve about 2.5 times reduction in critical path delay and 2.9 times reduction in dynamic power consumption over a conventional 2-D FPGA. An experimental 3-D prototype will be discussed.

7.3: 3DIC Multi-Project Wafer Service: A Practical Method for Mixed Technologies on a Single-Chip Footprint **(9:10)**

V. C. Tyree, W. Hansford
University of Southern California, Marina del Rey, CA

The availability of 3DIC Multi-Project Wafer (MPW) service for CMOS technology opens the door for mixing MEMS, photonics, and III-V technologies onto the same footprint as the CMOS circuits.

7.4: 3D Integration Technology Platforms for High-Performance Mixed-Signal Applications **(9:30)**

D. S. Temple, D. Malta, E. Vick, J. M. Lannon, Jr., J. D. Reed, A. Huffman
RTI International, Research Triangle Park, NC

Progress in the development of 3-D integration technology platforms that enable miniaturization and performance enhancement of electronic microsystems in military applications will be reviewed. The electrical performance of 3-D silicon interposers as well as die pairs integrated with face-to-face metal bonds and heterogeneous IC stacks capable of massively parallel signal processing will be described.

BREAK **(10:00)**

Session 8

ADVANCED RF/MIXED SIGNAL CIRCUITS

Wednesday, 23 March / 8:30 – 10:00 am / Gold Coast

Chair: **S. Raman**
DARPA/MTO, Arlington, VA

8.1: **Self-Healing CMOS ADC Design for Broadband Radios** **(8:30)**

S. Hshemi, Y. Toriyama, D. Markovic, D. Cabric, A. H. Sayed, J. C.S. Woo, B. Razavi
University of California Los Angeles, Los Angeles, CA

As part of the MTO HEALICS program, a self-healing ADC is under development to target a resolution of 10 bits and a sampling rate of 1 GHz with a power consumption of 10 mW in 65-nm CMOS technology. The ADC heals the offset of the comparators by shuffling their reference voltages rather than cancel their offset. As a result, the signal path remains undisturbed and the best trade-off between speed and power consumption is achieved.

8.2: **Analysis and Modeling of Non-Idealities in VCO-Based Quantizers Using Frequency-to-Digital and Time-to-Digital Converters** **(8:50)**

S. M. Yoder, W. Khalil, M. Ismail
Ohio State University, Columbus, OH

G. Creech
Wright-Patterson Air Force Base, Columbus, OH

VCO-based ADCs are becoming more attractive over conventional ADCs due to their inherent time-resolution architecture. A comprehensive analytical modeling and simulation of the VCO-based ADC in the presence of circuit non-linearity and jitter is presented. Time quantization using TDC is proposed for the first time and compared with FDC.

8.3: **Wideband Decade-Bandwidth 2–20 GHz GaN HEMT Power-Amplifier MMIC with Variable Power via Bias Adjustment** **(9:10)**

J. J. Komiak, S. M. Jessup, K. Chu, P. C. Chao
BAE Systems, Nashua, NH

The design and performance of a MMIC power amplifier that has established new benchmarks for 220-GHz power is reported. The amplifier achieved a P3 dB of 16 W with 26% PAE and 9.7-dB power gain from 2 to 20 GHz at full bias. Under bias adjustment conditions, 8 dB of variable power has been demonstrated while maintaining the PAE and power gain. To the authors' knowledge, this is the first reported result of performance versus bias conditions for wideband GaN HEMT power amplifiers.

8.4: **Single-Chip K-Band Transceiver ASIC with Internal PLLs, Image Reject Mixer, and Multiplexed IF** **(9:30)**

S. M. Lorg
Viasat, Inc., Gilbert, AZ

The design and measured results of a low-cost highly integrated K-band transceiver ASIC will be presented. This ASIC includes a transmitter, a receiver with 40-dBc image rejection, two independent PLLs, and a telemetry modulator/demodulator.

BREAK **(10:00)**

Session 9

TRUST IN ICs

Wednesday, 23 March / 8:30 – 10:00 am / Sun & Surf

Chair: **C. McCants**
DARPA, Arlington, VA

Co-Chair: **B. S. Cohen**
Institute for Defense Analyses, Alexandria, VA

9.1: DARPA TRUST Program (8:30)

C. E. McCants
DARPA Microsystems Technology Office, Arlington, VA

The DARPA TRUST in Integrated Circuits program is coming to a conclusion in FY11. This talk will provide a synopsis of the program success to date and a discussion of the transition activities.

9.2: ASIC TRUST Verification (8:50)

R. C. Anderson, T. D. Kim, R. T. Narumi, P. Saghizadeh
Raytheon Corp., El Segundo, CA

Under the DARPA TRUST in Integrated Circuits program, the Raytheon team has developed a set of verification techniques and tools that checks the entire ASIC flow to detect any changes compared to a golden representation.

9.3: Imaging ICs with X-Ray Microscopy (9:10)

M. Bajura, G. Boverman, J. Tan, G. Wagenbreth, C. M. Rogers
University of Southern California, Marina Del Rey, CA

M. Feser, J. Rudati, A. Tkachuk
Xradia, Inc., Pleasanton, CA

S. Aylward, P. Reynolds
Kitware, Inc., Carrboro, NC

X-ray microscopy as a non-destructive approach to image integrated circuits (ICs) has been developed. This capability could be applied to sampling IC lots from untrusted sources for comparison with a known design or to reverse engineering of a given device to determine its transistor-level layout. Imaging examples of 90-nm CMOS circuits from our work in DARPA's TRUST program will be presented.

9.4: Change Detection Platform for FPGA Trust (9:30)

J. Graf
Luna Innovations, Inc., Roanoke, VA

To trust an FPGA design, one must know not only how the design implements its required function, but also that it does not implement any additional undesired features. The Luna Change Detection Platform performs both of these tasks for FPGA designs and FPGA third-Party IP cores.

BREAK (10:00)

Session 10

3DIC II

Wednesday, 23 March / 10:30 am – 12:10 pm / Space Coast

Chair: **C. Lau**
Institute for Defense Analyses, Alexandria, VA

Co-Chair: **M. Fritze**
DARPA/MTO, Arlington, VA

10.1 An SOI-Enabled Technology for 3DIC Multiproject Wafers (10:30)

C. K. Chen, B. Wheeler, D.-R. W. Yost, J. M. Knecht, C.-L. Chen, C. L. Keast
Massachusetts Institute of Technology, Lexington, MA

An overview of the 3DIC multi-wafer project will be presented.

10.2: Vertically Integrated Pixel Readout Chip for High-Energy Physics (10:50)

G. W. Deptuch, M. Demarteau, J. Hoff, F. Khalid, R. Lipton, A. Shenai, M. Trimpl, R. Yarema, T. Zimmerman
Fermi National Accelerator Laboratory, Batavia, IL

Fermilab participated in two 3D Multi-Project-Wafer (MPW) runs by MIT-LL, where three SOI wafers with a 400-nm-thick BOX, a 50-nm-thick SOI layer, and three routing metal layers fabricated in a 0.18- or 0.15-mm fully depleted SOI (FDSOI) process were stacked using the via last approach. Two versions of a 2.5 × 2.5-mm^2 pixel prototype, called VIP1 and VIP2a (vertically integrated pixel) were submitted in 2006 and 2008, respectively. The thickness of the entire structure is about 700 mm, while the three active tiers are only about 22 mm in total. Each TSV occupies effectively about 5 × 5 mm^2, including pads receiving vias on the lower tiers of the stack and clearances between neighboring vias. There are about 200 transistors per pixel. The VIP1 chip is the first 3D prototype designed at Fermilab.

10.3: Power-Grid Noise in TSV-Based 3-D Integrated Systems (11:10)

I. Savidis, S. Kose, E. G. Friedman
University of Rochester, Rochester, NY

A test circuit examining power-grid noise in a 3-D integrated stack has been designed, fabricated, and tested. Fabrication and vertical bonding was performed by MIT Lincoln Laboratory for a 150-nm three-metal-layer SOI process. Three wafers were vertically bonded to form a 3-D stack. Noise analysis of three different power-delivery topologies will be described. The effect of through silicon via (TSV) density on the noise profile of the power delivery network for the 3-D stack will also discussed. A comparison of peak noise for each of the topologies with and without board-level decoupling capacitors is provided, and suggestions for enhancing the design of the power-delivery network are offered.

10.4: On-Chip Dynamic Programming Networks Design in TSV-Based 3D Stacking Technology (11:30)

T. Mak
Newcastle University, Newcastle Upon Tyne, UK

The design of a dynamic programming network (DP network) implemented in a fully stacked three-layered 3D through-silicon-via (TSV) 150-nm CMOS technology will be presented. The chip testing results demonstrated the effectiveness and high-speed computation of such a DP network for deadlock detection in 3D Networks-on-Chip (NoC).

10.5: 3D Integration of FD-SOI MESFETs and Photodiodes for Cellular Neural Networks (11:50)

T. Thornton
Arizona State University, Tempe, AZ

In previous multi-project runs through MIT Lincoln Labs, the feasibility of integrating MESFET devices with FD-SOI CMOS has been demonstrated. As part of the 3DM3 opportunity, the MESFETs with a CMOS transimpedance amplifier and photodiodes were combined to explore the potential of 3D integration for optical pattern recognition based on cellular neural networks (CNN). The enormous packing density offered by 3D integration combined with the power of local signal processing from CNN at each sensing node has the potential for ultra-high-speed low-power optical pattern recognition. Results characterizing the performance of the individual components in the 3D circuit will be presented and future plans for this exciting technology will be described.

LUNCH (12:10)

Session 11

RF CIRCUITS FOR WIRELESS SENSORS

Wednesday, 23 March / 10:30 am – 12:00 pm / Gold Coast

Chair: **P. L. Orlando III**
AFRL, Wright-Patterson AFB, Dayton, OH

Co-Chair: **J. E. Penn**
Army Research Laboratory, Adelphi, MD

11.1: Integrated CMOS Transceivers Applied to a Wide Area Radio Network for Sensor (WARNS) Communication (10:30)

W. C. Wesson, V. Bhagavatula, J. C. Rudell
University of Washington, Seattle, WA

A new concept for long-range sensor data communication, which challenges some of the assumptions of short-range communication using MESH networks, is being investigated at the University of Washington. The long-term vision of the sensor radio research program is the development of practical, small-form factor wireless sensor nodes with the ability to communicate using any available wireless network; this could be cellular, WiFi, or Bluetooth systems. A quick overview of the PIs background and the VLSI program at the University of Washington will be followed by a description of the Wide-Area Sensor Network (WASN) concept. Finally, a regulator-less CMOS GSM power amplifier currently under development for WASN applications will be described.

11.2: Low-Power RF Wireless Sensor Design with Highly Efficient SiGe RF Power Amplifier and Ultra-Low-Power SAR ADC (10:50)

D. Y.-C. Lie, J. Lopez, W. Hu
Texas Tech University, Lubbock, TX

Two of the key circuit blocks for realizing intelligent low-power RF wireless sensors will be discussed: (1) highly-efficient Si-based medium-power RF SiGe power amplifiers (PAs) and (2) an ultra-low-power analog-to-digital converter (ADC). Without needing off-chip on-board matching, high power-added efficiency (PAE) for the single-stage SiGe PAs at ~70% (900 MHz) and ~60% (2.4 GHz), respectively, in IBM's 0.18-□m BiCMOS process, for which performances rival that of commercially available III-V PA modules, has been achieved.

11.3: Postage-Stamp-Sized Micro-Sensor Technology (11:10)

J. E. Brewer
Kairos Microsystems Corp., Melrose, FL

K. K. O
Kairos Microsystems Corp., Melrose, FL
and
University of Texas at Dallas, Richardson, TX

Micro-sensor nodes with operating peaks of ~1 mA peak for 20-km node-to-node and 1-km node-to-base station communications (>1 year at 0.1% duty), approximately the size of a postage stamp, have been designed . This is a >10x improvement compared to the 2010 commercial state of the art.

11.4: A 1–20-GHz GaN HEMT Low-Noise Amplifier (11:30)

R. Benelbar, R. Mongia, J. Dishon, B. Preskenis, S. Nelson
Cobham Sensor Systems, Richardson, TX

J. Gillespie, T. Quach, L. Orlando, A. Mattamana, K. Groves, K. Chabak, A. Crespo, R. Fitch, M. Trejo, T. Dalrymple
AFRL, Wright-Patterson AFB, OH

A 120-GHz GaN-on-SiC HEMT high-dynamic-range low-noise amplifier (LNA) was designed using the AFRL 0.15-□m gate-length 0.15-□m GaN-on-SiC high-electron-mobility transistor (HEMT) process. The LNA offers a predicted performance of <4-dB NF to 18 GHz, with 16-dB associated gain, output P1 dB > 0.5 W, and in/out SWR near 1.2:1, at room temperature. RF input power handling of the LNA is predicted to be >33 dBm. Measured LNA RF performance will be presented.

LUNCH (12:00)

Session 12

TRUSTED ELECTRONICS APPLICATIONS II

Wednesday, 23 March / 10:30 am – 12:00 pm / Sun & Surf

Chair: **D. G. Both**
NSA, Ft. Meade, MD

Co-Chair: **J. A. Meinhardt**
Honeywell FM&T, Kansas City, MO

12.1: Process-Feature Development Opportunities on 300 mm x 65 nm CMOS for Defense Applications (10:30)

M. Liehr, D. Coolbaugh
University at Albany, Albany, NY

A set of existing and potential future opportunities for custom development of 65-nm CMOS-based capability at the College of Nanoscale Science and Engineering are specified.

12.2: Next-Generation Carbon-Nanotube (CNT) Based Nano-electronic Devices Offered Through a Fully Trusted DoD Accredited Supply Chain (10:50)

G. C. Taylor, G. Derderian
Lockheed Martin Space Systems Co., Billerica, MA

P. H. Behrens II
National Semiconductor Corp., Annapolis Junction, MD

Lockheed Martin Nanosystems and National Semiconductor will provide an update on their development of the next-generation CNT nano-electronic devices for terrestrial and space applications, including new manufacturing capabilities and incorporating TRUST into CNT electronics manufacturing.

12.3: Testing Solutions for PEM FPGAs in High-Reliability Systems (11:10)

M. Marshall
Integra Technologies LLC, Wichita, KS

The main content of the presentation will be a summary of up-screening and qualification methods for FPGAs that have been successfully used by aero-space, military, and space users. The intent is to help educate the commu-nity with the best methods to use PEM FPGAs in critical systems.

12.4: A Cloud Portal for Trusted SoC Design and Manufacturing (11:30)

T. Renz, J. Rooks
Air Force Research Laboratory, Rome, NY

The Air Force Research Laboratory sponsored a workshop to create a stake-holder requirements list for a trusted electronics design environment. Participants included government, DoD, and commercial designers; EDA tools, foundry, and IP suppliers; and trusted cloud experts. Recommen-dations and plans resulting from the workshop will be presented.

LUNCH (12:00)

Session 13

POWER ELECTRONICS I

Wednesday, 23 March / 1:30 – 3:00 pm / Space Coast

Chair: **F. Kub**
Naval Research Laboratory, Washington, DC

Co-Chair: **A. Hefner**
NIST, Gaithersburg, MD

13.1 Advanced SiC Power Technology for Next-Generation Power Electronics (1:30)

D. Grider, A. Agarwal, S.-H. Ryu, M. Das, J. Zhang, J. Richmond, C. Capell, J. Palmour
Cree, Inc., Durham, NC

There have been major advances in the development of a broad range of SiC power technologies, including 1.2–10.0- kV SiC DMOSFETs, 12-kV SiC IGBTs, 10-kV SiC GTOs, 15-kV SiC JBS Diodes, and 1.2-kV SiC BJTs. These recent advances will be reviewed along with their impact on next-generation high-power/high-temperature power electronics.

13.2: Development, Performance, and Applications of 4.5-kV SiC JBS Diodes (1:50)

A. Hefner, K. Hobart
NIST, Gaithersburg, MD

S. H. Ryu, D. Grider
Cree, Inc., Durham, NC

F. Kub
Naval Research Laboratory, Washington, DC

A new 60-A 4.5-kV SiC JBS diode will be presented, and its performance is compared to Si PiN diodes used as the anti-parallel diode for 4.5-kV Si IGBTs. The current–voltage, capacitance–voltage, reverse leakage, and reverse recovery characteristics of both diode types were measured using recently developed high-voltage high-frequency device test systems. The results indicated that the SiC JBS diodes are far superior to the silicon PiN diodes, resulting in an order of magnitude less switching loss and substantially less current spike stress. Applications and payoffs for the high-voltage SiC JBS will be discussed.

13.3: High Temperature and Switching Characterization of Ultra-High-Voltage SiC GTO Thyristors (2:10)

R. Singh, S. Jeliazkov, E. Lieser
GeneSiC Semiconductor, Inc., Dulles, VA

Through a systematic study, silicon carbide gate-turn-off (GTO) thyristors with record performance were demonstrated. Optimized fabrication parameters were developed that resulted in >6.5-kV >75-A devices with high yields (>65%) and a record low differential specific on-resistance of 2.55 $m\Omega$-cm^2. High-temperature static and dynamic operation was found to be stable with temperature. Turn-on transient characteristics show a stable delay time of about < 80 nsec and a rise time that decreases with increasing temperature. Switching measurements were used, for the first time, to extract the value of high-level minority-carrier lifetimes as a function of temperature.

13.4: Development of Silicon Carbide High-Voltage Switches for Power Converters and Solid-State Disconnects **(2:30)**

P. Alexandrov, J. Zhang, L. Fursin, X. Li, C. Dries
United Silicon Carbide, Inc., Monmouth Junction, NJ

L. Lin, J. H. Zhao
Rutgers University, Piscataway, NJ

T. Burke
U.S. Army RDECOM-TARDEC, RDTA-RS, Warren, MI

F. Kub
Naval Research Laboratory, Washington, DC

The development of high-voltage and high-current 4H-SiC VJFETs, BJTs, and GTOs, and the corresponding performance of solid-state disconnects and power converters, will be presented. Experimental results and technological aspects will be reviewed. The follow-up R&D activity will be outlined.

BREAK **(3:00)**

Session 14

EMERGING SEMICONDUCTOR TECHNOLOGIES II

Wednesday, 23 March / 1:30 – 3:00 pm / Gold Coast

Chair: **J. Albrecht**
DARPA/MTO, Arlington, VA

Co-Chair: **D. J. Radack**
Institute for Defense Analyses, Alexandria, VA

14.1: Highly Scaled GaN Electronics for Mixed-Signal Applications (1:30)

M. Micovic, K. Shinohara, I. Milosavljevic, A. Kurdoghlian, A. Corrion, S. Burnham, A. Schmitz, D. F. Brown, D. Regan, D. Chow
HRL Laboratories LLC, Malibu, CA

GaN MMIC technology has demonstrated RF power performance superior to any other MMIC technology up to a frequency of 100 GHz and has strong potential for sub-mmW power applications. Progress toward highly scaled E- and D-mode GaN transistors for mixed signal applications with cutoff frequencies of 800 GHz that are being developed under the DARPA NEXT program will be described. To date, GaN transistors with f_t = 220 GHz and f_{max} = 400 GHz have already been demonstrated.

14.2: State-of-the-Art E/D GaN Technology Based on an InAlN/AlN/GaN Heterostructure (1:50)

P. Saunier, A. Ketterson, M. Schuette, T.-M. Chou, J. Jimenez, H.-Q. Tserng
TriQuint Semiconductor, Richardson, TX

G. Xing
University of Notre Dame, Notre Dame, IN

S. Guo, X. Gao
IQE-RF LLC, Somerset, NJ

Under the DARPA NEXT contract, a very promising E/D GaN technology has been under development. The E-mode devices are achieved by selective recess of InAlN on AlN. Transconductance above 1 S/mm with a drive current of 1.9 A/mm have been demonstrated. The necessary small gate length was fabricated using a sidewall (or gate-shrink) process. An f_t of 140 GHz has been demonstrated on the same wafer for both E- and D-mode devices. 51-stage ring oscillator circuits have already been demonstrated.

14.3: N-Face GaN HEMT Technology for Next-Generation Mixed-Signal Electronics (2:10)

I. Smorchkova, R. Grundbacher, V. Gambin, X. Gu, G. Lewis, F. Oshita, C. Namba, P. Liu, S. Poust, P. Nam, M. Wojtowicz
Northrop Grumman, Redondo Beach, CA

U. K. Mishra
University of California at Santa Barbara, Santa Barbara, CA

The progress made on DARPA's Nitride Electronic Next-Generation Technology (NEXT) program will be discussed. On this program, Northrop Grumman and its team members are utilizing the intrinsic benefits of N-face nitride semiconductors to enable a highly scaled E/D-mode GaN technology for advanced mixed-signal applications.

14.4: Recent Advances in GaN-on-Diamond Development **(2:30)**

D. Francis, D. Babic, F. Faili, Q. Diduck, C. Khandavalli, F. Ejeckam
Group4 Labs, Inc., Fremont, CA

A summary of the state of the art of GaN-on-diamond wafer technology used for high-power and high-frequency applications will be presented. Late-breaking RF results, comparative thermal performance, and wafer-bow management will be presented. Significantly enhanced versions of GaN-on-diamond wafer technology will be presented.

BREAK **(3:00)**

Session 15

RADIATION-HARDENED MICROELECTRONIC DESIGN

Wednesday, 23 March / 1:30 – 3:00 pm / Sun & Surf

Chair: **R. C. Lacoe**
The Aerospace Corp., Los Angeles, CA

Co-Chair: **L. Massengill**
Vanderbilt University, Nashville, TN

15.1: Radiation Hardness by Design Using 45-nm SOI (1:30)

A. Kleinosowski, E. Cannon, T. Amort, M. Cabanas-Holmen, W. Snapp, R. Brees, J. Evans, J. Popp, S. Rabaa, J. Tostenrude, J. Mackler, A. Hurtado, T. McKay
Boeing Research and Technology, Seattle, WA

The foundational modeling and design approaches for radiation hardness by design using the 45-nm SOI fabrication process will be presented. Radiation effects and design challenges unique to highly scaled lithography and silicon-on-insulator will be discussed. Sensitivity to low-energy protons will be quantified and design approaches to address this sensitivity will be discussed. Test data collected in previous work will be expanded and presented.

15.2: Radiation-Enabled Compact Modes for Advanced Technology Integrated-Circuit Design (1:50)

J. S. Kauppila, A. L. Sternberg, M. L. Alles, T. D. Loveless, B. L. Bhuva, W. T. Holman, L. W. Massengill
Vanderbilt University, Nashville, TN

Efficient implementation of rad-hard circuits at modern technology nodes requires the consideration of radiation response and mitigation at all levels of the design hierarchy. The development and application of vertically integrated radiation-enabled compact models within a radiation-aware EDA flow are discussed.

15.3: Radiation-Hardened Digital Single-Sideband Modulator ASIC (2:10)

T. Pemberton
Air Force Research Laboratory, Wright-Patterson AFB, OH

H. Axtell, T. Hopkins, J. M. Emmert
Wright State University, Dayton, OH

A rad-hard digital single sideband modulator (DSSM) design fabricated using a structured application-specific integrated-circuit (ASIC) process will be presented. Structured ASIC design processes reduce IC design time and cost by prefabricating and shelving uncommitted standard digital components (for example, NAND gates, ROMS, and flip-flops). The designer commits the design by creating metal masks to wire the components, and the IC foundry adds the metal. When combined with rad-hard standard digital components, the result is an affordable, efficient means for mass-producing rad-hard ICs. The design results for this application will be presented.

15.4: An Overview of NASA's SiGe Integrated Electronics for Extreme Environments Project **(2:30)**

B. J. Blalock
The University of Tennessee, Knoxville, TN

J. D. Cressler
Georgia Tech, Atlanta, GA

A. Mantooth
University of Arkansas, Fayetteville, AR

R. Berger
BAE Systems, Manassas, VA

M. Mojarradi
Jet Propulsion Laboratory, Pasadena, CA

M. Alles, R. Reed
Vanderbilt University, Nashville, TN

W. Johnson, F. Dai, G. Niu
Auburn University, Auburn, AL

J. Holmes
Lynguent, Fayetteville, AR

P. McCluskey
University of Maryland, College Park, MD

L. Peltz, R. Frampton
The Boeing Company, Huntington Beach, CA

The recently completed NASA SiGe ETDP project successfully demonstrated the viability of commercially available SiGe BiCMOS technology for space avionics. The capability developed in the program was used to produce a 16-channel sensor interface and data-acquisition system that can operate reliability across -180°C to +120°C and under radiation exposure.

BREAK **(3:00)**

Session 16

POWER ELECTRONICS II

Wednesday, 23 March / 3:30 – 5:00 pm / Space Coast

Chair: **F. Kub**
Naval Research Laboratory, Washington , DC

Co-Chair: **A. Hefner**
NIST, Gaithersburg, MD

16.1: High-Temperature High-Frequency SiC Power Systems for Aircraft Applications (3:30)

E. S. Cilio, B. McPherson, J. Hornberger, A. Lostetter, M. Schupbach,
APEI, Inc., Fayetteville, AR

J. Scofield
Air Force Research Laboratory, Dayton, OH

A. Agarwal, J. Richmond
CREE, Inc., Durham, NC

A high-temperature three-phase 300-V/5-kVA SiC demonstration system utilizing Cree MOSFETs, specifically targeting an increase in power density and efficiency, has been designed, built, and tested. This discussion will focus on three key points: (1) the design and experimental results of the SiC prototype system, (2) simulation results of a comparably designed Si-based inverter, and (3) a system-level comparison of critical performance parameters between each converter.

16.2: Enhancement-Mode Gallium Nitride (eGaN™) FET Characteristics under Long-Term Stress (3:50)

A. Lidow
Efficient Power Conversion Corp., El Segundo, CA

J. B. Witcher
Sandia National Laboratories, Albuquerque, NM

K. Smalley
Microsemi Corp., Lawrence, MA

Enhancement-mode HEMT transistors built with gallium-gitride-on-silicon (eGaN) have been in the commercial marketplace for more than a year as a replacement for silicon power MOSFETs. Superior conductivity and switching characteristics allow designers to greatly reduce system power losses, size, weight, and cost. Military and space applications would benefit from using eGaN transistors, but the parts would be required to operate reliably under harsh environmental conditions. Results demonstrating the stability of these devices at temperature and under radiation exposure will be presented.

16.3: High Power Density and High Efficiency Power Conversion for Radar Applications (4:10)

G. Mitchell, M. Schupbach
APEI, Inc., Fayetteville, AR

F. Kub
Naval Research Labratory, Washington, DC

R. McCann
University of Arkansas, Fayetteville, AR

Modern phased-array radar systems require a generational improvement in power-supply capabilities. The current research addresses this growing need by combining wide-bandgap power devices with advanced power-conversion topologies. The resulting systems allow improvements not possible with conventional Si-based power device technology.

16.4: Solid Pulse-Forming Lines for Compact Pulsed Power (4:30)

M. T. Domonkos, S. Heidger
Air Force Research Laboratory, Kirtland AFB, NM

D. Brown
SAIC, Albuquerque, NM

A. Devoe
Presidio Components, San Diego, CA

F. Dogan
Missouri Institute of Science and Technology, Rolla, MO

J. Parker
SAIC, Albuquerque, NM

K. Slenes
TPL, Inc., Albuquerque, NM

J. Watrous
NumerEx, LLC, Albuquerque, NM

The use of solid dielectric pulse-forming lines was examined for compact pulsed-power applications. The first approach builds upon prior work using polymer ceramic nanocomposites (PCNC). The second approach involves the use of a ceramic multilayer media arranged as a transmission line.

Session 17

ANTENNA APPLICATIONS

Wednesday, 23 March / 3:30 – 5:10 pm / Gold Coast

Chair: **W. D. Palmer**
Army Research Office, Durham, NC

17.1: Wideband Antennas for Millimeter-Wave Applications (3:30)

D. Filipovic, J. Mruk, N. Sutton, H. Zhou, K. Kim
University of Colorado, Boulder, CO

Wideband millimeter-wave spiral, sinuous, end-fire, and planar log-periodic antennas will be discussed. Antennas are designed to be compatible with surface micromachining and conventional printed-circuit-board technologies. When technology allows, the impedance transforming and balun feeds and beamforming networks are monolithically integrated with antennas. Operating bandwidths for all designed antennas are within 18–10 GHz range. Very small losses and voltage standing-wave ratios (VSWRs) below 2.5:1 are measured. Comprehensive modeling using a finite-element code HFSS, a method of moments code FEKO, and finite-integration code MWS are utilized in the design. Excellent agreement with measurement are obtained.

17.2: A Transient Radiation-Pattern Measurement Technique (3:50)

J. Henrie, M. Tang
Point Mugu Naval Air Station, Pt. Mugu, CA

Conventional methods for measuring antenna radiation patterns record static magnitude and phase data that does not change with time. However, the radiation patterns of electronically steerable antennas such as phased arrays are capable of evolving on the nanosecond time scale. A simple technique for obtaining a time-domain measurement of the transient radiation pattern emitted by an electronically steerable antenna is proposed, and an experimental demonstration of the method is provided.

17.3: Common Mode Current Effects in Electrically Small Direction of Arrival Systems (4:10)

M. J. Slater, C. M. Schmitz, D. L. Jones, J. T. Bernhard
University of Illinois at Urbana-Champaign, Urbana, IL

Electrically small direction finding fosters a new generation of functionality in vehicle-mounted and unit-borne environment awareness. Measurements of an electrically small direction finding system which mitigate common mode current on the feed cable will be presented. Effects of common mode current are detailed in terms of ambiguity and direction-finding accuracy.

17.4: Biological-Inspired RF Direction-Finding (DF) Techniques (4:30)

H. Xin
University of Arizona, Tucson, AZ

Two interesting biological-inspired DF techniques will be presented. First, an improved DF technique using just two antennas with a scatter in between them, inspired by the human auditory system in which the head functions as a low-pass filter at high frequency and provides additional magnitude cues, will be discussed. Second, a novel DF method using only one ultra-wideband (UWB) antenna, which is also inspired by the human auditory system, will be presented.

17.5: Biologically Inspired Direction of Arrival Estimation **(4:50)**

M. Akcakaya, A. Nehoral
Washington University in St. Louis, St. Louis, MO

C. H. Muravchik
Universidad Nacional de La Plata, La Plata, Argentina

A biologically inspired antenna array to achieve high direction of arrival (DOA) estimation performance with small aperture arrays is proposed. The approach is inspired by the coupled ears of a parasitic fly called Ormia ochracea. The biologically inspired coupling as a multi-input multi-output filter was implemented and its effect on DOA estimation accuracy was demonstrated.

Session 18

NON-SILICON RADIATION-HARDENED MICROELECTRONIC TECHNOLOGIES

Wednesday, 23 March / 3:30 – 5:10 pm / Sun & Surf

Chair: **L. J. Palkuti**
DTRA, Ft. Belvoir, VA

Co-Chair: **B. Wilson**
DTRA, Ft, Belvoir, VA

18.1: Radiation Hardening of Carbon Nanoelectronics (3:30)

C. D. Cress
Naval Research Laboratory, Washington, DC

J. J. McMorrow
Global Strategies Group (North America) Inc., Crofton, MD

J. T. Robinson
Naval Research Laboratory, Washington, DC

B. J. Landi, S. M. Hubbard
Rochester Institute of Technology, Rochester, NY

S. R. Messenger
Naval Research Laboratory, Washington, DC

Total-ionizing-dose (TID) effects have been shown to alter the performance of single-walled carbon-nanotube and graphene field-effect transistors. The structures and passivation techniques aimed at improving the performance and radiation tolerance of these devices will be reported.

18.2: Radiation Effects in Carbon Devices: It's All About the Substrate (3:50)

M. L. Alles, J. L. Davidson, S. T. Pantelides, R. D. Schrimpf, D. M. Fleetwood, K. I. Bolotin, E. X. Zhang, C. X. Zhang, J. Greaving, B. Wang, A. Newaz
Vanderbilt University, Nashville, TN

J. U. Lee
University at Albany, Albany, NY

C. D. Cress
Naval Research Laboratory, Washington, D.C.

W. Lu
Fisk University, Nashville, TN

The mechanisms of radiation effects in carbon-based electronic materials (nanotubes, graphene, and diamond) are investigated for a range of structural, material, and fabrication variants using DFT simulations and experimental characterization.

18.3: Total-Dose Radiation Effects in Carbon-Nanotube Transistors (4:10)

Y. Fu, J. Zhang, C. Wang, C. Zhou
University of Southern California, Los Angeles, CA

R. Wormuth, V. Tyree, M. Fritze
USC Information Sciences Institute, Marina del Rey, CA

P. McMarr
University of Southern California, Los Angeles, CA

H. Hughes
Naval Research Laboratory, Washington, DC

The purpose of the RadCNT Program is to characterize the fundamental mechanisms and charge-transport phenomena governing the interactions between ionizing and non-ionizing radiation with carbon-nanotube electronics. Initial results on the total-dose radiation effects on carbon-nanotube transistors based on multi-tube parallel-array FETs will be presented.

18.4: Structural and Electrical Response of Graphene-Based Devices Exposed to Gamma and Neutron Irradiation (4:30)

M. Fanton, R. Cavalero, D. Snyder
Penn State University, Freeport, PA

J. Robinson, M. LaBella, B. Heidrich, M. Hollander, Z. Hughes
Penn State University, University Park, PA

The work presented here focuses on the response of graphene and graphene devices to gamma and neutron irradiation. The primary areas of interest are (1) Permanent Damage: Displacement of C atoms from, and impurity atoms into, graphene films exposed to neutron and cleavage of C-C bonds by high-energy photons. (2) Real-Time Effects: The interactions between graphene and ionizing radiation to create trapped charges or additional charge carriers. The fundamental electrical, structural, and chemical response of graphene test structures were characterized after irradiation with gamma rays and neutrons at the Penn State University Breazeale nuclear reactor.

18.5: Inelastic Electron Tunneling Spectroscopy (IETS) Study of Ionizing Radiation Effects on High-k Gate Dielectrics for CMOS Transistors (4:50)

Z. Liu, S. Cui, T. P. Ma
Yale University, New Haven, CT

The use of Inelastic Electron Tunneling Spectroscopy (IETS) to study the basic mechanisms of ionizing radiation effects on high-k gate dielectrics, including changes in microscopic bonding structures and generation of traps, is presented. The principle of IETS will be discussed and some pertinent results presented.

THURSDAY, 24 MARCH

Session 19

ADVANCED POWER AMPLIFIERS (RF TO MM-WAVE)

Thursday, 24 March / 8:30 – 10:00 am / Space Coast

Chair: **C. W. Hicks**
Naval Air Systems Command, Patuxent River, MD

Co-Chair: **P. A. Maki**
Office of Naval Research, Arlington, VA

19.1: State-of-the-art GaN HEMTs for K- and Ka-Band Power Applications **(8:30)**

M.-Y. Kao, C. F. Campbell, T.-M. Chou, H.-Q. Tserng, D. Fanning, P. Saunier
TriQuint Semiconductor, Richardson, TX

The development and power performance at 23 and 35 GHz of 0.15-□m gate-length AlGaN/GaN HEMTs on SiC substrate. At 35 GHz and V_d = 20 V, 160-□m GaN devices with state-of-the-art power characteristics of ~ 3-W/mm output power density, greater than 10-dB linear gain, about 9.0-dB power gain, and 46–50% PAE will be demonstrated.

19.2: Low-Noise Components for Interference-Immune Receivers and STAR Applications **(8:50)**

A. Kurdoghlian, M. Micovic, C. Moyer, A. Margomenos, J. May, D. Chow
HRL Laboratories LLC, Malibu, CA

GaN MMIC components for an all-GaN RF receiver chain with sharply increased dynamic range, high linearity, high RF survivability, and lower overall noise figure.

19.3: Simultaneous Transmit and Receive (STAR): Transmitter Device Perspective **(9:10)**

J. Moon
HRL Laboratories LLC, Malibu, CA

Prospective challenges associated with the high-power STAR transmitter in EW and technical approaches to realize high-power low-noise broadband GaN power amplifiers with improved spectral purity and efficiency will be presented.

19.4: W-band, GaN Power Amplifier/Combiner **(9:30)**

J. Schellenberg, E. Watkins, D. Radovich
QuinStar Technology, Inc., Torrance, CA

A W-band solid-state power amplifier with an output power of 1.3 W at 94 GHz and greater than 1 W over the 93.5–97.0-GHz band will be presented. These SOA results were achieved by combining four GaN MMICs in a low-loss (>93% combining efficiency) septum combiner network.

BREAK **(10:00)**

Session 20

PHASED-ARRAY BEAMFORMING TECHNOLOGY

Thursday, 24 March / 8:30 – 10:00 am / Gold Cost

Chair: **T. W. Dalrymple**
AFRL, Wright-Patterson AFB, OH

20.1: A Wideband Multi-User Digital Beamforming Receiver for SIGINT Applications (8:30)

L. K. Patton, R. W. Hawley
Matrix Research & Engineering, Dayton, OH

P. E. Buxa, M. B. Longbrake
Air Force Research Laboratory, Wright-Patterson AFB, OH

The Multi-User Digital Beamforming Wideband Array Signal Processing (MUDWASP) receiver being developed by the Air Force Research Laboratory will be described. This includes a brief motivation for the receiver's development, as well as an overview of the main system components. Simulation and component testing results will also be presented.

20.2: Reconfigurable Array Manifold (RAM) Program Overview (8:50)

R. T. Manley
Raytheon, Dallas, TX

J. D. Reynolds
Air Force Research Laboratory, Wright-Patterson AFB, OH

The AFRL is executing a Reconfigurable Array Manifold (RAM) program to demonstrate the capabilities that a highly reconfigurable wideband AESA architecture can provide. An overview of the program, including the program objectives, the capabilities of the hardware, and a summary of the demonstrations planned once the RAM AESA is delivered to AFRL will be provided.

20.3: A Miniature Reconfigurable Transmit/Receive Beamformer for Steerable Beam Antenna Systems (9:10)

M. P. DeLaquil, C. E. Baucom, M. C. Owens
L-3 Communications ComCept Division, Rockwall, TX

By incorporating a switching network and high-power amplifier with both MMIC and board-level delay elements, a transmit/receive module with 4.35 nsec of true-time-delay beamforming capability is realized in a 3.5 x 4.75 in. package. Combining this with a composite antenna creates a low-cost, lightweight, active/passive steerable beam antenna system.

20.4: Scalable Reconfigurable Phased Arrays for Space (9:30)

B. G. Martin, A. Jacomb-Hood, S. Robertson, M. Enoch, A. Kaytes, E. Lier, P. Papula
Lockheed Martin Space Systems Company, Newtown, PA

Experiments and studies related to the ongoing development of autonomous modular plug-and-play building blocks, essential to the realization of scalable phased arrays for space, will be discussed. Results from experiments in distributed electrical power subsystems and free-space optical links are given as well as relevant trade study recommendations. In addition, the challenges associated with clock synchronization of distributed RF aperture arrays will be discussed.

BREAK (10:00)

Session 21

FAULT-TOLERANT COMPUTING FOR SPACE SYSTEMS

Thursday, 24 March / 8:30 – 10:00 am / Sun & Surf

Chair: **M. N. Lovellette**
Naval Research Laboratory, Washington, DC

Co-Chair: **L. Cohn**
Naval Research Laboratory, Washington, DC

21.1: Efficient Data-Processing Protection via Parallel Parity Computations (8:30)

R. Redinbo
University of California, Davis, CA

High-speed real-number data processing can be protected from the onset of internal computer errors by augmenting normal computations with parity operations in either hardware or software. Error-detecting procedures employ real number parity codes, either block or convolutional type, depending on the nature of the processing. Selectively restarting processing after error detection is an efficient overall protection strategy.

21.2: Multi-Core Fault Tolerance for Space (8:50)

S. P. Crago, J. P. Walters, R. Kost, K. Singh, J. Suh
University of Southern California / Information Sciences Institute, Arlington, VA

The shift to multi-core microprocessors has a significant impact on software and fault tolerance. For fault-tolerant systems, the inherent redundancy in multi-core presents opportunities. These opportunities and challenges will be explored and preliminary results of fault-tolerance techniques implemented on a multi-core architecture for space will be presented.

21.3: Fault-Tolerance Improvement through On-Chip Parallelism (9:10)

I. Troxel
SEAKR Engineering, Inc., Centennial, CO

Commercial microprocessor architecture trends have jumped into multi-core and there seems to be no going back. On-chip parallelism offers the potential for enormous performance improvements for many defense and intelligence community applications if effective tools to take advantage of inherent parallelism are developed and utilized. Fault mitigation techniques for multi-core processors including conventional methods applied in new ways and a few novel concepts made possible by features inherent to multi-core architectures will be explored. Techniques for single-event-effect radiation testing of multi-core processors, derived from single-core processor qualification methods, will also be included.

21.4: The MAESTRO Fault-Tolerant Spacecraft Processor **(9:30)**

R. Brees, A. Kleinosowski, E. Cannon, M. Cabanas-Holmen, W. Snapp, B. Buchanan, C. Neathery, J. Ballast
Boeing Research and Technology, Seattle, WA

Advanced spacecraft payload processors require leading-edge technology to achieve needed performance, but they must be reliable and fault tolerant. A design methodology that has been applied to advanced spacecraft processor designs in 90-nm CMOS will be described. Design methods that are incorporated into the design flow which provide fault tolerance, soft-error mitigation, and enhanced reliability will be described. A 50-GFLOP multi-core processor that has been fabricated and characterized will be described in detail.

BREAK **(10:00)**

Session 22

POWER MANAGEMENT FOR RF ELECTRONICS

Thursday, 24 March / 10:30 am – 12:00 pm / Space Coast

Chair: **A. Fayed**
Iowa State University, Ames, IA

Co-Chair: **D. Both**
NSA, Ft. Meade, MD

22.1: Noise-Spectrum Manipulation Techniques in Switching Power Converters (10:30)

C. Tao, A. Fayed
Iowa State University, Ames, IA

Techniques for switching noise spectrum manipulation in power converters will be presented. These techniques has the potential of enabling the powering of sensitive analog/RF circuits directly from switching regulators without any post-filtering or linear post-regulation, which results in much higher efficiency and longer battery life.

22.2: Power-Amplifier Techniques for Improved Efficiency (10:50)

N. M. Neihart
Iowa State University, Ames, IA

Efficient power delivery is a challenge in many RF systems. The use of space-time block codes as a means for reducing the required output power of the power amplifier and thereby improving the system efficiency is described. The first implementation of a fully integrated four-antenna transmitter based on space-time block codes is described.

22.3: An Efficient Light-Load DC-DC Converter for Low-Power Wireless Devices (11:10)

J. Hu, M. Ismail
Ohio State University, Columbus, OH

A light-load efficient DC-DC buck converter with an on-off keying modulated power train and pseudo-hysteretic voltage mode control is designed in 0.5-□m CMOS. The converter regulates a fixed 1-V output from a 3-V supply and achieved an efficiency >70% while delivering an output current from 5 to 500 □A.

22.4: Leveraging Silicon-on-Sapphire Performance Advantages in Power Management (11:30)

J. Swonger, P. Bacon, G. Wu
Peregrine Semiconductor, San Diego, CA

Peregrine Semiconductor's UltraCMOS® technology has demonstrated superior power-management performance as a result of its reduced device parasitics. A pass device having an R_{on} of less than 65-mΩ with a fail-safe control interface and a >90% efficient DC-DC converter will be discussed, including their inherent immunity to latchup and minimal radiation sensitivity.

LUNCH (12:00)

Session 23

GaN RELIABILITY

Thursday, 24 March / 10:30 am – 12:00 pm / Gold Coast

Chair: **S. Binari**
Naval Research Laboratory, Washington, DC

23.1: Relations between Accelerated Lifetest Results, Short-Term Drift, Initial Gate Current, and Current Collapse in GaN FET Technology **(10:30)**

J. Jimenez, U. Chowdhury, Y. Cui, H.Q. Tserng, C. Lee, E. Beam, T. Nagle, B. Murdock, P. Saunier
TriQuint Semiconductor, Richardson, TX

The connections between accelerated DC lifetest, initial gate current, and current collapse and short-term drift through a set of target experiments were analyzed, and the physics linking all these phenomena was explored.

23.2: Reliability Status of GaN/AlGaN HEMT MMICs on 100-mm SiC **(10:50)**

S. Sheppard, T. McNulty, J. B. Barner, J. Milligan, J. Palmour
Cree, Inc., Durham, NC

The technology status of 28-V GaN/AlGaN HEMT MMICs on 100-mm SiC substrates will be reported. The 100-mm process includes: (a) 180-pF/mm^2 metal-insulator-metal capacitors rated to a MTTF of 1x10^6 hours at 100 V and 85°C; (b)12-Ω/sq. NiCr thin-film resistors rated to 10 □W/cm^2 and 1 mA/mm; and (c) low-resistance source vias that are small enough to embed inside the transistor technology that is rated for an MTTF >1x10^7 hours at a 225°C junction temperature.

23.3: FLOORS: Toward Reliability Simulation **(11:10)**

M. E. Law
University of Florida, Gainesville, FL

For 10-year parts, actual testing to failure under normal operating conditions is not possible. Consequently, accelerated testing is used to estimate failure. However, the physics must be well understood so predicted lifetimes are accurate. Combined electro-thermal-mechanical defect simulations can make these projected GaN/AlGaN device lifetimes accurate.

23.4: Reliable GaN HEMT Technology for DoD Systems **(11:30)**

W.-B. Luo, B. Heying, M. Wojtowicz, I. Smorchkova, Y. Chen, P. P. Huang, W. Sutton, V. Gambin, A. Oki
Northrop Grumman, Manhattan Beach, CA

On the DARPA WBGS-RF program, NGAS has successfully developed a reliable GaN HEMT technology for high-power microwave and millimeter-wave applications. RF-driven lifetests have demonstrated high reliability needed for DoD and space systems, >10^6 hours of lifetime at an 150°C junction temperature. Reliability improvements were accomplished by identifying and mitigating the primary degradation mechanisms such as electrical-field-induced trapping and gate current stability. This accomplishment provides a solid technology foundation for insertion into future DoD radar, communication, and electronic-warfare applications.

LUNCH **(12:00)**

Session 24

SPACE COMPUTING

Thursday, 24 March / 10:30 – 11:30 am / Sun & Surf

Chair: **M. N. Lovellette**
Naval Research Laboratory, Washington, DC

Co-Chair: **J. P. Egan**
National Reconnaissance Office, Chantilly, VA

24.1: Priorities for Spacecraft Bus *vs.* Payload Processors (10:30)

R. Berger, D. Pirkl, D. Stanley
BAE Systems, Manassas, CA

J. Dowling
Synopsys, Inc., Columbia, MD

When designing a space processor aimed at high-performance payload applications as opposed to the conventional bus flight computer, the priorities and trades to optimize the design are very different. These trades are reflected in the decisions made for the RAD750® compared to the RADSPEED™ DSP chips.

24.2: The High-Performance Low-Power High-Reliability HyperX Processor (10:50)

J. H. Jones, M. B. Doerr, C. S. Dobbs, M. R. Trocino
Coherent Logix, Inc., Austin, TX

The HyperX low-power high-performance reliable many-core processor (or a rich fabric of HyperX processors) brings the advantages of high-performance computing to bear on applications requiring extreme mobility, small-form factors, and long-duration remote operations in extreme environments. These challenging applications cannot tolerate the size, weight, and energy demands of yesterday's solutions.

24.3: Understanding the Radiation Mitigation Techniques Employed on the Cisco Space Router (IRIS) (11:10)

C. Olson, E. Watko
Cisco Systems, Inc., Research Triangle Park, NC

I. Troxel
SEAKR Engineering, Inc., Centennial, CO

Through its use of multiple operating systems with differing techniques for software mitigation of radiation-induced events, the Cisco 18400 Space Router flying as a hosted payload aboard Intelsat's IS-14 satellite offers a unique platform from which to understand and evaluate the efficacy of modern high-speed commercial processors in a space environment.

LUNCH (11:30)

Session 25

EXTREME-ENVIRONMENT SYTEMS

Thursday, 24 March / 1:30 – 3:00 pm / Space Coast

Chair: **M. M. Mojarradi**
JPL, Pasadena, CA

Co-Chair: **B. Blalock**
University of Tenessee, Knoxville, TN

25.1: Electro-Mechanical Systems for Extreme Space Environments (1:30)

M. Mojarradi
California Institute of Technology, Pasadena, CA

T. R. Tyler
National Aeronautics and Space Administration, Hampton, VA

P. B. Abel
NASA, Cleveland, VA

G. Levanas
Alliance Spacesystems, Pasadena, CA

The advancements made in the area of developing integrated electro-mechanical technology to survive the stringent environment of the moon and other challenging space-exploration missions with minimal environmental protection will be described.

25.2: High Reliability Frequency Control for Extreme Environment Systems (1:50)

K. Sariri
Frequency Management International, Inc., Huntington Beach, CA

Demand for extreme-environment electronic components has expanded beyond the energy exploration and into advanced system requirements in automotive, jet-engine controllers, and various space missions. FMI has addressed the pressing needs for robust frequency-control components that operate under extreme environmental conditions including a temperature range of from -220 to +500°C.

25.3: Wide-Temperature High-Resolution Integrated Data Acquisition for Spectroscopy in Space (2:10)

B. J. Farahani, S. G. Krishna, S. Venkatesan, Z. Zhu
A. Kathuria, G. Gildenblat, H. Barnaby
Arizona State University, Tempe, AZ

The research conducted at Arizona State University in collaboration with Jet Propulsion Lab in designing a wide-temperature-range 20-bit 1-ksps sigma-delta analog-to-digital converter that maintains its performance across a 300°C variation in temperature will be summarized. The design uses a second-order sigma-delta modulator. By using novel design techniques, the 20-bit ADC achieves a signal-to-noise ratio (SNR) of 129 dB with a spurious-free dynamic range better than 80 dB while consuming 1.45 mw. The small figure-of-merit of 1.45 pJ/conversion is much better than that of state-of-the-art designs.

25.4: Universal Gate Driver IC for Harsh Environments (2:30)

R. L. Greenwell, B. M. McCue, L. Zuo, M. A. Huque, B. J. Blalock, L. M. Tolbert, S. K. Islam
University of Tennessee, Knoxville, TN

An SOI-based gate driver for high-temperature (200°C) operation is presented. This gate driver is targeted to drive wide-bandgap power switches for DC-DC converters and traction drives in hybrid electric vehicles. Successful operation of the circuit at high temperature will help to achieve higher power-to-volume and power-to-weight ratios for power electronics modules.

BREAK (3:00)

Session 26

OPTICAL INTERCONNECTS FOR MILITARY PLATFORMS

Thursday, 24 March / 1:30 – 3:00 pm / Gold Coast

Chair: **M. D. Gerhold**
Army Research Office, Research Triangle Park, NC

Co-Chair: **J. J. Liu**
Army Research Laboratory, Adelphi, MD

26.1: Board-to-Board Optical Interconnects within Aerospace and Missile/Munitions Systems **(1:30)**

C. Tabbert, C. Kuznia
Ultra Communications, Vista, CA

The productization of board-to-board optical interconnects within missile and munitions systems will be reported. These links can replace electrical routing between ICs and connectors with direct board-to-board optical interconnects. The use of 850-nm VCSEL-based transceivers within these aerospace and missile/munitions systems will be discussed.

26.2: Free-Space Optical Interconnect for Reconfigurable Space Radar **(1:50)**

S. V. Robertson, J. T. Sroga, B. G. Martin
Lockheed Martin, Newtown, PA

Scalable reconfigurable antenna arrays for future space ISR applications require high-speed fiber-optic cables to support computationally intensive beamforming operations. However, autonomous array operations cannot support the stringent mechanical alignment tolerances required to mate/de-mate conventional fiber-optic connectors. The alignment-tolerant free-space optical interconnects based on expanded beam technology were experimentally investigated.

26.3: Rugged Optical Interconnect for Data Remoting in Military Environments **(2:10)**

M. Gross, A. Lenihan, A. Husain
Ziva Corp., San Diego, CA

A rugged high-speed fiber-optical interconnect is presented. Utilization of non-resonant optoelectronic devices only (no lasers) and coarse wavelength division multiplexing makes the interconnect rugged, especially with high tolerance to temperature change. A wide array of applications was identified and a prototype designed for mobile radar was fabricated and tested.

26.4: 1000-Gb/s Hybrid Macro for Direct-on-Die Integration of Terabit Optical Link Interconnect in Large Silicon CMOS SOCs **(2:30)**

T. E. Wilson, P. Farrell, J. Notor, C. Frost, D. Gerogantas, S. Williams, A. Leuciuc, M. Mengele, J. O'Keefe, J. Ebner, W. Evans, E. Naviasky
Cadence Design Systems, Inc., Columbia, MD

R. Zemach, N. Margalit, R. Gabzu, S. Stepanov, K. Hasharoni, J. Levy, M. Mesh
Compass Electro-Optical Systems, Netanya, Israel

A prototype 5 x 5 two-dimensional array of 8-Gbit/sec per channel integrated optical links was fabricated in a hybrid silicon/VCSEL/photodetector assembly implementing an orthogonal optical interface to a fiber bundle. A 65-nm CMOS IC with 25 complete self-testing serdes, including full clock data recovery, loopback, and BIST in each pixel achieved <12.5 mW/Gbit/sec. The IC included parallel data interface circuitry for direct interface to a parallel 500-MB/sec 16-bit-wide data streams and individually addressable pixels with drive current trim, TIA, and equalization adjustment. The CMOS IC was hybridized to VCSEL and photodiode arrays. Testing demonstrated a BER less than 10^{-12}. The array was a prototype section of a large-scale macro array to be placed directly in the center of a CMOS network processor IC to implement a 200-m OM2 terabyte chip-to-chip optical link .

BREAK **(3:00)**

Session 27

N/MEMS RELAYS FOR MICROMECHANICAL DIGITAL LOGIC

Thursday, 24 March / 1:30 – 3:00 pm / Sun & Surf

Chair: **R. Polcawich**
Army Research Laboratory, Adelphi, MD

27.1: Development of a PZT MEMS Switch Architecture Intended for Low-Power Digital Applications (1:30)

R. Proie, Jr.
George Washington University
and
Army Research Laboratory, Washington, DC

R. G. Polcawich, J. S. Pulskamp, T. Ivanov
Army Research Laboratory, Adelphi, MD

M. Zaghloul
George Washington University, Washington, DC

A novel low-power piezoelectric MEMS digital architecture has been developed, fabricated, and characterized. The architecture is based on a unique relay structure capable of performing any two-input Boolean operations with a single relay. Fabricated relays have demonstrated repeatable and reliable operation at 1.5 V with a static power draw under 1 pW.

27.2: Energy-Efficient Piezoelectric Aluminum Nitride Nano-Switches for Mechanical Computing (1:50)

Z. Guo, N. Sinha, G. E. Wabiszewski, R. W. Carpick, A. De Hon, G. Piazza
University of Pennsylvania, Philadelphia, PA

The latest advancements in the design and fabrication of thin film (50–100 nm) AlN actuators for the synthesis of energy-efficient nanomechanical switches will be reported. Tribological and electrical characterization of a selected set of switch contact materials will also be discussed with the intent of developing highly reliable mechanical computing elements.

27.3: Mechanical Computing Redux: Relays for Integrated-Circuit Applications (2:10)

T.-J. K. Liu, E. Alon
University of California at Berkeley, Berkeley, CA

V. Stojanovic
Massachusetts Institute of Technology, Cambridge, MA

D. Markovic
University of California, Los Angeles, CA

An overview of a reliable micro-relay developed for logic applications will be presented. Relay-based circuit design will be discussed, and demonstrations of functional relay logic circuits will be presented. Relay scaling for improved device density and performance will be described, and the energy-efficiency benefit of a scaled relay technology vs. a CMOS technology will be discussed.

27.4: Dynamic Spectrum Utilization and Performance Enhancement of Tunable Bandpass-to-Bandstop Reconfigurable Filters Using Advanced MEMS Switches **(2:30)**

E. J. Naglich, W. J. Chappell
Purdue University, West Lafayette, IN

Bandpass-to-Bandstop reconfigurable filters are designed and fabricated with advanced MEMS switches, and performance enhancements and new use cases are investigated. The latest MEMS switches offer higher isolation than solid-state switches while still having relatively fast switching times, which greatly improves bandpass-to-bandstop filters in both modes of operation.

BREAK **(3:00)**

Session 28

NANOWIRE- AND CNT-BASED ELECTRONICS

Thursday, 24 March / 3:30 – 5:10 pm / Space Coast

Chair: **H. Manohara**
Jet Propulsion Laboratory, Pasadena, CA

Co-Chair: **B. Blalock**
University of Tenessee, Knoxville, TN

28.1: Suitability of Carbon-Nanotube Transistors for Low-Voltage Electronics (3:30)

A. D. Franklin, S. O. Koswatta, W. Haensch
IBM T. J. Watson Research Center, Yorktown Heights, NY

The first study on the scaling limits for channel and contact lengths in carbon-nanotube transistors will be presented. The linear improvement of device performance with an increasing number of nanotube channels has been demonstrated. With these new results, simulations of scaled carbon-nanotube-transistor performance show promise for a low-voltage technology.

28.2: A 0.4-□m CNTFET Technology for RF Applications (3:50)

M. Schroter
RFNano Corp., Newport Beach, CA
and
University of California, San Diego, CA

S. Mothes, D. Wang, S. McKernan, P. Kolev, N. Samarakone, M. Bronikowski, Z. Yu, P. Kempf
RFNano Corp., Newport Beach, CA

Depletion-mode CNTFETs with an 11-GHz maximum oscillation frequency and 14-dB available power gain at 1 GHz have been fabricated in an advanced stepper-based production-like fabrication process. A compact model is compared to the experimental CNTFET characteristics over bias and frequency.

28.3: Etching of Silicon Nanowires and CNTs Using Implanted Ga Ions (4:10)

M. J. Shearn, A. Scherer
California Institute of Technology, Pasadena, CA

M. D. Henry
Sandia National Laboratory, Albuquerque, NM

Implanted Ga layers, defined by a focused ion beam (FIB) as an etch mask for silicon and carbon, providing etch selectivities of >10000:1 and >3000:1, respectively, were used. Si nanowires and CNTs bundles are fabricated using an implanted Ga etch mask followed by an inductively coupled plasma reactive ion etching (ICP-RIE).

28.4: Carbon-Nanotube Field-Effect-Transistor-Based Differential Amplifier Circuits for Sensing Applications **(4:30)**

M. Chin, M. Ervin, C. Anton, M. Dubey
Army Research Laboratory, Adelphi, MD

Carbon-nanotube-based field-effect transistors (CNTFETs) show potential in the area of integrated amperometric sensors due to their high sensitivity to analytes, fast response times (seconds to minutes), and large surface area-to-volume ratios. This research demonstrates the design, fabrication, and testing of a CNTFET-based differential amplifier.

28.5: Carbon Nanomaterials as Sensor Elements for Nondestructive Evaluation in Aerospace Applications **(4:50)**

P. Williams, B. Wincheski, M. Rogge
NASA Langley Research Center, Hampton, VA

Progress in utilizing the piezoresistance of carbon nanotubes (CNTs) to produce strain sensors for the monitoring of structural components will be reported. Prototype sensor geometry, the optimization of CNT processing, and the transfer of CNT devices to polymer-based substrates will also be discussed as a basis for conformal sensors for NDE applications.

Session 29

SUB-MM-WAVE VACUUM ELECTRONICS

Thursday, 24 March / 3:30 – 5:10 pm / Gold Coast

Chair: **J. Albrecht**
DARPA/MTO, Arlington, VA

Co-Chair: **W. D. Palmer**
Army Research Office, Durham, NC

29.1: A 50-W 220-GHz Power Amplifier (3:30)

J. Tucek, M. Basten, D. Gallagher, K. Kreischer
Northrop Grumman Corp., Rolling Meadows, IL

As part of the DARPA HiFIVE program, Northrop Grumman is developing a vacuum electronic power amplifier operating at 220 GHz, capable of 50 W CW with a minimum bandwidth of 5 GHz. The compact design incorporates advanced cathode technologies, permanent magnetics, microfabricated power-combined folded waveguide RF circuits, and high-power MMIC driver amplifiers.

29.2: Sheet Electron Beam mm-Wave Travelling-Wave-Tube Amplifier (3:50)

M. Field, R. Borwick, V. Mehrotra, B. Brar
Teledyne Scientific, Thousand Oaks, CA

J. Zhao, Y.-M. Shin, D. Gamzina, A. Spear, A. Baig, L. Barnett, N. Luhmann
University of California at Davis, Davis, CA

T. Kimura, J. Atkinson, T. Grant
Communications and Power Industries, Palo Alto, CA

Y. Goren
Teledyne MEC Vacuum Electronics, Rancho Cordova, CA

D. E. Pershing
Beam-Wave Research Inc., Bethesda, MD

A development program aimed at producing a travelling-wave-tube amplifier with significant gain and power at 220 GHz in a compact and lightweight package has been initiated. This paper provides an overview of the program, describing the development of the cathodes, the MEMS-fabricated interaction structure, and the sheet beam gun.

29.3: Compact THz Power Amplifiers (4:10)

J. Tucek, M. Basten, D. Gallagher, K. Kreischer
Northrop Grumman Corp., Rolling Meadows, IL

J. Liu, H. Choi
Electron Energy Corp., Landisville, PA

R. Mihailovich
Teledyne Scientific and Imaging, LLC, Thousand Oaks, CA

As part of the DARPA THz Electronics program, Northrop Grumman is developing vacuum electronic power amplifiers operating at 0.670, 0.850, and 1.030 THz. These devices are based on microfabricated, folded waveguide RF circuits and are designed to deliver 10–100 mW of saturated output power, operating up to 50% duty. A quasi-optical approach based on free-space transmission is being employed for the I/O networks.

29.4: Development of a 670-GHz Extended Interaction Klystron Power Amplifier **(4:30)**

D. Chernin
Science Applications International Corp., McLean, VA

R. Dobbs, M. Hyttinen, A. Roitman, D. Berry
Communications and Power Industries, Georgetown, Ontario, Canada

K. Nguyen, V. Jabotinsky, D. Pershing, E. Wright
Beam-Wave Research, Inc., Bethesda, MD

F. Maiwald, T. Gaier
Jet Propulsion Laboratory, Pasadena, CA

M. Blank
Communications and Power Industries, Inc., Palo Alto, CA

J. Calame, B. Levush
Naval Research Laboratory, Washington, DC

N. S. Barker, R. Weikle
University of Virginia, Charlottesville, VA

J. Neilson
Lexam Research, Redwood City, CA

J. Booske
University of Wisconsin, Madison, WI

Extended interaction klystrons (EIKs) have been demonstrated at frequencies up to 229 GHz, and the technologies on which they are based are poised to advance into the THz regime. This presentation will provide an update on our team's work to develop EIKs operating at 670 GHz and above, while meeting demanding metrics for output power, gain, bandwidth, and efficiency.

29.5: Techniques for Microfabrication and Characterization of Wideband Distributed Beam Amplifier Circuits at 220 GHz **(4:50)**

C. D. Joye, J. P. Calame, P. B. Larsen, D. Park, R. Bass,
B. Levush
Naval Research Laboratory, Washington, DC

K. Nguyen, D. Pershing
Beam Wave Research, Inc., Bethesda, MD

M. Garven
Scientific Applications International Corp. (SAIC), McLean, VA

Microfabrication techniques used to construct several types of distributed beam millimeter-wave planar amplifier circuits using ultraviolet photolithography will be reported. 220-GHz sheet beam grating amplifier circuits have been successfully fabricated and electromagnetically characterized using vector network analysis over a wide frequency range of 75–325 GHz.

Session 30

GENERAL POSTER SESSION

Thursday, 24 March / 9:00 am – 12:00 pm / Citrus Crown Ballroom

30.1: Ka-Band Coupled-Cavity Traveling Wave Tube (CCTWT)

M. Cusick, R. Begum, D. Gajaria, J. Legarra, B. Stockwell
Communications and Power Industries, Inc., Palo Alto, CA

D. K. Abe, M. Daniell, B. Levush, J. Pasour, A. N. Vlasov
Naval Research Laboratory, Washington, DC

A. Burke, D. Chernin, I. A. Chernyavskiy, J. Petillo
Scientific Applications International Corp. (SAIC), McLean, VA and Billerica, MA

A significant state-of-the-art power and bandwidth Ka-band coupled-cavity traveling wave tube (CCTWT) successfully developed, built, and tested at the Communications and Power Industries (CPI). The advances of this Ka-band TWT and another Ka-band CCTWT currently under development and testing at CPI will be reviewed.

30.2: 3-D FPGA System Exploration Study

N. Checka, C. Shirk
GoofyFoot Labs, Plano, TX

Field-programmable gate arrays (FPGAs) can benefit significantly from the increased device density and shift in interconnect distribution offered by 3-D integration. Simulation results that determine the performance impact of 3-D integration by comparing the point-to-point delays and energy consumption of two 3-D FPGA architectures will be presented. Results on how current 3-D technologies perform when used with deeply scaled (*i.e.*, 45 nm and below) device technologies are also presented. Finally, opportunities for designing low-power 3-D FPGAs will be discussed.

30.3: Demonstration of Software-Defined Multi-Gbps Modem Technology for Ka-Band Satellite Communications

D. G. Landon, J. Y. Sun, J. S. Winn, S. Laraway, W. K. McIntire, J. L. Metz, F. J. Smith
L-3 Communication Systems-West, Salt Lake City, UT

R. N. Simons, E. G. Wintucky
NASA Glenn Research Center, Cleveland, OH

The state-of-practice data rates for NASA's space-to-Earth links typically range from a few Mbps to about 150 Mbps. The experimental results demonstrating very high data rates on the order of multi-Gbps through a Ka-band space traveling-wave-tube amplifier using software-defined modems and bandwidth efficient modulation techniques will be presented. These results when included in a RF-link budget analysis show that the data rates can be enhanced by an order of magnitude (20x) or higher.

30.4: Delay-Insensitive Asynchronous Circuits for Operating under Extreme Temperatures

B. Hollosi, J. Di, S. C. Smith, H. A. Mantooth
University of Arkansas, Fayetteville, AR

Space electronics are exposed to wide temperature swings, resulting in timing violations in synchronous ICs. Due to its flexible timing requirements, delay-insensitive (DI) asynchronous logic is an ideal choice for extreme temperature digital electronics. The testing results of a DI 8031 microcontroller under high and low temperatures will be presented.

30.5: Demonstration of Octave-Bandwidth Metamaterial Boundary with Negligible Loss for RF Applications

E. Lier
Lockheed Martin, Newtown, PA

A new methodology for the design of metamaterials based on dispersion engineering has been used to demonstrate an octave-bandwidth negligible-loss metaliner inside a horn antenna. The results help to prove wrong the common perception that all metamaterials have narrow bandwidth and high losses.

30.6: Qualification of Radiation-Hardened Non-Volatile Magneto-Resistive Memory for Space

T. Romanko, R. R. Katti, D. Erstad, M. Smith, M. Cagle
Honeywell, Inc., Plymouth, MN

Through a combination of 150-nm rad-hard silicon-on-insulator (SOI) CMOS and magneto-resistive memory technology, the first non-volatile MRAM 1-MB memory product has been brought to production for strategic space applications. Qualification results and a roadmap to MRAMs greater than 64 MB will be presented presented.

30.7: Highly Integrated Low-Cost High-Linearity HPA Up-Convert Ka-Band MMIC

M. R. Lyons
ViaSat-Advanced Microwave Products, Gilbert, AZ

A highly integrated low-cost high-linearity HPA up-convert Ka-Band MMIC will presented. Each transmit chain section is scrutinized for optimal system performance, including a high-linearity mixer topology, on-chip filtering, and high-gain HPA. The system-on-chip methodology reduces overall transmit chain size, cost, and complexity while still maintaining high performance. A high gain of 42.7 dB and a saturated output power of 37.2 dBm for this interated design makes it ideal for low-cost compact Ka-band transmit systems.

30.8: A Sub-Threshold FPGA: Energy-Efficient Reconfigurable Logic

B. H. Calhoun, Y. Zhang, S. Khanna, K. Craig, Y. Shakhsheer, J. Lach
University of Virginia, Charlottesville, VA

A large set of emerging DoD applications demand ultra-low-power (ULP) operation for integrated circuits (ICs), but many of these applications do not require large enough volume to justify the costs of custom-IC design. Commercial FPGAs provide the needed flexibility to solve this problem, but they are not designed for ULP operation. A subthreshold FPGA fabric will be presented and the results from a 90-nm test chip that show how the design improves energy, delay, and area relative to a conventional FPGA circuit modified to work at low voltage will be reported.

30.9: High-Efficiency Envelope-Tracking GaN HEMT Power Amplifiers for MUOS Handheld and Manpack Applications

J. J. Yan, C. Hsia
University of California at San Diego, La Jolla, CA
and
MaXentric Technologies, LLC, San Diego, CA

D. F. Kimball
MaXentric Technologies, LLC, San Diego, CA

In order to increase the agility of the warfighters, a reduction in the weight and size of the handheld/manpack units can be achieved by using high-efficiency power amplifiers. By using our ET-PA, an efficiency of >46%, in a worst-case scenario, has been demonstrated with a 6.75-dB PAPR “notched” MUOS signal, meeting linearity without using predistortion.

30.10: Optimal High-Efficiency Amplifier Design: From Device to System

J. Lachapelle, D. White, C. Fisher, R. Ramahadran, S. Davis
Draper Laboratory, Cambridge, MA

T. Palacios, O. Saadat
Massachusetts Institute of Technology, Cambridge, MA

As customers demand even smaller miniature communications systems with longer lifetime, it has become clear that the PA and its associated battery conditioning, dominate both real-estate and lifetime constraints. Draper engineers are currently working on a variety of improvements, from device to system, that allow further extension of lifetime while decreasing real estate in real systems. A target design, including device and total system integration, with the goal of advancing the state of the art for a 1–2 W design for unique needs will be reviewed.

30.11 A Linear, High-Efficiency GaN Power Amplifier Operating at 74 GHz

B. Kim, J. Schellenberg, E. Watkins
QuinStar Technology, Inc., Torrance, CA

J. Yan, D. Kimball
University of California at San Diego, La Jolla, CA

A highly linear and efficient 74-GHz GaN MMIC PA which uses digital predistortion (DPD) and envelope tracking (ET) will be reported. For 64QAM 10-MHz modulation, this PA achieves an ACPR of better than –40 dBc with an efficiency improvement factor of greater than 2 (from 4.2 to 10.2%).

30.12: Measurement and Analysis of GaN Power Amplifier Variations & Impact to Active Antenna Performance

R. Palumbo
Raytheon Co., Andover, MA

The measured bias dependence of an X-band GaN MMIC power-amplifier insertion amplitude and phase variation were analyzed. These results were then extrapolated to predict the degradation in array performance for an active array. This works helps to quantify bias-dependent performance variations for GaN power amplifiers integrated into active phased-array systems.

30.13: A Fault-Tolerant Spacecraft Processor

W. Snapp
The Boeing Company, Huntington Beach, CA

Advanced spacecraft payload processors require leading-edge technology to achieve needed performance, but they must be reliable and fault-tolerant. A design methodology that has been applied to advanced spacecraft processor designs in 90-nm CMOS will be described. Design methods that are incorporated into the design flow which provide fault tolerance, soft-error mitigation, and enhanced reliability will be described. A 50-GFLOP multi-core processor that has been fabricated and characterized will be described in detail.

30.14: Device Architecture for Millimeter-Wave Power Amplifiers Using SiGe HBTs

T. J. Farmer, B. Huebschman, E. Viveiros, H. A. Hung
Army Research Laboratory, Adelphi, MD

A. Darwish
American University in Cairo, New Cairo, Egypt

M. E. Zaghloul
George Washington University, Washington, DC

A novel circuit architecture in silicon sermanium (SiGe) heterojunction bipolar transistors (HBTs)intended for use with power amplifiers at millimeter-wave frequencies is presented. Two prototypes of the architecture, two- and three-stage devices, have been simulated, fabricated, and measured using the IBM 8HP BiCMOS process. The prototypes serve as a verification of the circuit architecture at millimeter-wave. The architecture used for these devices represents a novel technique for customizing the bias voltage of an amplifier per application, increasing the achievable output voltage swing to improve output RF power, and potentially reducing, if not eliminating, matching circuitry for power amplifiers that may use the architecture at millimeter-wave frequencies. Simulation, layout, and measurement results are presented.

30.15: Thermally Stabilized Transmit/Receive Modules

J. Hoffman, L. Del Castillo, J. Miller, G. Birur
California Institute of Technology, Pasadena, CA

Improved TR module fabrication techniques using new materials and proven materials in new ways to increase RF power-density capacity while reducing thermal cycling and its negative effects, through improved thermal transfer, higher efficiency electronics, and a phase-change material thermal capacitor are being developed.

30.16: High-Performance Single-Crystal CMOS on Flexible Polymer Substrate

R. L. Chaney, D. R. Hackler
American Semiconductor, Inc., Boise, ID

FleX silicon-on-polymer technology provides high-performance CMOS that is flexible at the die and wafer levels. A brief overview of the FleX process followed by results from testing a variety of FleX circuits both as full thickness wafers and FleX wafers will be presented.

30.17: Development of a Miniaturized Scalable High-Voltage Module for Power Applications

P. Adell, L. Castillo, T. Vo, M. Mojarradi
Jet Propulsion Laboratory, Pasadena, CA

A miniaturized, scalable, and rad-hard high-voltage module was demonstrated as a proof-of-concept. The module is suitable for space applications. The design uses a commercial process that combines 0.25-mm complementary-metal-oxide semiconductor (CMOS) transistors with a high-voltage lateral double-diffused metal-oxide-semiconductor (DMOS) device (>600 V). The design was simulated, fabricated, and tested, and shows functionality up to 2.5 kV. Several radiation-hardening-by-design (RHBD) techniques were used to improve radiation hardness to over 100 krad.

30.18: W-Band Sheet-Beam Extended Interaction Klystron (EIK)

J. Pasour, B. Levush
Naval Research Laboratory, Washington, DC

K. Nguyen, E. Wright
Beam Wave Research, Inc., Bethesda, MD

A. Balkcum, J. Atkinson, M. Cusick
Communications and Power Industries, Inc., Palo Alto, CA

A 94-GHz sheet beam-extended interaction klystron (EIK) with saturated peak output power >5 kW is being developed. The EIK is powered by a 19.5-kV 3.3-A 0.32 mm x 4 mm sheet beam, which has been transported with less than 3% loss in a uniform 8.5-kG magnetic field. The gain at saturation of a three-cavity circuit is predicted to exceed 30 dB.

30.19: Patterned Metal Thin Films for Controlled Carbon Nanotube Growth

D. Magagnosc, B. M. Nichols
Army Research Laboratory, Adelphi, MD

The growth of single-walled carbon nanotubes (SWNTs) from patterned nickel-aluminum bilayered thin films was investigated. The effect of different film compositions and oxygen plasma treatments on the resulting density of SWNTs grown by chemical vapor deposition was studied.

30.20: High-Power-Bandwidth Product Ka-Band Helix TWT

K. C. Chae, D. A. Layman, R. J. Stolz
L-3 Communications, Torrance, CA

A successful effort to significantly expand the bandwidth and power-bandwidth product of a state-of-the-art high-power Ka-band helix TWT will be reported. This CW TWT is extremely compact and light weight, has excellent stability over the full bandwidth, and has high gain and good overall efficiency.

30.21: Semiconductor-Tuned High-T Superconductor Filters for Ultrasensitive RF Receivers (SURF): Technology Development and Evaluation

C. L. A. Cerny
Air Force Research Laboratory, Wright-Patterson AFB, OH

V. G. Fisher, J. T. McCartney, D. A. Ovenshire
Air Force Research Laboratory, Wright-Patterson AFB, OH and MacAulay-Brown, Dayton, OH

The DARPA/STO Semiconductor-Tuned High-Temperature Superconductor Filters for Ultrasensitive RF Receivers (SURF) Program was initiated for the purpose of detecting small signals in a dense background of radio-frequency (RF) interference. The specifications for these filters include exceptional operational bandwidth, low insertion loss, high out-of-band rejection, and microsecond tuning times, for addressing applications beyond those of commercially available switched-tuned or fixed-notch bandpass filters.

30.22: Mixed-Signal Silicon Germanium (SiGe): An Enabling Technology for Distributed Architectures in Extreme Environment Applications

R. J. Garbos
Aura Instrumentation, Inc., Mount Vernon, NH

Mixed-signal silicon germanium (SiGe) has been proven by the NASA ETDP program to operate over extreme environments while greatly reducing size, weight, and power (SWAP). How the results of the ETDP work can enable distributed architectures and the benefits of this architectural approach will be discussed.

30.23: Techniques for Healing RoC and SoC Systems

F. Kiamilev
University of Delaware, Newark, DE

Three techniques for calibrating (or healing) the performance of devices that incorporate multiple functions on a single-chip substrate such as Radio-on-a-Chip (RoC) or System-on-a-Chip (SoC) systems will be described. These techniques are modularity, stress testing, and proper statistical sampling. In our approach, stress testing is combined with proper statistical sampling to accelerate the transition from suboptimal to optimal (*i.e.*, healed) operation. As an example of our approach, a self-healing gigabit transceiver chipset will be described. The development of RF and IF VCO stimulus circuits that can be used for calibrating RoC systems will also be discussed.

30.24: Microspring Iinterconnects for Electronics Packaging

E. M. Chow
Palo Alto Research Center (PARC), Palo Alto, CA

Spring electrical contacts for test and packaging have many applications, including (1) lower-cost multi-chip modules (rework address KGD problem), (2) low-height chip stacking, (3) large die chip to board, (4) stress-sensitive MEMS/low-K die (springs compliant and absorb thermal mismatch), and (5) high-density (6 □m demonstrated).

30.25: Radiation-Tolerant Linear Regulator Featuring a CMOS Compatible SOI MESFET

W. Lepkowski, S. J. Wilk, T. Thornton
Arizona State University, Tempe, AZ
and
SJT Micropower, Inc., Fountain Hills, AZ

B. Bakkaloglu
Arizona State University, Tempe, AZ

P. S. Fechner
Honeywell Aerospace – Plymouth, Plymouth, MN

CMOS-compatible SOI MESFETs were utilized to create a cost-effective radiation-tolerant LDO for extreme environments. The LDO exhibits ultra-low dropout with fast and stable operation over all line and load conditions, from –196 to 150°C, and TID up to 1 Mrad(Si) without the need for an external capacitor.

30.26: SSPA Transmitter Development for High-Power TWTA Replacement in Current Military Systems

S. Behan,
CAP Wireless, Inc., Newbury Park, CA

M. Casto
Air Force Research Laboratory, Wright-Patterson AFB, OH

M. Lampenfeld, S. Hoover, P. Courtney, P. Jia, P. Daughenbaugh
CAP Wireless, Inc., Newbury Park, CA

A broadband, high-power microwave combining structure has been developed that enables significant advantages in design reuse, time to market, serviceability, maintainability, and reliability for microwave power-amplifier applications. This technology leverages existing and developing monolithic microwave integrated-circuit (MMIC) capability to replace vacuum devices for power amplification. State-of-the-art performance for high-power high-efficiency amplifiers has been demonstrated. The transition to current military-critical platforms is under way.

30.27: Experimental Demonstration of a Distributed Solar PV Power System, Integrated into a Modular Antenna "Tile" of a Scalable Reconfigurable Phased Array for Space

A. Kaytes, B. Martin, A. Jacomb-Hood, J. Teixeira, E. Lier, P. Papula
Lockheed Martin Space Systems Co., Newtown, PA

Experiments related to the development of a distributed electrical power system (solar arrays, batteries, charge, and DC regulation) for autonomous, modular, scalable, and low-cost-space active phased-array antennas will be described. Modular antenna "tiles" contain an integrated PV power system to operate the RF electronics, eliminating heavy centralized DC harnesses.

30.28: Memristive Behavior in Thin Anodic Titania

N. M. Neihart, S. Chaudhary
Iowa State University, Ames, IA

The memristive behavior in thin TiO_2 films fabricated by the brief electrochemical anodization of titanium has been studied. The effects of different anodization times and annealing are explored. Inherent oxygen vacancies at the bottom Ti/TiO_2 interface naturally lead to memristive switching in non-annealed films. It is found that annealing causes a collapse of the memristive switching behavior.

30.29: Trusted Facility Security Assessments: Trust in Manufacturing

N. Schumacher, S. Riccon, M. James
IBM, Bethesda, MD

In a global marketplace that seeks to reduce manufacturing costs by moving production capabilities offshore, how does the U.S. Government validate the "Trusted" status of its suppliers? The Trusted Facility Security Assessment provides a cost-effective repeatable value proposition to assess the security of a manufacturing capability.

30.30: 75-GHz 10-W GaN Power Amplifier with Radial Power Combiner

E. Watkins, J. Kuno, B. Kim, J. Schellenberg, K. Han
QuinStar Technology, Inc., Torrance, CA

D. Radovich
General Dynamics, Torrance, CA

Compact high-power amplifiers are needed in the 71–76 GHz region to enable high-speed 1–10 Gbps point-to-point data links for airborne, ground, and satellite applications. The design and performance of a 75-GHz 10-W SSPA using efficient radial power combiners and GaN MMIC power amplifiers will be reported.

30.31: Data Segregation in DWDM Networks

T. Berger, S. Braun
L-3 PHOTONICS, Carlsbad, CA

A new or existing single-optical-fiber infrastructure may simultaneously carry multiple types of data with complete isolation. Cross-talk between multiple independent data channels transmitted over a DWDM network can be eliminated by applying a limiting amplifier to each channel after the optical to electrical conversion.

30.32: Component and Technology Development toward an Adaptable RF System

S. Lardizabal, C. Wang, R. Molfino
Raytheon Co., Andover, MA

C. Moody, B. Pillans
Raytheon Co., Dallas, TX

Results of a study to the understand underlying design, fabrication and component technologies required to realize wideband reconfigurable RF circuits will be presented. An adaptable 2–18-GHz T/R chain was developed, and a reconfigurable GaN power-amplifier building block was designed and fabricated. Performance results will also be presented.

30.33: Comparison of Ku-Band Low-Noise-Amplifier Noise Figures Obtained from GaAs, GaN, SiGe, and SOI CMOS Technologies

C. Wolthausen, A. Kleinosowski, G. Kromholtz, R. Bonebright, F. Reinman, B. Kormanyos, M. Florian, M. Steeds
Boeing Research and Technology, Seattle, WA

The measured noise-figure results obtained for Ku-band low-noise amplifiers designed and fabricated in a diverse range of semiconductor process technologies including TriQuint Semiconductor's 0.15-□m gallium-arsenide (GaAs) PHEMT and MHEMT processes, HRL's 0.15-□m gallium-nitride (GaN) process, IBM's 8HP silicon-germanium (SiGe) process, Jazz Semiconductor's SBC18H2 silicon-germanium process, and IBM's 45-nm SOI12SO silicon-over-insulator (SOI) process will be presented and compared. The design details will be presented along with the measured versus modeled performance data. The performance advantages and disadvantages of each process technology at Ku-band will also be discussed.

30.34: SiGe HBT Stacked Power Amplifier at Millimeter Wave

T. J. Farmer, B. Huebschman, E. Viveiros, H. A. Hung
Army Research Laboratory, Adelphi, MD

A. Darwish
American University in Cairo, New Cairo, Egypt

M. E. Zaghloul
George Washington University, Washington, DC

The implementation of silicon germanium (SiGe) heterojunction bipolar transistor (HBT) based power amplifier that uses a novel circuit architecture at millimeter wave is discussed. Implemented in the IBM 8HP BiCMOS 0.12-□m process, the amplifier has been measured to have a PSAT = 19.0 dBm with a PAE of 11.47% in an area of 0.21 mm^2, at a center frequency of 30 GHz. This amplifier presents a level of RF output power competitive with that of current literature; however, the required area for the amplifier is substantially smaller than current implementations. The device architecture used in the amplifier provides a tool for silicon designers to achieve high power density, customizable bias, and a way to minimize, if not eliminate, matching circuitry at millimeter-wave frequencies. The amplifier implementation represents a competitively high-power millimeter-wave implementation of the device architecture. Simulation, layout, fabrication, and measurement results are presented.

30.35: Characterization of a 130-nm RadHard-by-Design ASIC Library Technology

R. Dumitru, P. Milliken, T. Farris, C. Hafer, T.-W. Wu, R. Rominger, H. Gardner, K. Bruno, D. Wilkin
Aeroflex Colorado Springs, Colorado Springs, CO

Radiation-hardness characterization has been performed on a RadHard-by-Design ASIC Library designed using a 130-nm commercial process. Test-chip results are presented, illustrating the ASIC library performance and radiation-hardness response. The total ionizing dose data for commercial and annular discrete transistors will be reviewed along with single-event effects data.

30.36: Switched-Tone Non-Linear Radar for Remotely Characterizing RF Devices

G. J. Mazzaro, A. F. Martone
Army Research Laboratory, Adelphi, MD

When illuminated by specially designed waveforms, an RF device can generate spectral content different from that used to probe it. This content can be used to characterize the device. Here, switched-tone frequency sweeps are designed to excite a front-end filter non-linearity pair. Experiments demonstrate that switched-tone responses may be captured remotely.

30.37: 3DIC High-Performance I/O, RF, and Multicore Circuits

W. R. Eisenstadt, R. Bashirullah
University of Florida, Gainesville, FL

Researchers at the University of Florida have placed a large number of circuits in the areas of high-speed I/O characterization, RF IC passive elements, on-chip characterization s-parameter standards, and a multicore array on the MIT LL 3D SOI IC run. In particular, GTL and CML circuits have been placed on various tiers of the 3DIC to examine the effects of TSVs on high-speed transients and data communications. In addition, A SOLT s-parameter calibration set and an inductive load has been defined in the 3DIC to examine the issues of measuring deeply embedded structures inside the 3DIC tier stack. Measurements are on-going and the measurements of successful 3DIC circuit designs will be reported.

30.38: Single-Event-Effects Characterization of Analog, Digital, and Low-Power Electronics Designed in a Multiple-Tiered SOI Process

T. D. Loveless
Vanderbilt University, Nashville, TN

Circuits were designed and fabricated using the MIT Lincoln Labs 3DSOI 150-nm process to characterize single-event effects. Circuits were tested with heavy ions; generated transients were measured on all tiers of the die.

30.39: A Picosecond Multiphase PLL Architecture with Time-to-Digital Calibration

K. Zhou
University of New Hampshire, Durham, NH

A time-to-digital converter (TDC) for GHz PLLs for use in the 3D silicon-on-insulator (SOI) process is proposed. The proposed TDC effectively reduces the phase mismatch in the 3D process. The TDC structure presented in this design replaced the conventional long Vernier delay line (VDL) and achieved a 2-psec timing resolution.

30.40: Integrated Indium Phosphide and Silicon Germanium Technology Millimeter-Wave Tuners

H. Levitt
Naval Research Laboratory, Washington, DC

In an enhanced mixer circuit, the MIXCASC node swings in response only to common-mode signal components, while remaing stiff to differential signal components, thereby improving CMRR and differential output amplitude balance.

Session 31

STUDENT POSTER SESSION

Thursday, 24 March / 9:00 am – 12:00 pm / Citrus Crown Ballroom

31.1: Circuit-Simulator-Compatible Models of Electromagnetic Circuit Structures for Co-Site Interference Analysis

C. S. Saunders, M. B. Steer
North Carolina State University, Raleigh, NC

Interactions among co-located radio transceivers can lead to significant interference, which degrades the performance of a communications link. Effective methods of combating co-site interference involve isolating non-linear elements in the transceivers from high-power interfering signals by controling antenna coupling and filtering. Models can be developed which permit the electromagnetic behavior of linear circuit elements, such as coupled antennas and filters, to be incorporated into a circuit simulator, for analysis without needing an electromagnetic field solver. The methods used to generate these models and verify their passivity will be discussed.

31.2: Design, Fabrication, Iteration, and Testing of the Superlattice LED Infrared Projection System and Associated Electronics

R. McGee, F. Kiamilev, N. Waite, C. Lange
University of Delaware, Newark, DE

The creation and testing of a cryogenic integrated infrared projection system combining large two-dimensional arrays of superlattice light-emitting diodes (SLEDs) with a custom driver IC and FPGA-based control system will be described. It covers a range of disciplines, design decisions, systems-engineering issues, and personal observations on the process of the design, fabrication, iteration, and testing of the 68 x 68 SLEDs system. Several testing sessions showed the unique functionality and capabilities in several important areas such as apparent temperature exceeding 1000 K, rise and fall time of a few microseconds, and over 90% functional yield. The work provides the foundation for the 512 x 512 SLEDs projection system currently in development.

31.3: Linearity Analysis for Adaptable Power Amplifiers Using Loadline Translation

D. L. Ryan, M. A. Reece
Morgan State University, Baltimore, MD

The trade-off between efficiency and linearity plays an important role in amplifier design. The best efficiency performance of an amplifier occurs at the point when the amplifier is displaying non-linear characteristics. A mathematical analysis was performed to develop a bias adaptation technique that assist in identifying a more efficient bias without the degradation of the amplifier linearity.

31.4: A Hardened-by-Design Bias Circuit Utilizing Sensitive-Node Active Charge Cancellation (SNACC)

R. Blaine, J. Kauppila, W. T. Holman, L. Massengill
Vanderbilt University, Nashville, TN

S. Armstrong, B. Olson
NAVSEA Crane, Crane, IN

A novel RHBD technique was applied to a bootstrap current source. This technique, called sensitive-node active charge cancellation (SNACC), compensates for injected charge at critical nodes in analog and mixed-signal circuits by using a combination of structures for charge sharing and current mirroring. The SNACC technique applied to the current source is verified using simulations of the bias circuit in a 90-nm CMOS process.

31.5: Smart Jamming Antenna

M. J. Radway, D. S. Filipovic
University of Colorado at Boulder, Boulder, CO

A simple method for placing nulls at arbitrary locations in the pattern of a multi-armed spiral antenna is presented and is validated by computer simulation and measurement. It was found that by adjusting the excitation weights on the arms, the null locations can be made essentially independent of frequency.

31.6: Towards the On-Chip Miniature RF Ion Trap for Chemical Detection

J. D. Maas, W. J. Chappell, Z. Ouyang
Purdue University, West Lafayette, IN

Progress towards on-chip RF chemical detection is realized through advanced packaging techniques in creating highly precise circuit-integrated small-scale ion-trap mass analyzers. At a fraction of the RF drive potential, dynamic waveform operation is enabled using a discrete RF amplifier.

31.7: Standoff Acoustic Shear Wave Imaging Using LFM Chirps

G. Garner, M. B. Steer
North Carolina State University, Raleigh, NC

Shear-wave seismic-acoustic imaging incorporating laser vibrometers has been successfully used to detect buried landmines using single-tone excitation. The use of linear frequency-modulated (LFM) chirps is proposed to exploit wideband resonant behavior. This technique captures more information about complex elastic inhomogeneities while being more tolerant to noise.

31.8: An Analysis of Error-Detection Techniques for Arithmetic Logic Units (ALUs)

R. C. Bickham, D. B. Limbrick, W. H. Robinson, B. L. Bhuva
Vanderbilt University, Nashville, TN

The scaling in VLSI systems magnifies the need for cost-effective error-detection techniques to improve system reliability. Area, timing, and power analysis of selected error-detection techniques are evaluated for arithmetic logic units.

31.9: A Hybrid X-Band Low-Noise Gallium Nitride Amplifier on Liquid-Crystal Polymer Substrate

A. Trippe
Georgia Institute of Technology, Atlanta, GA

K. Groves, P. L. Orlando III, A. Mattamana, R. Fitch, J. Gillespie, T. Quach
Air Force Research Laboratory, Dayton, OH

J. Papapolymerou
Georgia Institute of Technology, Atlanta, GA

A GaN HEMT device is used to design a hybrid single-stage LNA on a LCP substrate at X-band frequencies. By using a LCP substrate, a low-cost high-perfomance design can be achieved. The design process is demonstrated, including the design of the bondwire interconnects to improve LNA performance. This work demonstrates the first hybrid GaN-based LNA on a LCP substrate and will further enable the investigation of 3-D GaN-based modules on LCP.

31.10: Optimal Characterization of RF Circuits with Unknown Insertion Loss

A. K. Mikkilineni, S. Gelfand, D. King-Smith, E. J. Delp
Purdue University, West Lafayette, IN

An optimal detection method for RF front-ends with unknown random parameter perturbationsthat is shown to perform significantly better than previously published feature based methods based on empirical observations is presented.

31.11: Fully Differential mm/sub-mm Wave CMOS Amplifiers

Q. J. Gu
University of Florida, Gainesville, FL

Z. Xu
HRL Laboratories, Malibu, CA

M.-C. F. Chang
University of California, Los Angeles, CA

An effective design and verification methodology to build CMOS ultra-high-frequency amplifiers with fully differential structures will be presented. The scheme is validated in several mm/sub-mm-wave CMOS amplifiers: 7-dB NF W-band LNA, W- and D-band PAs with higher output power, larger gain, and superior efficiency compared with the state of the art.

31.12: Statistical Fault-Injection and Analysis at the Register Transfer Level Using the Verilog Procedural Interface

C. T. Toomey
Vanderbilt University, Nashville, TN

B. D. Sierawski, A. Sternberg
Institute for Space and Defense Electronics, Nashville, TN

D. B. Limbrick
Vanderbilt University, Nashville, TN

B. L. Bhuva, L. W. Massengill, W. H. Robinson
Institute for Space and Defense Electronics, Nashville, TN

R. Wong, S. Martin
Cisco Systems, Inc., San Jose, CA

A methodology to calculate the architectural vulnerability factor of a given design and its sub-modules has been developed. Fault injection and analysis are completed at the register-transfer level using the Verilog procedural interface. Test designs include both an 8-bit microprocessor and a 1.1-million flip-flop ASIC.

31.13: Application of a Modified Nelder-Mead Algorithm for Calibrating RF Analog Integrated Circuits

E. J. Wyers, M. B. Steer, C. T. Kelley, P. D. Franzon
North Carolina State University, Raleigh, NC

In-situ calibration of RF analog ICs is important to ensure proper operation over process, voltage, temperature, and aging variations, especially in deep-submicron technologies. A hybrid optimization algorithm for calibration using Nelder-Mead with modifications to handle digital calibration knobs is presented. Performance of the algorithm has been verified with three test cases, resulting in substantially fewer required function evaluations compared to exhaustively searching the digital knob settings.

31.14: LNA Linearization at the Ka Band Using 0.13-□m SiGe Technology

J. J. McCue, W. Khalil
Ohio State University, Columbus, OH

L. Orlando, K. Groves, A. Mattamana, T. Quach, G. Creech
Air Force Research Laboratory, Wright-Patterson AFB, OH

An investigation of LNA linearization at the Ka band is described. Several linearization techniques are used and their effects on IP3 quantified. These techniques include inductive degeneration, robust biasing, IM3 cancellation, and a novel linearization technique that makes use of bias adjustment by means of an RF power detector.

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NOTES

GOMACTech–11 CONFERENCE SCHEDULE

DOUBLETREE HOTEL, ORLANDO, FLORIDA

	GOMACTech Timetable	Convention Center Lobby	Universal Center	Space Coast	Gold Coast	Sun & Surf	GOMACTech Timetable	
Monday, 21 March	7:00–8:30 am	Tutorial 1 Only Registration	.....	.....	.....	.....	7:00–8:30 am	Monday, 21 March
	8:30–12:00 pm	.....	**Tutorial 1** Trusted Suppliers Summit		.....	.....	8:30–12:00 pm	
	9:00–5:00 pm	General Registration	.....	.....	.....	.....	9:00–5:00 pm	
	LUNCH 12:00–1:00 pm	.....	**TUTORIAL 1 LUNCH (Universal Center)**	.....	.....	.....	LUNCH 12:00–1:00 pm	
	1:00–5:00 pm	.....	**Tutorial 1 continued** Trusted Suppliers Summit	.....	**Tutorial 2** End to End Electronics	**Tutorial 3** SOI-Enabled Technologies for 3D Circuit Integration and Ultra Low Power Applications	1:00–5:00 pm	
Tuesday, 22 March	7:00–5:00 pm	Registration	.....	.....	.....	.....	7:00–5:00 pm	Tuesday, 22 March
	8:30–10:00 am	.....	**PLENARY SESSION** Introductory Comments, Awards, Keynote Address	.....	.....	.....	8:30–10:00 am	
	BREAK 10:00–10:30 am	.....	.....	**BREAK**			BREAK 10:00–10:30 am	
	10:30–12:00 pm	.....	**KILBY LECTURES**	.....	.....	.....	10:30–12:00 pm	
	LUNCH 12:00–1:30 pm	Exhibits (12:00–8:00 pm)	.....	**LUNCH (Universal Center)**			LUNCH 12:00–1:30 pm	
	1:30–3:00 pm	.....	.....	**Session 1** Graphene RF Electronics	**Session 2** Emerging Semiconductor Technologies I	**Session 3** Trusted Electronics Research	1:30–3:00 pm	
	BREAK 3:00–3:30 pm	.....	.....	**BREAK**			BREAK 3:00–3:30 pm	
	3:30–5:00 pm	.....	.....	**Session 4** Graphene Electronics	**Session 5** Adaptive RF/BIST and Calibration	**Session 6** Trusted Electronics Applications I	3:30–5:00 pm	
	6:00–8:00 pm	.....	**EXHIBIT RECEPTION (Citrus Crown Ballroom)**				6:00–8:00 pm	
Wednesday, 23 March	7:00–5:00 pm	Registration	.....	.....	.....	.....	7:00–5:00 pm	Wednesday, 23 March
	8:30–10:00 am	.....	.....	**Session 7** 3DIC I	**Session 8** Advanced RF/ Mixed Signal Circuits	**Session 9** Trust in ICs	8:30–10:00 am	
	BREAK 10:00–10:30 am	.....	.....	**BREAK**			BREAK 10:00–10:30 am	
	10:30–12:00 pm	.....	.....	**Session 10** 3DIC II	**Session 11** RF Circuits for Wireless Sensors	**Session 12** Trusted Electronics Applications II	10:30–12:00 pm	
	LUNCH 12:00–1:30 pm	Exhibits (8:00–3:30 pm)	.....	**LUNCH (Universal Center)**			LUNCH 12:00–1:30 pm	
	1:30–3:10 pm	.....	.....	**Session 13** Power Electronics I	**Session 14** Emerging Semiconductor Technologies II	**Session 15** Radiation-Hardened Microelectronics Designs	1:30–3:10 pm	
	BREAK 3:00–3:30 pm	.....	.....	**BREAK**			BREAK 3:00–3:30 pm	
	3:30–5:00 pm	.....	.....	**Session 16** Power Electronics II	**Session 17** Antenna Applications	**Session 18** Non-Silicon Radiation-Hardened Microelectronics Technologies	3:00–5:00 pm	
	6:00 pm	.....	**WEDNESDAY EVENING SOCIAL House of Blues – La Nouba, Cirque du Soleil (separate registration fee)**				6:00 pm	
Thursday, 24 March	7:00–3:00 pm	Registration	.....	.....	.....	.....	7:00–3:00 pm	Thursday, 24 March
	8:30–10:00 am	.....	**Poster Sessions 30 and 31** (9:00–12:00 pm)	**Session 19** Advanced Power Amplifiers (RF to Millimeter Wave)	**Session 20** Phased-Array Beamforming Technology	**Session 21** Fault Tolerant Computing for Space Systems	8:30–10:00 am	
	BREAK 10:00–10:30 am	.....	.....	**BREAK**			BREAK 10:00–10:30 am	
	10:30–12:00 pm	.....	.....	**Session 22** Power Management for RF Electronics	**Session 23** GaN Reliability	**Session 24** Spacing Computing	10:30–12:00 pm	
	LUNCH 12:00–1:30 pm	.....	.....	**LUNCH (Universal Center)**			LUNCH 12:00–1:30 pm	
	1:30–3:00 pm	.....	.....	**Session 25** Extreme Environment Systems	**Session 26** Optical Interconnects for Military Platforms	**Session 27** N/MEMs Relays for Micromechanical Digital Logic	1:30–3:00 pm	
	BREAK 3:00–3:30 pm	.....	.....	**BREAK**			BREAK 3:00–3:30 pm	
	3:30–5:00 pm	.....	.....	**Session 28** Nanowire & CNT Based Electronics	**Session 29** Sub-Millimeter-Wave Vacuum Electronics		3:00–5:00 pm	