GOMACTech-12

Government Microcircuit Applications
and
Critical Technology Conference

PROGRAM

"Spanning the Spectrum:
Innovations in
Micro-Technologies
for System Supremacy"

March 19 – 22, 2012

Bally's Hotel
Las Vegas, Nevada

www.gomactech.net

GOMACTech-2012
FINAL PROGRAM
CONTENTS

WELCOME

The GOMACTech-12 Program Committee warmly welcomes you to this year's conference in Las Vegas, Nevada, 19–22 March. GOMACTech is the pre-eminent conference for the review of developments in microelectronic devices, circuits, and applications for government systems. GOMACTech was established in 1968. GOMACTech is an unclassified, Export-Controlled event that requires all participants to be U.S. Citizens or legal U.S. Permanent Residents.

This year, our conference theme, “Spanning the Spectrum: Innovations in Micro-Technologies for System Supremacy,” focuses on technologies that operate at bands and frequencies that are of specific interest to defense applications. The new functionalities available to global consumers, particularly for commercial communications, have also affected the strategy for the defense space. Complementing the commercial inundation of low-frequency SoCs, firmware, and software, we will highlight the emerging device and integration technologies that will spur material development and identification of integration constraints and opportunities.

The topical sessions will focus on developments and accomplishments ranging from components to systems within selected ongoing government-sponsored programs. Technical sessions include:

Advanced Optical Technologies for Communications
Modular RF Technologies
Radiation Effects in Novel Materials
EW Components
Digital Phased-Array Technology
Rad-Hard Design
Space Processing
Next-Generation Spacecraft Data Bus
Sub-100-nm Rad-Hard
Trusted Electronics
Thermal Management

The conference content for this year includes several tutorials and open meetings on Monday, 19 March. The first tutorial is “Trusted Suppliers Industry Day,” hosted and planned by the Trusted Suppliers Steering Group. The tutorial’s objective is to gather members of industry and government agencies representing the interests of integrated-circuit and electronics producers who are focused on serving defense and aerospace applications that are trusted. The theme of this session is “Sustainability of the Trusted Supply Base” and is planned for the entire day (8:30 am to 5:00 pm).

The second tutorial will focus on “Radar Electronic-Warfare Basics.” This tutorial will focus on the most recent developments in electronic-warfare relevant technologies, capabilities, and needs and will be presented by Aram Partizian (GTRI) on the afternoon of Monday 19 March.

The third tutorial on Monday afternoon, “DoD Advanced Electronics Community of Interest,” is organized by the Office of the Assistant Secretary of Defense for Research and Engineering [ASD(RE)]. The Communities of Interest have been designated as collaboration tools for the scientists, engineers, technology executives, acquisition staff, and operators within DoD. This tutorial will instruct users on how to gain access, post submissions, and interact with personnel across the department in order to (1) foster technical discussion among subject matter experts, (2) coordinate and plan ad-hoc and strategic activities, and (3) facilitate rapid, technically accurate, broadly vetted responses to queries from DoD leadership and Congress.

The final event on Monday is an open sidebar discussion regarding post-2013 fabrication approaches and options for accessing leading-edge semiconductor technologies.

The conference formally opens on Tuesday morning, 20 March, with an outstanding Plenary Session which includes a Keynote Address by Dr. William Howard, Co-Chair of the Trusted Foundry Program Study, who will speak on "*Findings of the Third Party Independent Study of the Trusted Foundry Program."*

The Keynote will be then followed by the Jack S. Kilby Lecture Series which will consist of the following three presentations: Dr. Robert Doering, Senior Fellow and Technology Strategy Manager at Texas Instruments, will speak on *"Prospects for 'Beyond CMOS' Devices;"* Professor Ken O, Director of the Texas Analog Center of Excellence (TxACE), will speak on *"Silicon Integrated Circuits for Sub-Millimeter-Wave Frequencies and Beyond";* and Dr. Daniel Josell, *Leader, Thin Film and Nanostructure Processing Group, National Institute of Standards and Technology, Gaithersburg, MD, will speak on "Metallizations for Advanced Interconnects."*

The plenary, technical, and topical sessions are the major venues for information exchange at the conference. Other opportunities for technical interaction are provided by the Exhibits Program that includes major IC manufacturers and commercial vendors of devices, equipment, systems, and services for nearly every facet of the electronics business. The exhibition opens on Tuesday at noon and runs through Wednesday, 21 March at 4:00 pm. On Tuesday evening, attendees can network in a relaxing atmosphere during the Exhibitors' Reception. Wednesday evening features the conference banquet, which will be held at the Paris Casino & Hotel followed by a short bus ride to Treasure Island Resort for a performance of *Mystere by Cirque du Soleil*. On Thursday morning, 22 March, a Poster Session that includes our annual student poster competition will be held.

This year's technical program is a result of the hard work and enthusiasm of the GOMACTech-12 Technical Program Committee. The committee members discussed and collaborated on the topics and presentations. The quality of the conference reflects this comprehensive team effort. We hope that you find GOMACTech-12 an enlightening and rewarding experience. Thank you for your active participation.

Romeo del Rosario
Conference Chair

Daniel Radack
Technical Program Chair

REGISTRATION

All GOMACTech-12 sessions will be held at Bally's Hotel in Las Vegas, Nevada. Both check-in and on-site registration will take place in the hotel's Grand Salon

Conference check-in and on-site registration hours:

Monday, 19 March – 7:00 am – 8:30 am (Tutorial 1 only)
Monday, 19 March – 9:00 am – 5:00 pm
Tuesday, 20 March – 7:00 am – 5:00 pm
Wednesday, 21 March – 7:00 am – 5:00 pm
Thursday, 22 March – 7:00 am – 3:00 pm

SECURITY PROCEDURES

The GOMACTech Conference is an Unclassified, Export-Controlled event that requires participants to be U.S. Citizens or legal U.S. Permanent Residents. All registrants must provide proof of U.S. Citizenship or Permanent Resident status prior to being permitted entry into the conference. Additionally, a signed **Non-Disclosure Statement** will be required.

You may prove U.S. citizenship with any of the following:
U.S. Passport
Birth Certificate **AND** valid government-issued photo ID
Naturalization Certificate **AND** valid government-issued photo ID

The following are NOT proof of citizenship:
Voter registration card
Driver's license

GOMACTech TUTORIALS

Three tutorials of interest to the GOMACTech community are a special feature of the conference. The tutorials are all being held on Monday, 20 March. There is no additional fee for the Tutorials 2 & 3, but individuals must be registered for the Conference and must indicate their intention to attend a specific tutorial on their registration form. Tutorial 1 includes a lunch. The fee for Tutorial 1 is $20.

Tutorial 1: Trusted Suppliers Industry Day

Monday, 19 March, 8:00 am – 5:00 pm
Bally's Hotel, Bronze Room 3&4

Organizer:
Harry Kellzi, Teledyne

The National Trusted Suppliers Industry Day returns to GOMACTech for the third year. The objective is to gather members of industry and government agencies representing the interests of trusted integrated-circuit and electronics producers who are focused on serving the defense and aerospace industry. This industry day is organized by the Trusted Suppliers Steering Committee, and Harry Kellzi from Teledyne will be moderating the event. Some of the key issues include accreditation activity and criteria; emerging defense policy; and demand for trusted supplies, trust solutions, and oppor-

tunities for industry to work together and with government for further progress in this area. The program begins with status and updates of DoD policy, the accreditation process, and programmatic initiatives. Distinguished government as well as industry invited speakers will kick off the event. Later, industry representatives will discuss their perspectives in Trusted microelectronics requirements and sustainability issues. In the afternoon session, a moderated discussion, with panelists representing both industry and government, will take on topics that are frequently being asked by industry participants.

Agenda

7:00 am	Registration/Continental Breakfast
8:00 am	Welcome and Introduction *Harry Kelzi, Teledyne*
8:15 am	Keynote *Kristen Baldwin, DDR&E*
9:00 am	The Trusted Foundry Program *David Pentrack, DMEA*
9:30 am	Defense Microelectronics Activity *TBA*
9:45 am	**BREAK**
10:00 am	DoD Microelectronics Requirements *Brian Cohen, Institute for Defense Analyses*
10:45 am	IBM's Perspective *TBA*
11:15 am	NSA's Microelectronics Future Perspective *Tony Chemoske, NSA*
12:00 pm	**Luncheon Speaker:** *Don Davidson, Jr., DoD/CIO*
1:15 pm	Sustainability from the Government's Perspective *Don Davidson, Jr., DoD/CIO* *Kristen Baldwin, DDR&E*
2:15 pm	Trusted Suppliers' Customers *OEMs*
3:15 pm	**Break**
3:30 pm	Future of Government Microelectronics *Brian Cohen, Institute for Defense Analyses* *Tony Chemoske, NSA* *John Franco, DTRA*
4:00 pm	Wrap-up

Tutorial 2: Radar Electronic-Warfare Basics

Monday, 19 March, 1:00 – 5:00 pm
Bally's Hotel, Bronze Room 2

Organizer:
Aram Partzian, Georgia Tech Research Institute

This tutorial provides an overview of the fundamental concepts of radar electronic warfare, including different types of noise and deceptive jamming as well as radar electronic protection concepts. The discussion will present a variety of electronic-attack and electronic-protection approaches as well as a few data examples from test events

Presenters:
TBA

Tutorial 3: DoD Advanced Electronics Community of Interest
Monday, 19 March, 1:00 – 5:00 pm
Bally's Hotel, Bronze Room 2

Organizers:
Romeo del Rosario, Army Research Officer

The DoD Communities of Interest (CoIs) are comprised of scientists, engineers, technology executives, acquisition staff, and operators with common technology interests. The CoIs are established to (1) foster technical discussion among subject matter experts, (2) coordinate and plan adhoc and routine activities, and (3) facilitate rapid, technically accurate, broadly vetted responses to queries from DoD leadership and Congress.

Communities of Interest provide a place for sharing new ideas, technical directions and technology opportunities; to jointly plan programs, influence EXCOM budget plans, measure technical progress; and to report on technology state of health.

Communities of Interest serve as visible and enduring structures to integrate technology efforts throughout the large, widely dispersed, sometimes fragmented DoD S&T enterprise. They provide DoD S&T corporate understanding and memory, while also serving as a place for new staff to get up to speed quickly.

Another important function of the Communities of Interest is to provide the timely identification of critical areas and opportunities.

Presenters:
Paul Ryan, *SES ASD (R&E)*
Valerie Thomas, *SES ASD (R&E)*
Jammi Cash

LUNCHES

Lunch will be provided on Tuesday, Wednesday, and Thursday. The Wednesday Luncheon will include a presentation of great interest to the GOMACTech community by Mr. Joshua Alspector, Research Staff Member, Information Technology and Systems Division, Institute for Defense Analyses, Alexandria, VA.

EXHIBITION

An exhibition comprised of commercial vendors exhibiting products of interest to the GOMACTech community is an integral part of the conference. All attendees are reminded to visit the exhibition when they have some free time. The Exhibit Hall is located in the hotel's Gold/Silver Ballroom. Coffee breaks will be held in the exhibit area when they coincide with the exhibition's hours of operation. On Tuesday evening, an Exhibitors' Reception, where attendees can mix in a relaxing atmosphere of food and good spirits, will be held. Exhibition hours are as follows:

Exhibition hours are as follows:

Tuesday, 20 March	12:00 pm – 8:00 pm
Wednesday, 21 March	9:00 am – 4:00 pm

List of Exhibitors (as of March 1)

3D Plus USA
Abtum, Inc.
Aeroflex
Allvia
American Semiconductor, Inc.
ASIC North, Inc.
BAE Systems
Boeing Co.
Cadence Design Systems
College of Nanoscale Science & Engineering
Corwil Technology Corp.
Cree, Inc.
Cypress Semiconductor
Endicott Interconnect Technologies
Equinix, Inc.
Honeywell International
HRL Laboratories, LLC
IBM
Integra Technologies, LLC
Interconnect Systems, Inc.
Jazz Semiconductor
Luma Innovations, Inc.
MicroAssembly Technologies, Inc.
Micro-RDC
Microsemi Corp.
Mobile Semiconductor
MOSIS Services
National Reconnaissance Office
Netronome Systems, Inc.
Nimbus Services, Inc.
NNSA's National Secure Manufacturing Center
Northrup Grumman Corp.
Nuvotronics LLC
ON Semiconductor
Peregrine Semiconductor
Photronics, Inc.
Ridgetop Group, Inc.
Rochester Electronics
RTI International
Sandia National Laboratories
Silicon Turnkey Solutions
Sivaco, Inc.
Sonnet Software
SVTC Technologies
SypherMedia International, Inc.
Tahoe RF Semiconductor, Inc.
TAPO (Trusted Access Program Office)
Tektronix Component Solutions
Tela Innovations
Teledyne Microelectronics
Teradyne Global Services Organization
Triad Semiconductor, Inc.
TriQuint Semiconductor
Ultra Communications, Inc.
Zephyr Photonics, Inc.

WEDNESDAY EVENING SOCIAL

Dinner at the Paris Casino & Hotel
Performance of "Mystere by Cirque du Soleil"

The GOMACTech-12 Special Event is truly a special event. Wednesday evening features the conference banquet, which will be held at the Paris Casino & Hotel, adjacent to Bally's Hotel, followed by a short bus ride to Treasure Island Resort for a performance of *Mystere by Cirque du Soleil*.

Buses will leave Bally's Hotel at 8:30 pm for the 9:30 pm show.

Tickets should be purchased in advance along with your conference registration.

Adults $25, Children (13 and under) $15.

HOTEL ACCOMMODATIONS

GOMACTech has reserved a block of rooms at Bally's Hotel at a special rate of $119, single or double. These rates are exclusive of applicable state and local taxes.

Reservations may be made on line at http://www.totalrewards.com/hotel-reservations?propCode=BLV& oupCode=SBGOM2

Or, by calling the hotel reservations department at 1-800-358-8777. Be sure to note that you are attending GOMACTech.

The deadline for reservations from the GOMACTech block is Monday, 27 February 2012.

CONFERENCE CONTACT

Anyone requiring additional information about GOMACTech should contact the Conference Coordinator, Glenys Natera, GOMACTech, 411 Lafayette Street, Suite 201, New York, NY 10003 (212/460-8090 x217), gnatera@pcm411.com.

GOMACTech-11 PAPER AWARDS

Paper awards based on audience evaluations from GOMACTech11 will include the George Abraham Outstanding Paper Award, a Meritorious Paper Award, a Best Poster Paper Award, and a Best Student Poster award. Presentation of these well-deserved awards will be made at the Plenary Session on Tuesday morning in the Platinum Ballroom. The GOMACTech-11 winners are:

The George Abraham Outstanding Paper Award (28.1)
A. D. Franklin, IBM T. J. Watson Research Center, Yorktown Heights, NY
"Suitability of Carbon-Nanotube Transistors for Low-Voltage Electronics"

Meritorious Paper Award (29.2)
M. Field, Teleydyne Scientific, Thousand Oaks, CA
"Sheet Electron-Beam mm-Wave TWT Amplifier"

Best Poster Paper Award (30.2 & 30.8)
N. Checka, Goofyfoot Labs, Plano, TX
"DFPGA System Exploration Study"

B. H, Calhoun, University of Virginia, Charlottesville, VA
"A Sub-Threshold FPGA: Energy-Efficient Reconfigurable Logic"

Best Student Poster Paper Award (31.3)
D. L. Ryan and M. A. Reece, Morgan State University
"Linearity Analysis for Adaptable Power Amplifiers Using Loadline Translation"

RATING FORM / QUESTIONNAIRE

Don't forget to vote for your favorite presentation this year before you leave the conference. A rating form/questionnaire is being handed out at conference check-in. To encourage submission of these forms, GOMACTech has a special gift for all attendees submitting a completed form. Please turn your form in at the Conference registration desk when you leave the Conference to receive your gift item.

SPEAKERS' PREP ROOM

The Bronze Room 4 has been designated as the speakers' preparation room and will be available during the hours the conference registration desk is open. Speakers are encouraged to use the Bronze Room 4 facilities to ensure compatibility with the meeting's AV equipment. Speakers having difficulties should request, at the conference registration desk, to see an AV operator. **Speakers are also asked to be at their assigned presentation room 30 minutes before the sessions begins to meet with their session chair.** An AV operator will be assigned to each technical session room.

CD-ROM PROCEEDINGS

The GOMACTech CD-ROM Proceedings, containing searchable, condensed versions of submitted papers presented at the Conference will be distributed to all registrants. Additional copies of the CD-ROM can be purchased at the Conference at a cost of $40.00 per CD.

Previously published as the GOMAC Digest of Technical Papers, Volumes I–XXVII, this publication is the only record of the conference. Previous GOMAC Digests will, upon request, be made available to qualified Defense Technical Information Center (DTIC) users. Please call 1-800-225-3842 for bound or microfiche copies. Past Digests can be ordered by calling the above number and identifying the following accession numbers (please note that GOMAC was not held in calendar years 1985 and1995):

GOMAC-84 B113271	-86 B107186	-87 B119187
-88 B129239	-89 B138550	-90 B150254
-91 B160081	-92 B169396	-93 B177761
-94 B195015	-96 B212362	-97 B222171
-98 B235088	-99 B242763	-00 B254138
-01 B264749	-02 B275146	-03 M201604
-04 M201663	-05 M201849	-06 M202011
-07 M202134	-08 M202438	-09 M202646
-10 M202788	-11 M202918	

INFORMATION / MESSAGE CENTER

The Information/Message Center will be located adjacent to the GOMACTech Registration Desk at Bally's Hotel. The message center telephone number for incoming calls is 702/967-7377. Callers should ask to be transferred to the GOMACTech Registration Desk.

PARTICIPATING GOVERNMENT ORGANIZATIONS

Participating Government Organizations of GOMACTech-12 include: Department of Defense (Army, Navy, Air Force) ... National Aeronautics and Space Administration ... Department of Commerce (National Institute of Standards and Technology) ... National Security Agency ... Department of Energy (Sandia National Laboratories) ... Department of Energy (National Nuclear Security Administration) ... Defense Logistics Agency ... Department of Health and Human Services ... Defense Threat Reduction Agency ... Defense Advanced Research Projects Agency ... Advisory Group on Electron Devices ... Central Intelligence Agency ... National Reconnaissance Office

GOMACTech WEB SITE

Information on GOMACTech may be obtained through its Web site at www.gomactech.net.

TUESDAY, 20 MARCH

PLENARY SESSION

Tuesday, 20 March / 8:30 – 11:30 am / Platinum Ballroom

Opening Remarks **(8:30–8:45)**

Romeo del Rosario, GOMACTech-12 General Chair
Army Research Laboratory, Adelphi, MD

GOMACTech-11 Awards **(8:45–9:00)**

Keynote Address **(9:00–9:30)**

Dr. William G. Howard
Independent Consultant, Co-Chair, Trusted Foundry Program Study, Scottsdale, AZ
"Findings of the Third Party Independent Study of the Trusted Foundry Program"

BREAK **(9:30–10:00)**

Jack S. Kilby Lecture Series **(10:00–11:30)**

Dr. Robert Doering
Senior Fellow and Technology Strategy Manager
Texas Instruments, Dallas, TX
"Prospects for 'Beyond CMOS' Devices"

Professor Kenneth K. O
Director, Texas Analog Center of Excellence,
University of Texas at Dallas, Dallas, TX
"Silicon Integrated Circuits for Sub-Millimeter-Wave Frequencies and beyond"

Dr. Daniel Josell
Leader, Thin Film and Nanostructure Processing Group, National Institute of Standards and Technology, Gaithersburg, MD
"***Metallizations for Advanced Interconnects"***

LUNCH **(11:30–1:00)**

Session 1

TECHNOLOGY DIRECTIONS I: NRI/FCRP

Tuesday, 20 March / 1:00 – 3:00 pm / Bronze Room 1

Chair: **J. Welser**
Semiconductor Research Corp., Durham, NC

Co Chair: **D. J. Radack**
Institute for Defense Analyses, Alexandria, VA

1.1: **Midwest Institute for Nanoelectronics Discovery** (MIND) **(1:00)**

A. Seabaugh
University of Notre Dame, South Bend, IN

1.2: **Western Institute for Nanoelectronics (WIN)** **(1:20)**

K. Wang
UCLA, Los Angeles, CA

1.3: **Southwest Academy of Nanoelectronics (SWAN)** **(1:40)**

S. Banerjee
University of Texas, Austin, TX

1.4: **Institute for Nanoelectronics Discovery and Exploration (INDEX)** **(2:00)**

J. Ung Lee, A. E. Kaloyeros
College of Nanoscale Science and Engineering, State University at Albany, Albany, NY

The overarching goal of the INDEX Center is to explore all the facets of the development of post-CMOS devices and architectures. The post-CMOS device efforts and the strategy to integrate these devices into the advanced 300-mm fab line will be discussed.

1.5: **FCRP Program: Functional Engineered Nano Architectonics** **(2:20)**

BREAK **(3:00–3:30)**

Session 2

ADVANCED OPTICAL COMMUNICATIONS

Tuesday, 20 March / 1:00 – 3:00 pm / Bronze Room 2

Chair: **M. D. Gerhold**
U. S. Army Research Office, Research Triangle Park, NC

Co Chair: **J. J. Liu**
U.S. Army Research Laboratory, Adelphi, MD

2.1: Non-Hermetic Fiber-Optic Transceivers for Aerospace Applications (1:00)

C. Tabbert
Ultra Communications, Vista, CA

An opportunity exists to significantly reduce the cost of low-profile fiber-optic transceivers utilized in harsh-environment applications by exploiting advances made in optoelectronic (OE) packaging. Presently, the cost associated with traditional “hermetic can” (HC) packaging dominates the overall cost of transceivers fielded in the aerospace systems. While electronic components are commonly used in military avionics without hermetic packaging, OE components are relatively unproven. This paper describes a lower-cost alternative to transceiver packaging.

2.2: High-Frequency High-Resolution Analog-to-Digital Converter (1:20)

R. Zanoni, K. Jepsen, O. King, T. Cullen, M. Laliberte
Rockwell Collins, Inc., Columbia, MD

G. Fish, A. Fang
Aurrion, Inc., Santa Barbara, CA

J. Clark
Tektronix Component Solutions, Beaverton, OR

Military RF system designers have long known that wide bandwidth, high-resolution analog-to-digital converters (ADC) enable capabilities such as wideband SIGINT receivers and LPI/LPD radars. Under the DARPA RADAR program, a phase-modulated photonic ADC (pADC) has been demonstrated with performance that is not possible with existing electronic ADCs.

2.3: Rugged 10-Gbps Optical Interconnect for Military Applications (1:40)

A. Lenihan, A. Husain
Ziva Corp., San Diego, CA

C. Kryzak
Lockheed Martin Corp., Liverpool, NY

A high-speed fiber-optic interconnect will be presented. Required fiber counts are reduced compared to parallel link solutions, while ruggedization is realized through the use of non-resonant optoelectronic devices. A prototype module suitable for a number of applications, such as mobile radar, was designed and is being fabricated for testing.

2.4: Photonic Integrated Circuits as Key Enablers for Coherent Sensor and Communication Systems **(2:00)**

L. A. Coldren, L. Johansson, M. Rodwell, M. Lu, A. Sivananthan, J. Parker
University of California ar Santa Barbara, Santa Barbara, CA

InP-based photonic ICs (PICs), together with closely integrated electronic ICs, have recently been shown to enable robust, compact coherent optical communication and sensor systems that have not been possible in the past. Experimental results will illustrate these functionalities.

2.5: High-Speed Vertical-Cavity Surface-Emitting Lasers for Harsh-Environment Applications **(2:20)**

S. Lanka, D. Louderback, X. Jin, Z. Clark, D. Brady, S. Mahnkopf
Zephyr Photonics, Inc., Zephyr Cove, NV

In this paper, high-temperature and high-speed operation of vertical-cavity surface-emitting lasers (VCSELs) that can be used for optical interconnects in harsh-environment applications will be presented. These VCSELs demonstrate a maximum power of ~2mW and a minimum bandwidth of 8 GHz at an operating temperature of 125°C.

BREAK **(3:00–3:30)**

Session 3

ELECTRONIC-WARFARE COMPONENTS

Tuesday, 20 March / 1:00 – 3:00 pm / Bronze Room 3

Chair: **C. Dahlhauser**
ASD (R&E)/DASD, Washington, DC

Co Chair: **M. Potts**
AFRL, Wright-Patterson AFB, Dayton, OH

3.1: Electronic-Component Needs for Modern EW (1:00)

F. Klemm
Naval Research Laboratory, Washington, DC

The role of electronic warfare in modern combat has been significantly elevated in the last 10 years. The number of differing capabilities required to achieve the desired systems requirements in response to this need has also required an expanded growth. This paper will discuss the generalized component requirements essential to maintain and extend the responsive nature of EW.

3.2: Wideband Software Programmable RF Sensor Using a Monolithic Software-Defined Receiver CMOS Chip (1:20)

B. Analui, A. Goel, H. Hashemi
University of Southern California, Los Angeles, CA

A 50 MHz to 6 GHz software programmable RF sensor in a USB-dongle form factor has been demonstrated. The RF sensor utilizes a custom monolithic wideband software defined receiver chip and commercially available data converters and a microcontroller unit. The 130-nm CMOS chip is designed to be robust to various wide-band interference scenarios and includes the complete RF to base-band signal path as well as frequency synthesizers.

3.3: Microwave and Millimeter-Wave Front-End Subsystems for Wideband Direction Finding and Towed Decoys (1:40)

D. S. Filipovic, N. Sutton, N. Jastram, M. Radway
University of Colorado, Boulder, CO

The development of multi-octave wideband direction finding and decoy front-end subsystems operating up to V-band will be discussed. A fast and inexpensive prototyping approach for coaxial transmission line platforms will also be demonstrated. Millimeter-wave devices including transmission lines, resonators, filters, hybrids, *etc.* were designed and fabricated by using this approach. A low-cost two-element Vivaldi antenna array was designed, fabricated, and tested for amplitude-only and amplitude/phase direction finding front-ends. Direction finding functions were measured and two subsystems were compared over a 4.5:1 bandwidth. They were designed not only for easy scaling to higher frequencies but also straightforward for extension into multi-element linear and circular direction finding arrays. Finally, a high-power-capable antenna was designed and fabricated by using low-cost printed-circuit-board-based manufacturing. Excellent performance over a 18–40-GHz band with low VSWR, consistent radiation patterns with stable beamwidth, low-level cross-polarization, and WoW were measured. An antenna was developed for an AN/ALE 55-like small towed decoy platform.

3.4: Rectifying Nanoantenna Array-Based Common Optical/RF EM Threat Detection Sensor **(2:00)**

T. Rao, S. Fastert
Salbec, LLC, Southborough, MA

K. Kempa
Boston College, Chestnut Hill, MA

The ability to detect, identify, and localize intentional or unintentional radiated EM energy across RF and optical bands using low-cost small-sized low-weight low-power (SWAP) form-factor sensors has the potential to dramatically alter conventional approaches to threat detection and countermeasures. This paper describes a revolutionary common optical/RF EM threat sensor comprised of arrays of rectifying nanoantennas that has the potential to bring a unique broadband EM threat detection capability to the Navy.

3.5: Rapid Threat Detection and Identification Using Multi-Band Ultra-High-Resolution LADAR **(2:20)**

P. Roos, B. Kaylor, N. Greenfield, C. Keith, R. Reibel
Bridger Photonics, Inc., Bozeman, MT

At Bridger Photonics, Inc., (Bridger), ultra-high-resolution LADAR technology is being combined with state-of-the-art target identification algorithms to enable rapid detection, identification, and appropriate countermeasure response to potential threats. The system has a high potential to improve protection against surveillance, missile guidance, and targeting threats. In this paper, clear identification of mock threats out to 1 km with a predicted range of operation up to 20 km will be described.

BREAK **(3:00–3:30)**

Session 4

TECHNOLOGY DIRECTIONS II: FCRP

Tuesday, 20 March / 3:30 – 5:10 pm / Bronze Room 1

Chair: **J. Rogers**
Defense Advanced Research Projects Agency, Arlington, VA

Co Chair: **B. Weitzman**
Semiconductor Research Corp., Research Triangle Park, NC

4.1: Center for Materials, Structures, and Devices (3:30)

J. Bokor
University of California at Berkeley, Berkeley, CA

D. Antoniadis
MIT, Cambridge, MA

4.2: Interconnect Focus Center: Accomplishments and Future Prospects (3:50)

P. Kohl
Georgia Institute of Technology, Atlanta, GA

Transistor scaling has created denser and faster integrated circuits. However, scaling has also created major bottlenecks in on-chip and off-chip signal connectivity because wiring, power delivery, and cooling do not benefit from smaller component dimensions. In addition, systems have become power limited which limits interconnect options. The progress in electrical and optical connectivity, chip cooling, power delivery, and wireless technology within the Interconnect Focus Center will be review along with future device and system prospects.

4.3: Gigascale Systems Research Center (GSRC) (4:10)

S. Malik
Princeton University, Princeton, NJ

4.4: Center for Circuits and Systems Solutions (C2S2) (4:30)

L. Pileggi
Carnegie Mellon University, Pittsburgh, PA

C2S2 was formed to address the challenges of CMOS scaling as it reaches its physical limits. Research accomplishments include circuit designs and new opportunities for end-of-roadmap silicon, diverse more-than-Moore technologies, and promising post-silicon devices. Novel circuit designs are based on novel architectures that ignore boundaries that once stood between digital and non-digital modules.

4.5: Multiscale Systems Research Center (MuSyC) (4:50)

E. Lee, J. Rabaey
University of California at Berkeley, Berkeley, CA

Session 5

DIGITAL PHASED-ARRAY TECHNOLOGY

Tuesday, 20 March / 3:30 – 5:10 pm / Bronze Room 2

Chair: **T. W. Dalrymple**
AFRL, Wright-Patterson AFB, Dayton, OH

Co Chair: **Peter Buxa**
AFRL, Wright Patterson AFB, Dayton, OH

5.1: **Wideband SiGe MMIC-Based DREX Technology for X-Band Array Radars** **(3:30)**

R. G. Drangmeister, R. A. Stiffler, J. W. Myer, M. S. Raj, L. M. Johnson
Massachusetts Institute of Technology, Lexington, MA

P. E. Buxa, K. S. Groves, M. B. Longbrake, A. G. Mattamana, P. L. Orlando, V. J. Patel, T. W. Dalrymple, T. K. Quach
AFRL, Wright-Patterson AFB, Dayton, OH

B. K. Kormanyos, R. K. Bonebright
The Boeing Co., Seattle, WA

A miniaturized wideband digital receiver/exciter (DREX) technology for X-band phased-array radars will be described. The DREX architecture combines silicon germanium MMICs with high-speed data converters and digital processors to achieve up to 1-GHz instantaneous bandwidth. Progress developing a four-channel DREX test system for operation at 8–11 GHz will be reported.

5.2: **A Low-Cost Digital Array Radar Architecture** **(3:50)**

P. Clough, M. Harger, V. Pai
Purdue University, West Lafayette, IN

C. Fulton
University of Oklahoma, Norman, OK

T. Snow
Naval Surface Warfare Center Crane, Crane, IN

The Digital Array Radar architecture incorporates a robust feature set with a flexible digital beamformer in a low-cost panelized form factor which, when scaled up to a larger array, provides a solution to the digital-phased-array challenge for moderate bandwidths.

5.3: **Wideband Digital Receiver Exciter (DREX) Technology for Multi-Channel Phased-Array Radar** **(4:10)**

W. H. Weedon, J. A. Phillips, A. J. Muratori, T. P. Halloran, R. N. Weedon
Applied Radar, Inc., North Kingstown, RI

A four-channel wideband DREX for ground-based and airborne radar applications has been developed. The DREX is being integrated with a GFE-provided scalable panel array developed by Cobham Sensor Systems (San Diego, CA) in Applied Radar's rooftop radar test range. Test results along with bench test results for a SiGe-based MDREX chipset developed by AFRL and packaged in a module by MIT/LL will bw discussed.

5.4: Wideband Software-Defined Radar Technologies at X-Band (4:30)

M. Sullivan, K. Church, H. Xu
Azure Summit Technology, Inc., Fairfax, VA

Advances in digital technologies have enabled the implementation of software-defined digital receiver-exciter modules capable of supporting instantaneous bandwidths of 1 GHz or more. The cost, size, weight, and power of these modules is approaching levels that allow their practical use in phased-array radars.

5.5: Advancements in Low-Cost Phased Array Technology (4:50)

D. Ferwalt, S. Nelson, C. Ison, G. Pshsnychniak
Cobham Sensor Systems, San Diego, CA

Low-cost technologies are critical to future phased-array development. An introduction to low-cost MMICs and TR modules will be presented, along with several key technology development efforts at Cobham, including highly integrated MMICs and chipsets, innovative MMIC packaging and TR modules, and automation advancements. Measured results from low-cost phased arrays that utilize these technologies for both ground and airborne applications will be presented.

Session 6

GaN RF AMPLIFIERS

Tuesday, 20 March / 3:30 – 5:10 pm / Bronze Room 3

Chair: **P. A. Maki**
Office of Naval Research, Arlington, VA

Co Chair: **C. W. Hicks**
Naval Air Systems Command, Patuxent River, MD

6.1: Hybrid X-Band Power Amplifier Using Commercially Available Discrete GaN FETs **(3:30)**

C. F. Campbell, M. Poulton
TriQuint Semiconductor, Richardson, TX

This paper describes the design and characterization of a highly integrated X-band power amplifier that utilizes commercially available discrete GaN transistors. The compact design integrates all of the RF matching and bias circuitry on to ε_r = 36 circuit boards, one for the input and one for the output. This includes the DC blocks, RF bypasses, and RF chokes. Dimensions for the complete single-stage power amplifier are 9.8 x 8.6 mm. Measured results for the GaN power amplifier under pulsed bias conditions demonstrate an outpower of up to 76 W with an associated gain and power-added efficiency of 8.9 dB and 44%, respectively.

6.2: An Octave Bandwidth, High PAE, Linear Class-J GaN High-Power Amplifier **(3:50)**

K. Skowronski, S. Nelson, R. Mongia, H. Sheehan, S. Anderson
Cobham Sensor Systems, Richardson, TX

In this paper, the design and measured performance of a wideband (1.2–2.5 GHz) high-efficiency, high-linearity, Gallium Nitride (GaN) Class-J 200-W power amplifier (PA) will be reported. The Class-J PA output stages exhibit 45–62% power-added efficiency (PAE) and a near-maximum power match over > 2:1 bandwidth and an impressive 802.11-g WLAN linearity. This linear PA has 65–70-dB small-signal gain over this bandwidth.

6.3: A 4-bit Digital-Analog GaN Power Amplifier for Linearization and 40% Power Reduction with 64QAM Wideband Signals **(4:10)**

Tim LaRocca
Northrop Grumman, Redondo beach, CA

6.4: Enabling High-Performance W-band Systems Using GaN Technology **(4:30)**

M. Micovic, A. Margomenos, A. Kurdoghlian
HRL Laboratories, Malibu, CA

Recent advances in GaN device technology enable high-performance W-band systems by offering significant improvements in the transmitter and receiver components. A family of 92–96-GHz GaN power amplifiers (PA) with increasing gate peripheries (150–1200 mm) will be presented.

6.5: A 0.7–1.6-GHz Two-Stage High-Power-Amplifier MMIC in a Commercial GaN-on-SiC Process **(4:50)**

C. J. Galbrath, L. M. Johnson
MIT Lincoln Laboratory, Lexington, MA

Session 7

ADVANCED SILICON TECHNOLOGIES I

Wednesday, 21 March / 8:30 – 10:00 am / Bronze Room 1

Chair: **P. M. Amirtharaj**
Army Research Laboratory, Adelphi, MD

Co Chair: **T. K. Quach**
AFRL, Wright-Patterson AFB, Dayton, OH

7.1: **A 90-nm SiGe BiCMOS Technology for mm-wave Applications** **(8:30)**

J. Pekarik, J. Adkisson, R. Camillo-Castillo, P. Cheng, J. Ellis-Monaghan, P. Gray, D. Harame
IBM Corp., Essex Junction, VT

M. Khater
IBM Research, Yorktown Heights, NY

Q. Liu, A. Vallett, B. Zetterlund
IBM Corp., Essex Junction, VT

A manufacturable 90-nm BiCMOS technology is being developed to support mm-wave and high-performance analog applications with high-performance SiGe npn transistors integrated onto a full-featured RFCMOS. The technology features an $f_T = 300$ GHz and an $f_{MAX} = 350$ GHz SiGe HBT transistors, 90nm Low Power RF CMOS, and a full suite of passive devices. A design kit will support custom and analog designs and a library of digital functions will aid logic and memory design.

7.2: **Integrating a 65-nm Low-Power CMOS Technology with Spin-Torque-Transfer Magnetic Memory Elements** **(8:50)**

D. Coolbaugh, M. Liehr
College of Nanoscale Science and Engineering at the University at Albany, Albany, NY

R. Ranjan, E. Abedifard
Avalanche Technology, Fremont, CA

This paper shows THE results of the integration of a 65-nm low-power CMOS technology with spin-torque-transfer magnetic memory. This effort has focused upon a set of compatible, stable, and high-yielding fabrication modules. Magnetic tunnel junction (MTJ) devices from a 64-MB array have been demonstrated and the device radiation hardness will be discussed.

7.3: CMOS Compatible SOI MESFETs at the 45-nm Node **(9:10)**

W. Lepkowski, S. Wilk, T. J. Thornton
SJT Micropower, Inc., Fountain Hills, AZ
and
Arizona State University, Tempe, AZ

M. R. Ghajar, Y. Zhang
Arizona State University, Tempe, AZ

Enhanced-voltage silicon-metal-semiconductor field-effect transistors (MESFETs) have been fabricated by using 45-nm SOI CMOS technology with no process changes. The devices have been demonstrated on several runs with low statistical variation. RF characterization demonstrates that the devices will be suitable for microwave applications such as X-band.

7.4: On-Shore 45-nm Bulk CMOS with Reduced Mask Costs **(9:30)**

R. L. Chaney, D. R. Hackler, D. G. Wilson
American Semiconductor, Inc., Boise, ID

DoME CMOS is an advanced 45-nm process that implements Mask-Lite™ technology based on an 1D/grated layout to reduce mask costs up to 90%. DoME CMOS is implemented in an on-shore foundry that is optimized for low-volume requirements typically found in military and aerospace applications. American Semiconductor's design and foundry operations are ITAR compliant and TRUSTED capable.

BREAK **(10:00)**

Session 8

MODULAR RF TECHNOLOGIES

Tuesday, 21 March / 8:30 – 10:00 am / Bronze Room 2

Chair: **C. D. Lesniak**
AFRL, Wright Patterson AFB, Dayton, OH

Co Chair: **B. Paul**
AFRL, Wright-Patterson AFB, Dayton, OH

8.1: Electronic Chassis (EC) Toolkit (8:30)

B. B. Garber, D. N. DeThomas
MacAulay Brown, Inc., Dayton, OH

MOSA is being researched by the DoD as a means to shorten development and upgrade schedules, reduce development costs, and address network interoperability requirements. The objective of the Electronic Chassis Toolkit program is to develop an Open System Architecture (OSA) testbed that is modular and scalable to handle a multitude of radar sensor applications. This testbed will provide a means to objectively quantify the "openness" of an open system.

8.2: Modular Open Systems Methodologies for RF System Design (8:50)

G. Twaites, N. Hastad, S. Reese
General Dynamics Advanced Information Systems, Bloomington, MN and Waimea, HI

E. Culpepper
Air Force Research Laboratory, Wright-Patterson Base, Dayton, OH

Radio-frequency (RF) systems have traditionally been designed as monolithic systems with tightly coupled RF front ends and processing back ends. The MOSA Back End (MBE) for RF systems is an Air Force Research Laboratory program that defines a reference architecture for a modular processing engine. MBE leverages industry standards to deliver a loosely coupled, highly cohesive, modular architecture.

8.3: Mission Objective Driven MOSA for Modular Backend Electronics (9:10)

A. Jacomb-Hood, B. Martin
Lockheed Martin Space Systems Co., Newtown, PA

M. Enoch
Lockheed Martin Space Systems Co., Albuquerque, NM

J. Varnell-Sarjeant
Lockheed Martin Space Systems Co., Littleton, CO

This paper describes a Mission Objective Driven MOSA Configure to Order design approach using an extensible abstract architecture. This overcomes the limitations associated with using conventional pre-defined MOSA architectures. This allows a wider range of missions to reap the cost and schedule benefits of Configure to Order MOSA implementations.

8.4: Cooking IA into the System for Modular Back-End Electronics Reference System **(9:30)**

J. F. Varnell-Sarjeant
Lockheed Martin Space Systems Co., Littleton, CO

A. Jacomb-Hood, B. G. Martin
Lockheed Martin Space Systems Co., Newtown, PA

R. P. Bellini
Lockheed Martin Space Systems Co., Philadelphia, PA

S. J. Dill
Lockheed Martin Space Systems Co., Frederick, MD

A reference architecture for payload back ends is being developed by using the MOSA Back End (MBE) program. In this paper, the challenge of IA certification when, during the architecture phase, the exact mission is not known will be discussed. An Information Assurance (IA) process to build security into the architecture using DoDAF view products for complete, secure architectures will be presented.

BREAK **(10:00)**

Session 9

SPACE PROCESSOR

Wednesday, 21 March / 8:30 – 10:00 am / Bronze Room 3

Chair: **M. N. Lovellette**
Naval Research Laboratory, Washington, DC

Co Chair: **L. Cohn**
Naval Research Laboratory, Washington, DC

9.1: On-Board Mission Processing Architecture (8:30)

G. R. Brown, E. Grobelny, D. Campagna
Honeywell International, Inc., Clearwater, FL

On-board satellite mission processing solutions must survive 15 years in the on-orbit space environment and offer attractive size, weight, and power. The processing architecture must support scalability and flexibility so it can change with mission needs over the life of the constellation. It is beneficial for the selected architecture to be based on widely supported commercial standards with an ecosystem that can lower the cost of ownership. A mission processing architecture that meets these goals will be discussed.

9.2: Space Computing Subsystems Based on Multicore Processing Components (8:50)

R. Berger, M. Bear, J. Marshall, D. Moser, D. Stanley
BAE Systems, Inc., Manassas, VA

C. A. Dennis
NOVA Solutions, Inc., Warrenton, VA

Reliable high-performance spaceborne payload processing requires the throughput of rad-hard multicore processing components. At this performance, minimizing power dissipation across a broad spectrum of applications requires heterogeneous processing solutions. Key processing components and the supporting memory and I/O interfaces needed to optimize the capabilities of these subsystems will be described.

9.3: Discrete-Fourier-Transform (DFT) Codes and How to Correct Them (9:10)

R. Redinbo
University of California at Davis, Davis, CA

Real number block codes derived from the discrete Fourier transform (DFT) are corrected by coupling a very modified Berlekamp-Massey algorithm with a syndrome extension process. Simulation results provide probability of error and mean-squared error performances for some DFT codes.

9.4: High-Performance High-Volume Onboard Processor Architecture **(9:30)**

P. Murray, T. Randolph, D. Van Buren, D. Anderson
SEAKR Engineering, Inc., Centennial, CO

I. Troxel
Betrokor, Inc., Cheyenne, WY

In support of next-generation satellite communication and onboard processing, SEAKR Engineering is developing a flexible processing architecture that accommodates dynamic processing loading and radiation-induced hardware upsets. The design of the flexible modem and its capability to dynamically reconfigure will be featured along with considerations for supporting high volume manufacturing programs.

BREAK **(10:00)**

Session 10

ADVANCED SILICON TECHNOLOGIES II

Wednesday, 21 March / 10:30 am – 12:00 pm / Bronze Room 1

Chair: **G. L. Creech**
AFRL, Wright-Patterson AFB, Dayton, OH

Co Chair: **G. Birdwell**
Army Research Laboratory, Adelphi, MD

10.1: A 44–46-GHz 16-Element SiGe BiCMOS High-Linearity Transmit/Receive Phased Array (10:30)

C. Y. Kim, D. W. Kang, G. M. Rebeiz
University of California at San Diego, La Jolla, CA

This paper presents a 16-element Q-band transmit/receive phased array with high receive linearity and low power consumption. The design is based on the All-RF architecture with passive phase shifters and a 1:16 Wilkinson network. In the receive mode, an input P1dB of -10 dBm and a noise figure of 10.5 dB is achieved at 45 GHz with a power consumption of 0.95 W. In the transmit mode, each channel has an output P1dB of 3 dBm and Psat of 6 dBm at 45 GHz, with a power consumption of 1.16 W. The design results in a low rms gain error due to a high-resolution VGA in each channel. Measurements on multiple channels show near-identical gain and phase response in both the transmit and receive mode due to the use of a symmetrical passive combiner. To our knowledge, this is the highest linearity millimeter-wave receive silicon phased array to date.

10.2: Phased-array Radar and Multistatic Array Imaging with 16-Element 60-GHz SiGe Tx and Rx ICs (10:50)

A. Natarajan, M. Piz, A. Valdes-Garcia, S. Reynolds
IBM T. J. Watson Research Center, Yorktown Heights, NY

This paper presents active imaging measurements performed using a fully integrated phased-array 60-GHz SiGe Tx and Rx. Measurements demonstrate a range resolution of 15 cm, while multistatic array measurements show a lateral resolution of 40 mm. Wireless data rates of up to 5.3 Gb/sec for a Tx-Rx separation of 9 m have previously been demonstrated using the array. These measurements are a proof of concept for integrated multi-function mm-wave phased-array front ends capable of both multi-gigabit per second wireless links and high-resolution imaging.

10.3: A 2–18-GHz SiGe BiCMOS Solid-State-Mode Former Building Block for Low-Cost Light-Weight, Beamformers **(11:10)**

D. Saunders
ViaSat Advanced Microwave Products, Gilbert, AZ

N. Jain, G. Menon
Anokiwave, San Diego, CA

M. Barber, K. Hamblin, N. Vanderpool
BerrieHill Research Co., Dayton, OH

C. Harper, T. Dalrymple, K. Aihara
AFRL, Wright-Patterson AFB, Dayton, OH

The design and measured results of a highly integrated 2–18-GHz active hybrid will be presented. The active hybrid provides 6 dB of gain adjustment range in 0.5-dB steps, 360° of phase-adjustment range in 5.625° steps, a 10-dB noise figure, 50 dB of spurious-free dynamic range, and less than 2.8° rms phase error. It is designed to operate from –40 to +85°C at 1.8 V, 2.1 W. Fabricated using IBM's 0.13-μm SiGe BiCMOS process and packaged in a 32-pin 5 × 5 mm QFN, this chip makes low-cost small mode formers possible.

10.4: X-Band CMOS Phased Arrays: Transmit and Receive Chips with Chip-on-Board Packaging **(11:30)**

D. Shin, C. Y. Kim, D. W. Kang, G. M. Rebeiz
University of California, San Diego, La Jolla, CA

This paper presents the design and chip-on-board packaging of four-element phased-array receiver and transmitter chips for 8–11-GHz applications. The phased-arrays are built using 0.13-μm CMOS with a single-ended design for the Rx chip and differential design for the Tx chip. The Rx chip results in a measured gain of 10.1 dB, an input P_{1dB} of –12.5 dBm, an input IP3 of –4 dBm, and a NF of 3.4 dB at 9.5 GHz. The transmit chip results in a gain of 15 dB and an output power of +13 dBm per channel at 8–9 GHz. The phased arrays are packaged using chip-on-board techniques and bond-wires. Measurements and simulations show that, with well-isolated input bond wires, < –30 dB coupling between the channels, and an rms amplitude and phase error of < 0.2 dB and < 1°, respectively, at 9.5 GHz, when the phase of neighboring channels are changed, can be obtained. To our knowledge, this is the first in-depth study of coupling in a phased-array chip with chip-on-board packaging.

LUNCH **(12:00)**

Session 11

SUB-100-nm RAD-HARD TECHNOLOGIES

Wednesday, 21 March / 10:30 am – 12:00 pm / Bronze Room 2

Chair: **B. Wilson**
DTRA, Ft. Belvoir, VA

Co Chair: **R. C. Lacoe**
The Aerospace Corp., Los Angeles, CA

11.1: Trends in the SEE and TID Radiation Response of 65-, 45- and 32-nm SOI CMOS Transistors, Memories, and Latches **(10:30)**

K. P. Rodbell
IBM T. J. Watson Research Center, Yorktown Heights, NY

Trends in SEE and TID radiation response of recent generation CMOS SOI devices will be reviewed. SEE data and modeling on 65-, 45-, and 32-nm SRAMs and latches will be presented. The implications of novel materials (*i.e.,* HKMG) and new device structures (*i.e.,* multi-fingered devices) on future CMOS scaling will also be discussed.

11.2: High-Performance 64-MB SRAM Fabricated in a Rad-Hard 90-nm Technology **(10:50)**

S. Doyle, J. Ross, N. Haddad, C. Hill, A. Kelly, J. Rodgers, E. Chan
BAE Systems, Manassas, VA

Technology and development status will be presented on new deep submicron rad-hard 64MB SRAM family. Electrical characterization, radiation test results, and preparation for qualification will be discussed.

11.3: Rad-Hard QML ASIC Design Flow for 90-nm Bulk CMOS Using a Commercial Foundry **(11:10)**

C. Hagan, P. Milliken, R. Van Art, D. Wilkin
Aeroflex Colorado Springs, Inc., Colorado Springs, CO

A. Amort
The Boeing Co., Seattle, WA

This paper reports on efforts to develop a QML ASIC design flow using a RHBD library on IBM's Commercial 90-nm CMOS9SF process. Issues addressed include core cell place and route flow development, demonstration of correlation between models and silicon, design for test techniques, and development of a customer design toolkit.

11.4: Radiation Effects in Sub-100-nm Strained-Silicon CMOS and SiGe BiCMOS RF Technology Platforms **(11:30)**

S. Phillips, R. Arora, K. Moen, N. Lourenco, J. D. Cressler
Georgia Institute of Technology, Atlanta, GA

The effects of radiation on highly scaled RF-CMOS and SiGe BiCMOS processes will be discussed in the context of total ionizing dose and single-event effects. The impact of scaling, process modifications, and device layout on radiation-induced degradation will be addressed and supported with experimental data obtained from IBM's 65- and 45-nm RF-CMOS platforms and IBM's fourth-generation 9HP (90-nm CMOS node) SiGe BiCMOS process.

LUNCH **(12:00)**

Session 12

SPACE BUS

Wednesday, 21 March / 10:30 am – 12:00 pm / Bronze Room 3

Chair: **J. P. Egan**
National Reconnaissance Office, Chantilly, VA

Co Chair: **L. Cohn**
Naval Research Laboratory, Washington, DC

12.1: The Next-Generation Space Interconnect Standard (NGSIS) (10:30)

C. P. Collier
AFRL, Kirtland AFB, NM

Requirements for future spacecraft subsystem interconnect are growing by orders of magnitude. In the past 5 years, the industry has gone from 1553 at 1 Mbits/sec to SpaceWire at 250 Mbits/sec to TTGE at 1 Gbit/sec. Over the next 5 years, requirements are expected to grow beyond 10 Gbits/sec to support high-data-rate instruments and onboard sensor data processing. New systems paradigms will require extending interconnect capabilities and reliability levels well beyond those available in current technologies. The NGSIS sole focus is to bring together government and industry to work towards a common methodology that standardizes the design and development of satellite interconnects and networks

12.2: Space-Data-Bus Technologies Evolve to Network Fabrics (10:50)

J. R. Marshall, R. W. Berger, M. J. Bear
BAE Systems, Manassas, VA

The PCI Bus, the space-industry interconnect workhorse, is limited in bandwidth, flexibility, and scalability. The move to network topologies starting with SpaceWire implementations and evolving into SerDes-based fabrics such as serial RapidIO, 10-GB Ethernet, and PCI Express will be described. Standardization efforts under way to reach a manageable solution will also be summarized.

12.3: High-Speed Interconnect for Space Applications (11:10)

G. R. Brown, E. Grobelny, D. Campagna
Honeywell International, Inc., Clearwater, FL

Modern high-performance computers require high-speed interconnect to move data around to supply the processing engines with data to process. It is beneficial for the selected interconnect to have a widely supported ecosystem and for it to support scalability and flexibility. Finally, the implementation must survive 15 years in the on-orbit space environment and offer attractive size, weight, and power. How the RapidIO protocol and our Space Network implementation meet these goals will be discussed.

12.4: High-Data-Rate and Capacity Advanced Data Storage Unit **(11:30)**

J. Carroll, B. Koritnik
SEAKR Engineering, Inc., Centennial, CO

I. Troxel, D. Beckman
Betrokor, Inc., Cheyenne, WY

High-performance sensors are exceeding the limits of spacecraft downlink capacities and the growth curves in these technologies show the disparity is worsening. To address this need, a new solid-state recorder architecture is under development to meet the throughput, capacity, and fault-tolerance requirements for future advanced sensors.

LUNCH **(12:00)**

Session 13

ELINT RECEIVERS

Wednesday, 21 March / 1:30 – 3:00 pm / Bronze Room 1

Chair: **T. W. Dalrymple**
AFRL, Wright-Patterson AFB, Dayton, OH

Co Chair: **S. Hary**
AFRL, Wright-Patterson AFB, Dayton, OH

13.1: Small-Form-Factor Digital RWR (DRWR) Development Incorporating System-on-Chip (SoC) Technology (1:30)

F. Stroili, D. C. Packard, V. L. Miller
BAE Systems, Merrimack, NH

R. Perry, S. Hary
AFRL., Wright-Patterson AFB, Dayton, OH

The application of SiGe-based System-on-Chip (SoC) technology to achieve a highly miniaturized Wideband RF (WBRF) downconverter set combined with 3U (Vita-46/48) implementation of Digital Channelized Receiver (DCR) technology has produced a small-form Digital RWR (DRWR) System with advanced performance levels which has been demonstrated.

13.2: Advanced Wideband Digital ELINT Processor (1:50)

C. Estrella
AFRL, Rome, NY

The Advanced Wideband Digital ELINT Processor (AWDEP) is a single-channel system utilizing recent developments in commercially developed high-speed analog-to-digital sampling and processing technologies. The AWDEP system directly digitizes a 2-GHz IF BW signal and performs digital DSP processing using onboard field-programmable gate array (FPGA) devices to produce precise, repeatable pulse descriptor words (PDWs). Monitoring of the conventional 0.5–18-GHz ELINT spectrum was attained by using a custom-built DRS 9159 tuner. This paper discusses, in detail, the key elements of the AWDEP system and provides results from characterization and performance testing.

13.3: Nyquist Folding Receiver for Analog-to-Information (2:10)

G. L. Fudge, B. C. Rutherford
L-3 Communications, Greenville, TX

A. Agoston
Hyperlabs, Inc., Beaverton, OR

The Nyquist Folding Receiver is a wideband architecture based on compressive sensing ideas that uses sub-Nyquist-rate RF pulse sampling to fold the RF input into a narrow bandwidth for conventional ADC digitization. By modulating the pulse sample times, a corresponding fold-dependent modulation was induced on received signals to allow recovery of the original RF from the aliased data.

13.4: A Super-Wideband Compressive Receiver for ELINT Applications **(2:30)**

A. V. Messier, R. A. Stiffler, N. Kinayman, D. B. Du Russel, D. H. Vooys, G. D. Holland, R. L. Slattery, P. G. Murphy, D. J. Baker, P. A. Baldo, K. E. Parrillo, L. C. Mailhiot, T. M. Hancock, M. A. Gouker
Massachusetts Institute of Technology, Lexington, MA

The super-wideband compressive receiver is an digitally augmented realization of the analog chirp transform spectral analysis technique. It results in an unprecedented combination of analysis bandwidth, low latency, high probability of intercept, and the ability to work in dense spectral environments.

BREAK **(3:00)**

Session 14

RAD-HARD DESIGN METHODS

Wednesday, 21 March / 1:30 – 3:00 pm / Bronze Room 2

Chair: **L. W. Massengill**
Vanderbilt University, Nashville, TN

Co Chair: **L. J. Palkuti**
DTRA, Ft. Belvoir, VA

14.1: A Systems-Based RHBD Approach for High-Speed Communications Devices **(1:30)**

S. E. Armstrong
NSWC Crane, Crane, IN
and
Vanderbilt University, Nashville, TN

R. Blaine, W. T. Holman, L. Massengill
Vanderbilt University, Nashville, TN

Typical high-speed communications systems can be assessed with respect to functional blocks, global signals, signal domains, and design aspects. Each point-of-view provides valuable information for radiation hardening. A systems-level approach was used to facilitate the analog rad-hard–by–design process for SE vulnerable interfaces.

14.2: Globally Optimized and Certified Soft Error Resilience **(1:50)**

S. Mitra
Stanford University, Stanford, CA

R. Iyer, Z. Kalbarczyk
University of Illinois, Urbana-Champaign, IL

K. Lilja
Robustchip, Pleasanton, CA

Techniques for designing globally optimized robust digital systems with certified protection from single-event single-upsets and single-event multiple upsets will be presented. This is possible through an inter-disciplinary approach combining device physics, circuit design, system-level design, coding theory, and formal methods.

14.3: Analysis of Single-Event Transients in a 45-nm SOI Technology for Rad-Hard Applications **(2:10)**

D. Loveless, J. Kauppila, T. Haeffner, T. Holman, M. Alles, B. Bhuva, L. Massengill, S. Jagannathan, N. Gaspard, N. Atkinson, R. Blaine, J. Ahlbin
Vanderbilt University, Nashville, TN

Recent data on single-event-transient (SET) pulse widths in a 45-nm silicon-on-insulator (SOI) technology will presented. Results for ion strikes up to an LET of 49 MeV-cm^2/mg at normal incidence indicate that the transient pulse widths in inverters are limited to 200 psec. Also, a novel method for experimentally extracting the measurement offset and skew introduced by the on-chip measurement circuit will be provided.

14.4: Honeywell's HX5SA Structured Array **(2:30)**

J. B. Hobbs, D. K. Nelson, J. P. Graebel
Honeywell Defense & Space, Plymouth, MN

The HX5SA structured array capability extends Honeywell's QML-qualified 150-nm rad-hard application-specific integrated-circuit (ASIC) capability to offer the cost and schedule advantages of a gate array while retaining many of the features of the HX5000 standard cell library. The product development approach, product features, and qualification test results will be presented.

BREAK **(3:00)**

Session 15

3D INTEGRATION AND ADVANCED PACKAGING FOR ICs

Wednesday, 21 March / 1:30 – 3:00 pm / Bronze Room 3

Chair: **M. Fritze**
DARPA/MTO, Arlington, VA

Co Chair: **V. Sharma**
IDA, Alexandria, VA

15.1: High-Density 3D Integration for Micro-Systems **(1:30)**

D. Yost, B. Aull, C.-L. Chen, C. Chen, S. Hsu, C. Keast, J. Knecht, V. Suntharalingam, B. Tyrrell, K. Warner, B. Wheeler
MIT Lincoln Laboratory, Lexington, MA

Micro-system density is the driver for 3D. Package-level 3D is now in production. Device-level 3D with high-density interconnects offers even greater benefits for signal interaction between components. Approaches to high-density 3D integration will be summarized and applications enabled and demonstrated by MIT Lincoln Laboratory's 3D technology will be discussed while sharing lessons learned regarding homogeneous and heterogeneous integration.

15.2: 3D IC Technology Overview **(1:50)**

J. Knickerbocker|
IBM, Yorktown Heights, NY

15.3: An Advanced Temporary Bonding Process Critical for Achieving 3-D Integration **(2:10)**

J. McCutcheon, R. Puligadda
Brewer Science, Inc., Rolla, MO

This paper focuses on the Brewer Science® ZoneBOND™ process that has been developed to allow temporary bonding of a device wafer to a carrier substrate, survival through processing, and separation at room temperature. The separation process consists of softening the material at the outer edge, securing the device wafer onto vacuum support, and separating the carrier from the adhesive.

15.4: Test Circuits for 3-D Systems Integration **(2:30)**

I. Savidis, E. G. Friedman
University of Rochester, Rochester, NY

Three test circuits have been developed to experimentally demonstrate and stress the state of the art in 3-D integrated systems. Several critical elements of this emerging technology, synchronization, power delivery, and thermal management, are just beginning to be explored. The three test circuits explore these three fundamental design issues. These test circuits will be discussed, and trends and challenges outlined.

BREAK **(3:00)**

Session 16

NEXT PROGRAM

Wednesday, 21 March / 3:30 – 5:00 pm / Bronze Room 1

Chair: **J. Albrecht**
DARPA/MTO, Arlington, VA

Co Chair: **P. A. Maki**
Office of Naval Research, Arlington, VA

16.1: State-of-the-Art E/D GaN Technology Based on an InAlN/AlN/GaN Hetereostructure (3:30)

A. Ketterson, M. Schuette, T-M. Chou, H-Q. Tserng, P. Saunier
TriQuint Semiconductor, Richardson, TX

S. Guo and X. Gao
IQE-RF LLC, Somerset, NJ

G. Xing
University of Notre Dame, Notre Dame, IN

State-of-the-art integrated E- and D-mode devices based on InAlN/AlN/GaN heterostructure will be reported. A F_t of 261 and 278 GHz were achieved for (integrated) E- and D-mode devices. The corresponding F_{max} are 302- and 232 GHz. The E-mode devices are selectively RIE recessed down to the AlN layer. 501-stage ring oscillators have also been demonstrated with 11% yield (100-nm gates).

16.2: Deeply-Scaled Self-Aligned-Gate GaN DH-HEMTs with Ultrahigh Cutoff Frequency (3:50)

M. Micovic, K. Shinohara, D. Regan, A. Corrion, D. Brown, S. Burnham, A. Margomenos, A. Kurdoghlian
HRL Laboratories, Malibu, CA

Record DC and RF performance in deeply scaled self-aligned gate (SAG) GaN-HEMTs operating in both depletion-mode (D-mode) and enhancement-mode (E-mode) will be reported. Through aggressive lateral scaling of the gate length (L_g) and the source-drain distance (L_{sd}) using a novel self-aligned gate technology and engineering of a thin top barrier layer, 20-nm gate AlN/GaN/AlGaN double-heterojunction (DH) HEMTs operating in D-mode (and E-mode) exhibited record DC and RF characteristics with high yield and uniformity.

16.3: N-Face GaN HEMT Technology for Next-Generation Mixed-Signal Electronics (4:10)

I. Smorchkova, R. Grundbacher, V. Gambin, X. Gu, G. Lewis, F. Oshita, C. Namba, P. Liu, S. Poust, P. Nam, M. Wojtowicz
Northrop Grumman, Redondo Beach, CA

The progress made on DARPA's NEXT Program will be discussed. On this program, Northrop Grumman and its team members are developing highly scaled E/D-mode N-polar GaN transistors for advanced mixed-signal applications. To date, N-face GaN HEMTs with an f_t = 270 GHz, f_{max} = 370 GHz, and off-state breakdown voltage > 20 V have been demonstrated.

16.4: Recent Progress In N-Polar GaN Technology (4:30)

U. K. Mishra
University of California at Santa Barbara, Santa Barbara, CA

The progress made on DARPA's NEXT Program will be discussed. On this program, Northrop Grumman and its team members are developing highly scaled E/D-mode N-polar GaN transistors for advanced mixed-signal applications. To date, N-face GaN HEMTs with an f_t of 270 GHz, f_{max} of 370 GHz, and off-state breakdown voltage > 20 V have been demonstrated.

Session 17

RADIATION EFFECTS IN NOVEL MATERIALS

Wednesday, 21 March / 3:30 – 5:00 pm / Bronze Room 2

Chair: **L. J. Palkuti**
DTRA, Ft. Belvoir, VA

Co Chair: **L. W. Massengill**
Vanderbilt University, Nashville, TN

17.1: Radiation Effect on the Magnetism and the Spin-Dependent Transport in Ferromagnetic $L1_0$ MnAl **(3:30)**

J. Lu
University of Virginia, Charlottesville, VA

B. D. Weaver
Naval Research Laboratory, Washington, DC

N. Anuniwat, M. Marc, Y. Cui
University of Virginia, Charlottesville, VA

E. Chen
Grandis, Inc., Milpitas, CA

This paper studied the radiation effect on the magnetic and transport properties in nanostructures and magnetic materials potentially important for the future of spintronics and nanomagnetics. The goal is to understand the adverse impacts of the radiation on the magneto-transport, particularly the spin torque transfer phenomenon in magnetic nanostructures and the magnetism of novel ferromagnetic materials, respectively. Such an understanding will have a broad impact on the potential application of nanomagnetics and spintronics to aerospace and military systems in the future.

17.2: III-V Nanowire Devices for Radiation Effect Studies **(3:50)**

S. C. Lee, A. Chaudhuri, N. Youngblood, S. R. J. Brueck
University of New Mexico, Albuquerque, NM

A. Sharma, D. Telesca, C. Mayberry
AFRL/RVSE, Kirtland AFB, Albuquerque, NM

A novel process for the growth of in-plane circuit-integrated, III-V nanowires will be presented. The process takes advantage of nanolithography and selective area growth. Importantly, these nano-wires can be grown integrated with single-crystal contacts in complex geometries, and the structure can incorporate a dielectric layer for isolation from the substrate.

17.3: Radiation Tolerance and Recovery Characteristics of ZnO Thin-Film Transistors (4:10)

B. Bayraktaroglu, K. Leedy
AFRL, Wright-Patterson AFB, Dayton, OH

Y. V. Li, D. A. Zhao, J. I. Ramirez, H. H. R. Fok, T. N. Jackson
Penn State University, University Park, PA

It is expected that devices made from the wide-bandgap ionic semiconductor ZnO will be resistant to radiation-induced disorder because of the insensitivity of electron transport in this material to bond angle and bond length. Preliminary results for nanocrystalline ZnO thin-film transistors (TFTs) irradiated with ^{60}Co gamma rays will be reported. Initial experiments show that for gamma-ray exposure doses up to 1 MGy, the device changes are primarily a negative turn-on and a threshold-voltage shift, with less than a 10% change in field-effect mobility. Both the threshold-voltage and turn-on shifts are nearly completely removed by annealing at 200°C for 1 minute, and some recovery is seen even at room temperature.

17.4: MBE for Advanced GaN-Based Electron Devices (4:30)

S. Kaun, M. H. Wong, U. Mishra, J. Speck
University of California, Santa Barbara, CA

This presentation will provide an overview of progress in the MBE growth of group III nitrides for electron devices, including new work on high-temperature plasma-assisted MBE (PAMBE) growth and devices, the role of threading dislocations in GaN-based HEMT performance, and recent work on vertical structures using ammonia-based MBE.

Session 18

ADVANCED RESEARCH INTO SCRM

Wednesday, 21 March / 3:30 – 4:30 pm / Bronze Room 3

Chair: **C. E. McCants**
DARPA, Arlington, VA

18.1: Do You Know What You are Buying? A Study in Microelectronic System Development Using Untrusted Advanced Electronic Parts, and the Impact on the Supply Chain **(3:30)**

S. Fazzari, G. Jones, A. Brown
Booz Allen Hamilton, Arlington, VA

Within the DoD, there is a desire to leverage existing commercial technologies to provide advanced features for next-generation microelectronic systems design. The use of commercial components for military applications has many benefits including reduced cost of system design and reduction of development cycle. However, by relinquishing control of the design of electronics components to an untrusted third party, questions arise related to the integrity of the specific inserted parts. This paper will discuss methods to quantify the technical challenges and provide novel approaches to manage the risk.

18.2: A Method for Trusting Integrated Circuits: A Non-Simulation-Based Approach **(3:50)**

M. Noell, M. Redekopp
Raytheon, El Segundo, CA

This presentation describes a non-simulation-based approach developed as part of the DARPA TRUST in Integrated Circuits program to detect hardware Trojans in third-party intellectual property.

18.3: The Integrity of FPGA Designs: Capabilities Enabled by Unlocking Bitstreams and Third-Party IP **(4:10)**

J. Graf, S. Harper, L. Lerner
Luna Innovations, Inc., Roanoke, VA

A novel, broad definition of field-Programmable gate-array design integrity will be introduced. An FPGA design with integrity must continuously provide the FPGA user with the function described by the designer and no other function. Using this definition, its value to the domains of FPGA Trust, high-reliability FPGA design and FPGA design anti-obsolescence will be explored. Further, solutions in each of those domains that have a common starting point will be described: Luna's unique software that evaluates the previously inaccessible designs inside of FPGA bitstreams and Third-Party Intellectual Property.

Session 19

THERMAL MANAGEMENT I

Thursday, 22 March / 8:30 – 10:00 am / Bronze Room 1

Chair: **A. Bar-Cohen**
DARPA, Arlington, VA

Co Chair: **K. Bloschock**
System Planning Corp., Arlington, VA

19.1: Thermal Characterization of Composite GaN Substrates for HEMT Applications **(8:30)**

J. Cho, Z. Li, E. Bozorg-Grayeli, T. Kodama, M. Asheghi, K. E. Goodson
Stanford University, Stanford, CA

D. Francis, F. Ejeckam, F. Faili
Group4 Labs, Inc., Fremont, CA

D. H. Altman
Raytheon Co., Waltham, MA

Thermal resistances in composite substrates for GaN HEMTs limits the peak power density. This paper reports thermal properties in composite substrates containing SiC and diamond using two separate photothermal techniques and electrical heating and thermometry in nanopatterned bridges. The data are used to project the potential impact of novel substrate technologies on HEMT power scaling.

19.2: Thermal Management of High-Power-Density Electronics **(8:50)**

Y. Zhao, Q. Cai, Y.-C. Chen, B.-C. Chen
Teledyne Scientific & Imaging Co., Thousand Oaks, CA

C.-L. Chen
University of Missouri, Columbia, MO

A low-profile CTE-matched high-performance vapor-chamber heat spreader and a novel carbon-based nanothermal interfaces (NTIs) will be introduced. The vapor chambers, made of silicon, have a thermal expansion coefficient matching nicely with most semiconductor materials. Unlike conventional thermal interface materials (TIMs) infiltrated with randomly oriented high-conductivity fillers, the carbon-based NTIs relies on vertically aligned graphite nanoplatelets to provide both extraordinarily high thermal conductivity along the heat transport direction and controllable stiffness to conform to surfaces with different roughness and hardness, greatly improving the overall heat transfer performance. Experiments and numerical simulations were conducted and results indicated that the vapor-chamber heat spreaders and NTIs offer superior thermal performance to conventional thermal management technologies, which will have great impact on the development of the next-generation high-power electronics, *i.e.,* high-power laser diodes and high-power RF devices.

19.3: Near-Junction Thermal Management in High-Power GaN HEMTs **(9:10)**

D. C. Dumka, U. Chowdhury, J. L. Jimenez, T.-M. Chou, A. Ketterson, D. M. Fanning, B. Murdock
TriQuint Semiconductor, Inc., Richardson, TX

D. Francis, F. Faili, F. Ejeckam
Group4 Labs, Inc., Fremont, CA

A process for near-junction thermal management in high-power GaN HEMTs will be presented. It involves lift-off of epitaxial AlGaN/GaN film grown on Si substrate and bonding that to polycrystalline CVD diamond substrate developed for very-high thermal conductivity of 1300 W/mK. A three-fold enhancement in the power handling by such GaN/Diamond wafers, compared to standard GaN/SiC wafers, is predicted.

19.4: Solder-Bonded Carbon-Nanotube TIMs for Compliant High-Performance Die Attach **(9:30)**

D. Altman, A. Gupta, S. G. Lee
Raytheon, Sudbury, MA

S. Hodson, T. Fisher
Purdue University, West Lafayette, IN

A. Bulusu, S. Graham, B. Cola
Georgia Institute of Technology, Atlanta, GA

This paper reviews the development of carbon-nanotube-based thermal interface materials as an alternative to high-performance die-attach epoxies. These interfaces are expected to provide the thermal performance of a solder joint while retaining the compliance of a filled epoxy. Data indicates thermal resistances of < 0.04 cm^2 C/W are achievable with this approach.

BREAK **(10:00)**

Session 20

TRUSTED ELECTRONICS I

Thursday, 22 March / 8:30 – 10:00 am / Bronze Room 2

Chair: **D. Pentrack**
DMEA, McClellan AFB, CA

Co Chair: **J. A. Meinhardt**
Honeywell FM&T, Kansas City, MO

20.1: The Practical Implications of Trust **(8:30)**

N. Levine, A. Gahoonia, J. Opray
DMEA, McClellan, CA

The Trusted Foundry Program was established to protect integrated circuits that are being inserted into sensitive military systems, from threats to their integrity, confidentiality and availability. Three approaches for ensuring trust are evaluated and compared. Additionally, an example of a Trojan will be discussed.

20.2: Use of Circuit Camouflage Techniques to Protect ICs from Reverse Engineering and Tampering **(8:50)**

R. C. Cocchi, J. P. Baukus, L. W. Chow, B. J. Wang
SypherMedia International, Inc., Westminster, CA

Technology has been developed that inhibits hardware IP from reverse-engineering attack and Trojan insertion using advanced circuit camouflage techniques. Cell libraries using techniques specifically designed to hide cell functionality from reverse engineers have been successfully employed in commercial and government segments.

20.3: Trusted Maskmaking for Defense Electronics **(9:10)**

J. Murduck, M. Fitzpatrick, J. Miller, B. Miskimon, J. Monk, M. Schneider, P. Warner, M. Sherwin
Northrop Grumman Corp., Linthicum, MD

Mission-critical microcircuits for DoD systems have been produced at Northrop Grumman Corporation (NGC) over the past half-century. Recent approval of Trusted Maskmaking status now allows integration of mask fabrication through our already established Trusted Foundry wafer fabrication. Techniques involved in taking design data to glass reticle in a secure fashion as well as NGC's overall Trusted maskmaking capabilities will be described.

20.4: Establishing Trust in Third-Party IP Using Anti-Tamper (AT) Countermeasures to Malicious Circuit Attacks (MCAs) **(9:30)**

E. C. King, M. E. Scheitrum
Atessa, Inc., Pleasanton, CA

Trusted design intellectual property (IP) is the foundation of system security. This paper highlights a method for using anti-tamper (AT) circuitry and other techniques to improve the Trust levels of third-party IP used in field-programmable gate arrays (FPGAs) and other logic-bearing devices.

BREAK **(10:00)**

Session 21

ADVANCED RF/MMW TECHNOLOGIES I

Thursday, 22 March / 8:30 – 10:00 am / Bronze Room 3

Chair: **W. Chappell**
Purdue University, West Lafayette, IN

Co Chair: **J. B. Muldavin**
MIT Lincoln Laboratory, Lexington, MA

21.1: A Chip Scale Switchable Channelizer (8:30)

S. V. Krishnaswamy, C. Milton, W. Miller, J. Hartman, D. Adam
Northrop Grumman Electronic Systems, Baltimore, MD

C. Elsass
Agile RF, Santa Barbara, CA

K. M. Lakin
Consultant, Redmond, OR

Miniature bulk-acoustic-wave (BAW) filters that use electrostrictive barium strontium titanate in place of the more usual piezoelectric AlN films enable chip scale channelizers with an intrinsic switching capability. The chip scale channelizer will replace five discrete BAW filter chips and two GaAs switch chips, resulting in significant size and cost reduction for digital beam forming (DBF) radar application.

21.2: High-Performance Filtering Technologies (8:50)

R. A. Newgard
Rockwell Collins, Cedar Rapids, IA

In cooperation with the Defense Advanced Research Program Agency (DARPA), universities and national labs, Rockwell Collins has developed high-performance filtering technologies. These technologies include high-Q wide-tuning-range pre-selectors based on cavity filters along with high-Q microelectromechanical (MEMS) filters based on AlN micro-resonators having unprecedented measured performance.

21.3: C-Band Aluminum Nitride Resonator and Filter Arrays (9:10)

M. Ziaei-Moayyed, P. Clews, J. Nguyen, R. H. Olsson III
Sandia National Laboratories., Albuquerque, NM

This paper reports C-band resonators and filter arrays realized in aluminum nitride (AlN) lamb wave microresonator technology. Microresonators have been realized at 5.7 GHz with coupling coefficients (k_t^2) and quality factors (Q) of 1.5% and 365, respectfully. Overtoning techniques have been utilized to increase the Q factor at 5.7 GHz to 2025 while maintaining a nearly constant k_t^2Q figure of merit of 4. The demonstrated AlN frequency *Q product (fQ) of 1.15 x 10^{13} approaches that of crystalline quartz or silicon allowing narrow % bandwidth (< 0.1%) filters to be realized with low insertion loss. An array of dual-mode microresonator filters spanning 5.5–6 GHz has also been demonstrated. When properly matched the filters exhibit insertion losses less than 6 dB and percent bandwidths of 0.75–1%.

21.4: Small-Antenna-Array Near-Field Cancelation Using Tunable Resonators for Simultaneous Transmit and Receive **(9:30)**

A. Wegener, T. Dalrymple, W. Chappell
Purdue University, West Lafaytte, IN

A planer 1 × 3 antenna array with tunable resonators placed between the antennas which are used to mitigate the effects of mutual coupling will be presented. These resonators can be tuned to reduce mutual coupling over a narrow band placed at any frequency covered by the patch antennas. The resonators can also be tuned to provide an arbitrary narrow band phase shift between the antenna elements. This is used to demonstrate phase cancelation at the middle element, which would allow it to receive a low-power signal while the outer two elements transmit relatively large signals.

BREAK **(10:00)**

Session 22

THERMAL MANAGEMENT II

Thursday, 22 March / 10:30 am – 12:00 pm / Bronze Room 1

Chair: **A. Bar-Cohen**
DARPA, Arlington, VA

Co Chair: **K. Bloschock**
System Planning Corp., Arlington, VA

22.1: Advancements in Thin-Film Superlattice Thermoelectric Coolers **(10:30)**

C. E. Lents, J. E. Turney, E. Landry, M. Pearson,
United Technologies Research Center, East Hartford, CT

P. Barletta, J. Pierce, G. Bulman, R. Venkatasubramanian
RTI International, Research Triangle Park, NC

This DARPA-sponsored research program seeks to reduce parasitic losses in thin-film superlattice thermoelectric coolers through development of thick (~14 μm) films, low-resistance ohmic contacts, and a geometry optimization toolset for the design of modules with minimally impeded current and heat flow.

22.2: Fabrication and Characterization of a High-Performance Air-Cooled Heat Exchanger with an Integrated Multi-Condenser Heat Pipe **(10:50)**

T. B. Peters, H. A. Kariya, D. F. Hanks, W. Staats
MIT, Cambridge, MA

J. Allison
The Boeing Co., El Segundo, CA

D. Jenicek, M. Cleary, J. H. Lang, J. G. Brisson, E. N. Wang
MIT, Cambridge, MA

M. McCarthy
Drexel University, Philadelphia, PA

An advanced air-cooled heat exchanger for the thermal management of high-performance electronics is being developed. The state of the art of heat sinks were advanced by (1) leveraging a loop heat pipe with multiple condensers to minimize thermal resistance and (2) interdigitating impellers between the fins to enhance heat transfer. The impellers are driven by a custom low-profile high-efficiency permanent-magnet motor. The heat exchanger was designed to dissipate 1000 W, while achieving a low thermal resistance of 0.05 K/W and a COP of 30 within a 10 × 10 x 10 cm^3 volume.

22.3: Flexible and Conformal Thermal Ground Planes **(11:10)**

C. Oshman, Q. Li, W. Wang, C.-Y. Lin, L.-A. Liew, A. Abdulagatov, M. Kong, S. Song, S. M. George, V. M. Bright, R. Yang, Y.-C. Lee
University of Colorado at Boulder, Boulder, CO

X. Dai, C. Li
University of South Carolina, Columbia, SC

S. P. Rawal, R. J. Monson
Lockheed Martin Corp., Denver, CO

Novel flexible thermal ground planes (FTGPs) based on heat-pipe technology will be reported. The FTGPs' effective thermal conductivities are much higher than those of copper and graphite heat spreaders. Mylar-aluminum, copper-Kapton, and all-polymer FTGP prototypes and advanced technologies which will further enable high-performance FTGPs will also be reported.

22.4: High-Heat-Flux High-Power Low-Resistance, Low-CTE Two-Phase Thermal Ground Planes for Direct-Die-Attach Applications **(11:30)**

P. Dussinger
Advanced Cooling Technologies, Inc., Lancaster, PA

Y. S. Ju, I. Catton
University of California at Los Angeles, Los Angeles, CA

M. Kaviany
University of Michigan, Ann Arbor, MI

A low coefficient of thermal expansion (CTE) vapor chamber for heat transport and spreading was developed for the thermal management of high-power high-heat-flux silicon, gallium arsenide, or gallium nitride microelectronics chips. The development effort focused on innovative wick structures and low-CTE envelope materials, specifically aluminum nitride ceramic with direct-bond copper. The low-CTE construction allows for direct die attach, eliminating the thermal resistance of the die substrate and associated interface.

LUNCH **(12:00)**

Session 23

TRUSTED ELECTRONICS II

Thursday, 22 March / 10:30 am – 12:10 pm / Bronze Room 2

Chair: **D. G. Both**
National Security Agency, Ft. Meade, MD

Co Chair: **B. S. Cohen**
Institute for Defense Analyses, Alexandria, VA

23.1: Electrical Test Methods for Counterfeit Device Avoidance (10:30)

M. Marshall
Integra Technologies, Wichita, KS

Integra Technologies has had over 25 years of experience in testing and qualifying IC components, both for IC manufacturers and users of the devices. Over the past decade, Integra Technologies has been on the forefront of testing and evaluation methods for the detection of counterfeit components. The best electrical test methods and the risk trade-off inherent in dealing with the counterfeit issues will be discussed. Included will be many real examples and experiences encountered with counterfeit parts. The presentation will also include some of the risks and concerns prevalent in today's testing laboratory industry. Discussion will include summarizing the draft document and explaining the purpose for the effort. Wide industry acceptance is expected with the documents release.

23.2: CDR: Combating Die Recovery (10:50)

X. Zhang, N. Tuzzio, M. Tehranipoor
University of Connecticut, Storrs, CT

The recycling of integrated circuits (ICs) has become a major problem in recent years, potentially impacting the security and reliability of electronic systems bound for military, financial, or other critical applications. Two novel combating die recovery (CDR) methods are proposed to distinguish recovered ICs and fresh ICs. By using statistical data analysis, the separation of process and temperature variations from aging effects on the circuit's aging sensor is possible. Simulation results using 90-nm technology and silicon results from 90-nm test chips demonstrated the effectiveness of this technique for recycled IC identification.

23.3: Applying IC Testing Concepts to Secure ICs (11:10)

J. Rajendran, R. Karri
Polytechnic Institute of New York University, Brooklyn, NY

Y. Pino
AFRL., Rome, NY

O. Sinanoglu
New York University at Abu Dhabi, Abu Dhabi, UAE

One way to protect ICs from supply-chain attacks is to encrypt the design by inserting additional gates into it such that correct outputs are produced only on applying-specific inputs to these gates. IC testing concepts, such as fault excitation, propagation, and masking, were used to develop an effective logic encryption technique.

23.4: Unique Number Generator (UNG) IP First-Time Instantiation in Trusted Foundry SiGe BiCMOS (11:30)

J. Torneden
Kansas City Plant, Kansas City, MO

The Unique Number Generator (UNG) is an IP cell that ensures a chain of custody of ICs. The UNG cell generates a 256-bit signature for every chip in which it is instanced. Each chip's signature can be recorded at the end of fabrication and verified in the field. Currently, the device has been verified in National Semiconductor's C9T5V (180nm) process. This IP has been ported to IBMs CMRF8SF and BICMOS8HP technologies in an effort to expand the scope of the Trusted concept. Once the UNG operation has been verified in these two processes then it can become available to the Trusted IC design community to further promote program security. Development in IBM technologies expands the potential customer base, and these processes make advancements in the IP design apparent. For example, by utilizing the SiGe process, attempts can be made to radiation harden the design, expanding its deployment opportunities.

23.5: Scalable Physical Unclonable Functions (11:50)

M-D. Mandel, Y. D. M'ra hi
Verayo, Inc., San Jose, CA

S. Devadas
MIT, Cambridge, MA

A scalable PUF architecture will be presented. PUF Hamming Authentication (PHA) is small in footprint; an in-exhaustible number of challenge/response pairs prevent replay attacks, making the PUF ideal for multi-party trusted supply-chain applications. PUF Key Generation (PKG) generates device-unique keys for higher-value cryptographic applications. PUF Key eXchange (PKX) provides a hardware "SSL" connection and is ideal for multi-factor authentication, key distribution, and end-point security management for critical infrastructure.

LUNCH (12:10)

Session 24

ADVANCED RF/MMW TECHNOLOGIES II

Thursday, 22 March / 10:30 am – 12:00 pm / Bronze Room 3

Chair: **J. B. Muldavin**
MIT Lincoln Lab, Lexington, MA

Co Chair: **R. Polcawich**
Army Research Laboratory, Adelphi, MD

24.1: Progress of a Wideband 220-GHz 50-W Serpentine Waveguide Amplifier: Circuit Microfabrication and Cold Testing (10:30)

C. D. Joye, J. P. Calame, A. M. Cook, D. K. Abe, B. Levush
Naval Research Laboratory, Washington, DC

K. T. Nguyen, E. L. Wright, D. E. Pershing
Beam-Wave Research, Inc., Bethesda, MD

M. Garven
SAIC, McLean, VA

A 220-GHz 50-W vacuum electron amplifier is under development utilizing an 11.7-kV 120-mA electron beam. The amplifier showcases a novel microfabrication technique employing embedded polymer monofilaments to simultaneously fabricate the circuit and beam tunnel in a single UV-LIGA step. The method shows promise for fabricating beam tunnels and circuits into the THz range.

24.2: High-Dynamic-Range RF Noise-Shaping Multibit ΣΔ ADC Demonstration (10:50)

L. E. Pellon
Lockheed Martin, Moorestown, NJ

A band-pass multibit ΣΔ ADC that demonstrates a high-dynamic-range digital receiver topology for high-interference-processing applications will be presented. The architecture employs a delay-based high-NPR recursive transversal filter (RTF) and a 6-bit ADC–DAC, combined with a non-linear filter for error correction. A multichip module implementation, operated near 4 GSPS provides center frequency and bandwidth tuning over the 0.2–1-GHz range. Performance drivers, implications, and scaling capabilities will also be discussed.

24.3: Full W-Band Power MMIC Using Low-Cost GaAs pHEMT Process (11:10)

B. Kim, J. Schellenberg
QuinStar Technology, Inc., Torrance, CA

The first full-band W-band MMIC power amplifier using a commercial GaAs process will be reported. The MMIC, using a 0.1-μm GaAs pHEMT process, has demonstrated a small-signal gain of greater than 15 dB with a typical P_{sat} of 14 dBm across the full 75–110-GHz frequency band.

24.4: Monolithic Low-Phase-Noise CMOS FBAR Non-Linear Oscillators **(11:30)**

A. Imani, H. Hashemi
University of Southern California, Los Angeles, CA

Design and experimental results of film bulk-acoustic-wave resonator (FBAR) non-linear CMOS oscillators with low-phase noise will be presented. A model for the non-linear FBAR, including the memory effect, is proposed, and its effect on the oscillator phase-noise performance was demonstrated. A proof-of-concept 1.5-GHz FBAR CMOS oscillator, consuming 40-mW DC power, with a measured phase noise of –110 dBc/Hz at 1 kHz, 125 dBc/Hz at 10 kHz, 145 dBc/Hz at 100 kHz, and –160 dBc/Hz at 10 MHz offset frequencies will be reported.

LUNCH **(12:00)**

Session 25

THERMAL MANAGEMENT III

Thursday, 22 March / 1:30 – 3:00 pm / Bronze Room 1

Chair: **A. Bar-Cohen**
DARPA, Arlington, VA

Co Chair: **K. Bloschock**
System Planning Corp., Arlington, VA

25.1: Development of a Compliant Nanothermal Interface Material **(1:30)**

D. Shaddock, R. Bahadur, S. Weaver
General Electric Global Research, Niskayuna, NY

I. Chasiotis
University of Illinois at Urbana-Champaign, Urbana, IL

A compliant thermal interface material allows for thin solder bondlines by using a compliant structure of Cu nanosprings sandwiched between two plates of materials to match thermal expansion of their mated materials. The compliance is >100× more compliant than the solder bond allowing for thin bondlines with a resistance < 0.01 cm^2-C/W.

25.2: Stirling Microcooler Array with Elemental In-Plane Flow **(1:50)**

J. Gao, D. Guo, A. J. H. McGaughey, S. Santhanam, S.-C. Yao, G. K. Fedder
Carnegie Mellon University, Pittsburgh, PA

M. Moran
Isotherm Technologies LLC, Medina, OH

W. Anderson, D. Wolf
Advanced Cooling Technologies, Inc., Lancaster, PA

A Stirling-cycle microcooler comprised of an array of microelectro-mechanical elements has its gas flow direction within the plane of the silicon substrate, enabling efficient regeneration and heat transport. Three-dimensional finite-element simulation leads to a coefficient of performance of 7.4 at 100 Hz and 2 bar air, assuming recovery of cold-side work.

25.3: Micro-Stirling Active Cooling Module (MS/ACM) for DoD Electronics Systems **(2:10)**

D. S. Beck
Beck Engineering, Inc., Port Orchard, WA

The Department of Defense (DoD) has many systems that can benefit from the features of a cm-scale micro-refrigerator. Under a DARPA contract, a cm-scale Micro-Stirling Active Cooling Module (MS/ACM) micro-refrigerator has been developed to benefit DoD systems. Under the DARPA contract, a breadboard MS/ACM has been designed, built, and demonstrated.

25.4: Developing Nanowire Solutions for Thermal Cooling **(2:30)**

M. P. Siegal, S. J. Limmer, W. G. Yelton, T. E. Beechem, B. S. Swartzentruber, J. A. Martinez, C. T. Harris, E. A. Shaner
Sandia National Laboratories, Albuquerque, NM

D. L. Medlin, J. L. Lensch-Falk
Sandia National Laboratories, Livermore, CA

High-power electronics and photonics require improvements for both active cooling and heat dissipation: these can be addressed by thermoelectric nanowires and carbon nanotubes, respectively. To date, success has been severely limited by materials-quality issues. The materials structure and property correlation studies that can enable the development of nanowire cooling solutions will be presented.

BREAK **(3:00)**

Session 26

STT-RAM AND LOGIC

Thursday, 22 March / 1:30 – 3:00 pm / Bronze Room 2

Chair: **D. Shenoy**
DARPA, Arlington, VA

Co Chair: **V. Sharma**
IDA, Alexandria, VA

26.1: Progress and Prospects of Spin Transfer Torque Random-Access Memory **(1:30)**

E. Chen, D. Apalkov, A. Driskill-Smith, A. Khvalkovskiy, D. Lottis, K. Moon, V. Nikitin, A. Ong, X. Tang, S. Watts, M. Krounbi
Grandis, Milpitas, CA

R. Shull
National Institute of Standards and Technology, Washington, DC

K. Bussmann
Naval Research Laboratory, Washington, DC

S. Schäfer, T. Mewes
University of Alabama, Tuscaloosa, AL

Progress made on the material improvement, device design, wafer processing, integration with CMOS, and testing of STT-RAM memory chips to meet the requirements of BAA 08-16 will be reported. Initial radiation testing will also be discussed.

26.2: Spin-Transfer-Torque MRAM for Ultrafast Low-Power Nonvolatile Electronics **(1:50)**

M. D. Lewis, J. G. Alzate, P. Upadhyaya, H. Jiang, Z. Zeng, A. Kovalev, Y. Tserkovnyak, K. Galatsis, P. K. Amiri, K. L. Wang
University of California, Los Angeles, CA

G. Rowlands, Y.-J. Chen
University of California, Irvine, CA

H. Zhao, A. Lyle, T. Rahman, J. Wang
University of Minnesota, Minneapolis, Minneapolis, MN

J. A. Katine
Hitachi Global Storage Technologies, San Jose, CA

J. Langer
Singulus Technologies, Kahl am Main, Germany

Three different designs of magnetic tunnel junctions (in-plane, out-of-plane, and combined) for spin-transfer-torque random-access-memory applications have been investigated to optimize performance. Write energy and write current density have been significantly reduced and ultrafast switching speeds have been achieved.

26.3: Novel Materials and Structures for Spin-Torque-Transfer Magnetic Random-Access Memory (STT-MRAM) **(2:10)**

S. Wolf, J. Lu, J. Poon, A. W. Ghosh, M. Stan
University of Virginia, Charlottesville, VA

Spin-transfer-torque random-access memory (STT-RAM), the successor to MRAM, can provide a truly universal memory that can in principle replace most, if not all, semiconductor memories in the near future. It utilizes a spin-polarized current to directly switch the magnetization of a nanomagnet. The STT switching technique brings significant advantages to magnetoresistive random-access memory (MRAM). For the first time, magnetic tunnel junction (MTJ) materials based memory devices are being developed at the same advanced nodes as mainstream semiconductor memories.

26.4: Embedded STT-MRAM for System-on-Chips: Device, Design, and Integration **(2:30)**

S. H. Kang
Qualcomm, Inc., San Diego, CA

This paper addresses embedded STT-MRAM for mobile system-on-chip (SoC) applications. Recent technological advances are highlighted with an emphasis on integrating STT-MRAM into a leading-edge low-power CMOS platform to capture emerging product opportunities as a scalable nonvolatile working memory.

BREAK **(3:00)**

Session 27

POWER ELECTRONICS I

Thursday, 22 March / 1:30 – 3:00 pm / Bronze Room 3

Chair: **F. Kub**
Naval Research Laboratory, Washington, DC

Co-Chair: **A. R. Hefner**
NIST, Gaithersburg, MD

27.1: Advanced SiC Power Technology for Next-Generation Power Electronics **(1:30)**

D. Grider, A. Agarwal, S.-H. Ryu, L. Cheng, S. Dhar, C. Capell, C. Jonas, A. Gupta, M. Das, J. Palmour
Cree, Inc., Durham, NC

Recent advances in the development of advanced 1200-V SiC DMOSFETs, 10-kV SiC DMOSFETs, 10-kV SiC GTOs, and 15-kV SiC IGBTs for next-generation power-electronics systems applications will be presented.

27.2: Compact High-Voltage Power Converters Using High-Frequency High-Voltage SiC Devices **(1:50)**

R. Raju, R. Steigerwald, M. Schutten, M. Dame
General Electric Co., Niskayuna, NY

M. Das, D. Grider
Cree, Durham, NC

S. Leslie
Powerex, Pittsburgh, PA

T. Challita
IAP Research, Dayton, OH

W. Reass
LANL, Los Alamos, NM

A. Hefner
NIST, Gaithersburg, MD

New high-voltahe high-frequency SiC devices and magnetic components can enable the design of compact, efficient power converters. This paper will discuss a 1-MVA 13.8-kV/465-V solid-state transformer using 10-kV SiC devices developed under the DARPA/ONR High Power Electronics program.

27.3: Power Electronics for the More Electric Aircraft (MEA) **(2:10)**

J. A. Weimer
AFRL, Wright-Patterson AFB, Dayton, OH

The MEA initiative embraces the concept of using electrical power for driving aircraft subsystems which are typically driven by hydraulic, pneumatic, and mechanical power. Power electronics provides the means to drive electric actuators, electric fuel pumps, and other subsystems at variable speeds. Furthermore, power electronics is used to condition the power from the aircraft's generators and used in over-current circuit-protection devices, replacing conventional circuit breakers and contactors. review The role of power electronics for the MEA initiative will be reviewed.

27.4: Applications of SiC JFETs Modules for Power System Control and Protection **(2:30)**

D. C. Sheridan, R. Schrader, K. Speer, J. B. Casady
Semisouth Labs., Inc., Starkville, MS

M. S. Mazzola
Mississippi State University, Starkville, MS

J. D. Scofield
AFRL, Wright-Patterson AFB, Dayton, OH

Normally-off and normally-on 1200-V SiC vertical JFETs were used in high-temperature and high-power modules for power conversion and circuit-breaker applications up to 250°C.

BREAK **(3:00)**

Session 28

SUPERCONDUCTING ELECTRONICS

Thursday, 22 March / 3:30 – 5:00 pm / Bronze Room 1

Chair: **M. Gouker**
MIT Lincoln Laboratory, Lexington, MA

Co Chair: **S. Holmes**
Booz Allen Hamilton, Arlington, VA

28.1: Prospects for Energy-Efficient Superconducting Computing (3:30)

M. A. Manheimer, D. S. Holmes
Laboratory for Physical Science, College Park, MD

Power and energy use by high-end computing systems is a significant and growing problem. Superconducting computing is re-evaluated based on recent developments. Potential advantages are identified as well as areas requiring further development.

28.2: Ultra-Low-Power Superconducting Digital Logic Demonstrations (3:50)

Q. P. Herr, A. Y. Herr, O. T. Oberg, O. Naaman, S. B. Shauck
Northrop Grumman Systems Corp., Baltimore, MD

Reciprocal quantum logic has recently demonstrated zero static power dissipation, thermally limited dynamic power dissipation, high clock stability, high operating margins, and low BER. In a further demonstration, an 8-bit carry look-ahead adder operating at 9.8 GHz with 150-psec latency and operating at 6.2 GHz with 500-nW power dissipation will be reported.

28.3: ERSFQ: Zero-Static-Power Dissipation Single-Flux Quantum Logic (4:10)

A. F. Kirichenko, S. Sarwana, I. V. Vernik
HYPRES, Inc., Elmsford, NY

A novel resistor-free approach to dc biasing of single-flux quantum circuis will be represented. Called energy-efficient RSFQ (ERSFQ) logic, this new variant dissipates orders of magnitude less power than conventional RSFQ logic while operating and has zero power dissipation in the inactive mode. By using this approach, at high speed (exceeding 20 GHz) a number of complex digital circuits including a 20-stage static frequency divider, a digitizer for detector readout (ADC), and an 8-bit parallel adder have been demonstrated.

28.4: Real-Time Adaptive Filtering Using Reciprocal Quantum Logic (4:30)

A. Y. Herr, Q. P. Herr, S. B. Shauck, P. H. Feinberg
Northrop Grumman Systems Corp., Baltimore, MD

Non-linear adaptive algorithms are capable of delivering nearly optimum signal detection in multi-channel systems with excellent stability and convergence properties, but can be computationally prohibitive. Superconducting digital logic featuring Tera-OPS throughput, nanosecond latency, and negligible power dissipation is uniquely suited to adaptive signal detection in highly non-stationary environments.

Session 29

TECHNOLOGY POTPOURRI

Thursday, 22 March / 3:30 – 5:10 pm / Bronze Room 2

Chair: **D. J. Radack**
Institute for Defense Analyses, Alexandria, VA

Co Chair: **D. G. Both**
National Security Agency, Ft. Meade, MD

29.1: Reliability Demonstration of a Commercial 90-nm Bulk CMOS Process for Space-Level Applications **(3:30)**

R. Ciccariello, P. Milliken, C. Hagen, D. Wilkin
Aeroflex Colorado Springs, Inc., Colorado Springs, CO

D. Pierce
Sandia Technologies, Inc., Albuquerque, NM

The results of a Failure Modes and Effects Analysis (FMEA) and reliability demonstration performed on IBM's 90-nm Bulk CMOS 9SF process manufactured at IBM's East Fishkill facility will be reported. The data will show that IBM's commercial process, when combined with RHBD techniques, is suitable for use in aerospace applications.

29.2: PolyStrata Millimeter-wave Tunable Filters **(3:50)**

J. R. Reid, P. Ralston, W. Stacy, C. Snelgrove, J.-M. Rollin
Nuvotronics, LLC, Radford, VA

A Ka-band tunable filter will be described. At 36.7 GHz, the filter has a 217-MHz bandwidth (0.59%) with a mid-band insertion loss of 2.35 dB. The filter is capable of tuning its center frequency over a range greater than 5%. The unloaded resonator quality factor is estimated at 540. To our knowledge this is the highest performance reported for a tunable filter using planar fabrication technologies.

29.3: Recent Advances in GaN-on-Diamond HEMTs **(4:10)**

D. Francis, K. D. Matthews, F. Lowe, Q. Diduck, D. Babic, S. Zaitsev, F. Faili, C. Khandavalli, J. Smart, F. Ejeckam
Group4 Labs., Inc., Fremont, CA

GaN-on-diamond has the potential for providing the most efficient heat extraction from GaN HEMTs of any material system. To fully realize the potential, the wafer must be perfected. In this work, we discuss optimization GaN-on-diamond as well as the mounting wafers for fabrication and early devices reliability results.

29.4: Three-Dimensional Package-Integrated Antennas for Electrically Small Sensor Nodes **(4:30)**

J. J. Adams, J. T. Bernhard, S. C. Slimmer, J. A. Lewis
University of Illinois at Urbana-Champaign, Urbana, IL

New conformal printing techniques enable the integration of antennas directly onto the package of a small wireless sensor node. This volume-filling approach ensures maximum performance of the antenna, increasing battery life, data rate, or range. An antenna with an integrated source will be discussed, and measured results from these package-integrated antennas will be presented.

29.5: CVD Graphene Radio-Frequency Transistor Technology on Rigid and Flexible/Conformable Substrates for Ubiquitous High-Speed Communications **(4:50)**

O. M. Nayfeh, B. Nichols, T. Ivanov, R. Proie, G. Meissener
Army Research Laboratory, Adelphi, MD

Recent advances on the ARL large-area chemical-vapor-deposited (CVD) graphene-based radio-frequency transistor technology integrated on both rigid and mechanically flexible/conformable substrates will be presented. Both GHz f_t (current-gain cutoff) and f_{max} (maximum frequency of oscillation) were achieved, and the dependence on bias conditions iwill be examined. Technological challenges as well as physical limitations will also be discussed. The results could enable a new generation of ubiquitous high-speed communications electronics for the U.S. Soldier.

Session 30

POWER ELECTRONICS II

Thursday, 22 March / 3:30 – 5:00 pm / Bronze Room 3

Chair: **A. R. Hefner**
NIST, Gaithersburg, MD

Co Chair: **F. Kub**
Naval Research Laboratory, Washington, DC

30.1: High-Temperature Wide-Bandgap Power Modules for High-Performance Systems **(3:30)**

T. McNutt, A. Lostetter, M. Schupbach, J. Hornberger, B. McPherson, B. Reese, R. Shaw, E. Cilio, W. Cilio, B. Passmore
Arkansas Power Electronics International, Inc. (APEI, Inc.), Fayetteville, AR

High-performance high-temperature power modules for extreme environment systems and applications to exploit the advantages of wide-bandgap semiconductors have been developed. These power modules are rated >1200 V, >100 A, >250°C, and are designed to house any wide-bandgap device.

30.2: Radiation-Tolerant Enhancement-Mode Gallium Nitride (eGaN®) FET Characteristics **(3:50)**

A. Lidow
Efficient Power Conversion Corp., El Segundo, CA

K. Smalley
Microsemi Corp., Lawrence, MA

eGaN FETs have demonstrated their ability to operate reliably under harsh environmental conditions and high radiation conditions. New results characterizing the stability of these devices under radiation exposure as well as showing their capability in high-performance DC-DC converters and operating at frequencies as high as 1 GHz will be presented.

30.3: High-Voltage GaN Power HEMTs and Diodes **(4:10)**

L. Shen, Y. Wu, R. Coffie, Y. Dora, P. Parikh, U. Mishra
Transphorm, Inc., Goleta, CA

Production readiness and performance of 600-V-class GaN HEMTs and diodes will be presented. Large-area devices were successfully manufactured, showing total dynamic on-resistance below 150 mΩ and leakage below 10 μA at 600 V and 150°C. Lower switching on-resistance, higher pulsed current, and lower output charging energy than conventional Si products were simultaneously achieved. A 1-kW, 99% efficient total GaN boost converter has been demonstrated at a PWM frequency of 100 kHz.

30.4: Normally-Off AlGaN/GaN HEMT with Nanocrystalline Diamond Heat-Spreading Layer **(4:30)**

T. J. Anderson, K. D. Hobart, C. R. Eddy, Jr., F. J. Kub,
Naval Research Laboratory, Washington, DC

T. I. Feygelson
SAIC, Inc., Washington, DC

M. A. Mastro, J. D. Caldwell, J. K. Hite, B. B. Pate
Naval Research Laboratory, Washington, DC

An approach to achieve normally-off AlGaN/GaN HEMT employing selective wet chemical etch to implement an ultra-thin (4-nm-thick) AlGaN barrier layer while maintaining low source and drain access resistance has been demonstrated. In addition, nanocrystalline diamond films for lateral heat spreading were incorporated into the device structure prior to gate fabrication, achieving 20% reduction in channel temperature.

Session 31

GENERAL POSTER

Thursday, 22 March / 9:00 am – 12:00 pm / Gold/Silver Ballroom

31.1: Closure for a Plane Fin Heat Sink with Scale-Roughened Surfaces for Volume-Averaging Theory (VAT) Based Modeling

F. Zhou, D. J. Geb, G. W. DeMoulin, I. Catton
University of California, Los Angeles, CA

An effort to obtain closure for a Volume Averaging Theory (VAT) based model of a plane fin heat sink (PFHS) with scale-roughened surfaces by evaluating the closure terms for the model using computer fluid dynamics (CFD) will be presented. To complete the VAT-based model, proper closure is needed, which is related to a local friction factor and a heat-transfer coefficient of a Representative Elementary Volume (REV). In this work, CFD was used to obtain detailed solutions of flow and heat transfer through an element of the scale-roughened heat sink and use these results to evaluate the closure terms needed for a fast running VAT-based code, which can then be used to solve the heat-transfer characteristics of a higher-level heat sink. The objective is to show how heat sinks can be modeled as a porous media based on VAT and how CFD can be used in place of a detailed, often formidable, experimental effort to obtain closure for a VAT-based model.

31.2: Multi-Beam Antenna Systems Using Third-Generation Miniature Reconfigurable Beamformers

M. P. DeLaquil, C. E. Baucom
L-3 Communications ComCept Division, Rockwall, TX

A new high-gain, electronically steerable, multi-beam antenna system will be described. By using a new high-performance true-time-delay MMIC, an antenna system providing eight simultaneous, independently steerable outputs was created. This antenna provides superior RF performance while requiring 5x less weight than similar legacy systems.

31.3: Investigation of the Properties of Metamaterials Exhibiting Anisotropic Permeability and Permittivity for VHF/UHF Antenna Applications

G. Mitchell
Army Research Laboratory, Adelphi, MD

Cavity-backed antennas are frequently used to achieve desired characteristics in antenna performance. At low VHF and UHF frequencies the depth of the cavity comprises the bulk of the antenna system especially for planar apertures. The emergence of metamaterials with high permittivity and permeability exhibiting low losses at these frequencies introduces a way to reduce cavity depth in these systems. These materials can be inherently anisotropic, and, therefore, the transverse Green's function for a lossless magneto-dielectric substrate was derived.

31.4: Non-Linear Modeling of GaN Devices for High-Efficiency Power-Amplifier Design

K. Mcknight
Army Research Laboratory, Adelphi, MD

A non-linear model for GaN transistors with an emphasis on high-efficiency switching-mode power-amplifier design will be presented. The primary losses for switch-mode power amplifiers are caused by the drain-to-source capacitance. Along the class-B load line, the drain-to-source capacitance exhibits non-linear behavior which is a function of both gate and drain voltages. A non-linear model which incorporates this behavior along with temperature and dispersion effects in GaN devices will be presented. A detailed description of the extraction process including the use of Pulsed IV measurements will be presented. Finally, the model will be used to design a broadband class-F amplifier at 10 GHz.

31.5: High-Dynamic-Range High-IP3 Low-Power Amplifier

D. R. Helms
Lockheed Martin, Burlington, MA

J. Sweder, T. P. Higgins, B. Ingersoll, M. Gruber
Lockheed Martin, Moorestown, NJ

A high-dynamic-range amplifier with a low-noise high-intercept point, demonstrates high dynamic range while operating under low dissipated power. The amplifier provided 34 dBm of input third-order intercept point (IIP3) at a noise figure of 2.5 dB while using only 2.2 W of power.

31.6: IBM BiCMOS 9HP IP Development Study

S. Ventrone, A. M. Chu, K. Ford, D. Scagnelli, D. Seitzer, R. Shetty, J. Zimmerman, J. Pekarik, H. Wu, R. Piro, J. Ellis-Monaghan
IBM, Essex Junction, VT

The creation of IBM 9HP BiCMOS technology, taking into consideration IP and COT tool development to be more tightly coupled into the early technology phase, will be described. Integrating IP and tools into the early 9HP development phase potentially lessens technology changes and improved bring-up is possible.

31.7: High-Power GaN HEMT with Low-Temperature Bonded Diamond Substrate Technology

P. C. Chao, K. Chu, P. M. Smith, C. Creamer, S. Sweetland
BAE Systems, Nashua, NH

D. Francis, S. Zaitsev, F. Ejeckam
Group4 Labs., Fremont, CA

J. Fu
JPSA, Manchester, NH

S. Guo
IQE/RF, Somerset, NJ

A new GaN-on-Diamond HEMT, which will be more efficient, provides a 10,000 hour longer operating lifetime and also enables smaller chip size or >5× more power per unit chip area than the conventional GaN HEMT, will be described. The new device is ideally suited for wideband EW PAs because they are the most thermally challenging.

31.8: Advanced High-Performance SRAM for Space Applications

S. Doyle, J. Ross, J. Maimon, D. Lee, A. Kelly, R. Brown, N. Haddad, R. Brown
BAE Systems, Manassas, VA

Design techniques, qualification test results, and production status on a new low-cost high-speed 10-nsec deep submicron rad-hard 20-Mbit SRAM MCM will be presented. Electrical characterization and radiation test results will be discussed. This high-density VLSI product utilizes integrated process features along with advanced design techniques and is intended for use in space and other strategic rad-hard applications.

31.9: Pliable Smart-Sensor System

R. L. Chaney, D. R. Hackler, D. G. Wilson
American Semiconductor, Inc., Boise, ID

Sensors and sensor systems proliferate towards becoming ubiquitous. As the demand for sensors grows, expectations of capabilities, both for performance and mechanical attributes, increases. Intelligent sensors in a pliable form factor will be instrumental in sensor market growth.

31.10: Radiation Testing of Aluminum Nitride Microresonators

M. S. Baker, R. H. Olsson III, J. R. Schwank
Sandia National Laboratories, Albuquerque, NM

The result of a series of radiation experiments performed on aluminum nitride microresonator-based RF filters to quantify any change in center frequency, bandwidth, and insertion loss after exposure will be reported. Devices were tested using gamma, neutron, electron, and proton irradiation, with no measureable change in performance detected.

31.11: Using DPD to Improve the Output Power and Linearity of Millimeter-Wave Power Amplifiers

B. Kim, T. Phan, J. Schellenberg
QuinStar Technology, Inc., Torrance, CA

The use of digital pre-distortion (DPD) to linearize and increase the output power delivered for two commercial-off-the-shelf (COTS) 44-GHz power amplifiers will be reported. For a 64-QAM 10-MHz modulation bandwidth signal, an ACPR level of better than – 40 dBc with a 6-dB improvement in average output power has been demonstrated.

31.12: RF MEMS Switch for DC to Ka Band

D. H. Brenman, K. Saechao, K. M. Chang, S. Chao, W. T. Tang, M. B. Cohn
MicroAssembly Technologies, Inc., Richmond, CA

C. Hua, B. Kirby, C. Chao
Laserlith Corp., Grand Forks, ND

A two-substrate MEMS process with integrated hermetic packaging has been developed and characterized for RF MEMS relay components. This architecture is based on a metal–metal bonding process that is performed under CMOS-compatible temperatures. This approach enables the separate processing of a MEMS substrate and a RF substrate. Separate processing of the two substrates enables process optimization without concern for incompatibility between the MEMS processes steps and the RF processing steps. The fabrication process, RF performance data, and contact reliability results will be discussed.

31.13: High-Efficiency Integrated Air-Cooler for Electronics Applications

B. St. Rock
UTRC, East Hartford, CT

An integrated air cooler to reduce airside thermal resistance by 80% over state-of-the-art systems operating at equivalent power has been demonstrated. The efficiency improvements were achieved through significant increases in blower efficiency and integrated design.

31.14: Electrically Small Direction-of-Arrival Estimation: Validation in Outdoor Environments

M. J. Slater, C. D. Schmitz, D. L. Jones, J. T. Bernhard
University of Illinois at Urbana-Champaign, Urbana, IL

Electrically small direction finding fosters a new generation of functionality in vehicle-mounted and unit-borne environment awareness. Measurements of an electrically small direction-finding system were performed in an outdoor environment. The effects of various noise environments, scatterers, transmitter distance, *etc.,* on direction-of-arrival estimation using the MuSiC algorithm were examined.

31.15: Mechanical Computing on the Micro-Scale: A Low-Proie Rad-Hard Digital Relay Architecture

R. M. Proie, Jr., R. G. Polcawich, J. S. Pulskamp, T. Ivanov
Army Research Laboratory, Adelphi, MD

A PZT MEMS digital switch, with intrinsic radiation insensitivity, was designed as a low-power control system intended to create energy-efficient microcontrollers and provide integrated control over other MEMS or high-voltage platforms. To date, all building blocks required to produce fully mechanical computing have been demonstrated with fabricated components.

31.16: Placement-Insensitive Miniaturized Slot Antennas for RFID Systems

J. E. Ruyle
University of Oklahoma, Norman, OK

J. T. Bernhard
University of Illinois at Urbana-Champaign, Urbana, IL

A miniaturization and multi-band design technique has been shown for a placement-insensitive RFID antenna. The slot antenna, the effective inverse of the dipole, is shown to be an effective RFID antenna for environment-independent peel-and-stick applications expanding the purview of peel-and-stick RFID systems to track all object types.

31.17: Trusted Foundry Advanced Technology Hybrid Multi-Project Wafer

D. M. Carpentier
IBM Corp., Essex Junction, VT

Advanced Technology Trusted Foundry Hybrid Multi Project Wafers with the ever-increasing cost of advanced node technology access, cost can become prohibitive for prototype circuit design validation. This approach of sharing mask cost sharing with various entities has provided a vehicle for leading-edge technology access in the both the 45- and 32-nm nodes with great success. The concept was initiated to share the development cost among the Trusted Foundry, IBM Development Teams, and commercial interest and provides a vehicle to share resources and ultimately reduce everyone's cost to participate.

31.18: Radiation Studies of STT-RAM Materials and Devices

K. Bussmann, P. McMarr, H. Hughes, S.-F. Cheng
Naval Research Laboratory, Washington, DC

R. Shull, A. P. Chen
National Institute of Standards and Technology, Gaithersburg, MD

S. Schäfer, T. Mewes
University of Alabama, Tuscaloosa, AL

E. Chen
Grandis, Milpitas, CA

Co-60 radiation testing of STT-RAM films and devices having in-plane magnetization have been performed. The materials have a biased, synthetic antiferromagnet spin-valve architecture composed of Si/SiO_2 (substrate)/ PtMn 15-nm/CoFe 2.5/Ru 1.0/CoFeB 2.5/MgO 1.2/CoFeB 2.2/Ta 5/Cu 20/ Ru 7 (top). Measurements of M *vs.* H, ferromagnetic resonance and tunnel magnetoresistance (TMR) were performed on unpatterned films before and after exposure to 1- and 10-MRad (Si) Co-60 gamma rays. and no changes were observed in the associated material properties. Patterned devices show a TMR > 75% with no changes to the bit state on exposure to 1-MRad (Si).

31.19: Wideband Amplifier Linearization

N. Kingsley
Auriga Microwave, Chelmsford, MA

The Auriga Microwave linear amplifier is capable of providing excellent power, efficiency, and linearity simultaneously across a very wide instantaneous bandwidth (multi-octave). A family of products was created to offer a range of size-performance trade-offs. Applications include radar, electronic warfare, and counter electronic-warfare (jamming) systems.

31.20: Ultra-Low-Power Sub-V_t Digital Circuits with Autonomous Block-Level Supply Control

G. Ansel, D. Savage, X. Zhang, B. Evans, D. Roberts, J. Kelly
Camgian Microsystems, Starkville, MS

R. Reese
Mississippi State University, Mississippi State, MS

A clockless logic design methodology employing autonomous block-level power supply control to achieve large energy savings for systems with variable data rate will be presented. Circuits set the power supply voltage for a logic block based on data-rate requirements continuously monitored at the block signal interfaces.

31.21: Adaptive Voltage Scaling and Parallelism in Delay-Insensitive Asynchronous Circuits for Ultra-Low Power

B. Hollosi, J. Di
University of Arkansas, Fayetteville, AR

The landscape for digital integrated circuit (IC) design has changed from one driven by performance to one driven by energy or more-balanced design goals. This shift requires next-generation circuits to be adaptable and flexible to ever-widening application requirements. Techniques such as parallelism, dynamic voltage scaling (DVS), and subthreshold operation have shown effectiveness. In this paper, a scalable delay-insensitive asynchronous platform architecture which implements parallelism and aggressive DVS for energy efficiency and the corresponding design flow will be presented.

31.22: Trusted FPGAs

A. Gahoonia, K. Bergevin, J. lloyd
Defense Microelectronics Activity, McClellan, CA

FPGAs are increasingly being used in the heart of DoD systems. There are several initiatives and techniques to protect the trustworthiness of the design implemented on the FPGA, but no effort has been made to protect the base array. A DMEA initiative planned to begin in FY-12 will look at ensuring that the DoD has a selection of Trusted FPGAs to fulfill this need.

31.23: 19-dBm 30-GHz SiGe Power Amplifier

T. J. Farmer, A. Darwish, B. Huebschman, E. Viveiros, H. A. Hung
Army Research Laboratory, Adelphi, MD

M. E. Zaghloul
George Washington University, Washington, DC

A 30-GHz SiGe power amplifier, implementing the High Voltage/High Power (HiVP) architecture that achieved a PSAT of 19.0 dBm, will be discussed. The amplifier has been implemented in the commercially available IBM 8HP BiCMOS 120-nm process through the Multi-Project Wafer (MPW) run offered through the Trusted Access Program Office (TAPO) and consumes an area of 0.23 $mm.^2$ At 30 GHz, the small signal gain is 10.0 dB and the 1-dB compression is 16.58 dBm, while the PSAT = 19.0 dBm while achieving an efficiency of 11.47%, a notable achievement in a silicon-based technology at millimeter wave. The innovative HiVP architecture will be discussed and presented for SiGe HBT devices, while simulation, layout details, and fabrication issues will also be discussed.

31.24: Millimeter-Wave and Sub-Millimeter-Wave Waveguide Slotted Antenna Arrays Microfabricated in PolyStrata

A. Boryssenko, K. Vanhille
Nuvotronics, Radford, VA

This work represents a new design technique for low-loss, copper-based, air-filled WG of different cross-sectional and longitudinal geometries to build monolithic slotted radiating apertures in PolyStrata at mmW and sub-mmW frequencies. Illustrations will be provided for recently designed and fabricated low-loss slotted arrays with frequency-steered and shaped beams.

31.25: Ultra-Low-Power General-Purpose Microcontroller

D. G. Wilson, R. L. Chaney, D. R. Hackler
American Semiconductor, Inc., Boise, ID

An ultra-low-power general-purpose microcontroller platform designed to operate at 0.5 V with 50-MHz performance has been developed. The potential dynamic power savings can be up to 13× of similar microcontrollers operating at 1.8 V.

31.26: Tunable Simultaneous Transmit and Receive Architecture for Military Systems

T. Snow
Purdue University, Crane, IN

A compact monopole array architecture that exploits symmetric mutual coupling between elements, using a digital transceiver architecture to actively cancel coupled transmit interference at co-located receive antennas and enabling simultaneous transmit and receive (STAR) operation for electronic warfare and other military systems, will be presented.

31.27: A Fully Monolithic 1-D Coupled-Oscillator Array IC Realizing Electronic Beam-Steering for L-Band Phased-Array Antennas

J. Lopez
Texas Tech University, Lubbock, TX
and
NoiseFigure Reseach, Inc., Lubbock, TX

D. Y. C. Lie
Texas Tech University, Lubbock, TX

B. K. Meadow, J. Cothern
SPAWAR SSC Pacific, San Diego, CA

A novel L-band three-element phased-array antenna system that uses a one-dimensional (1-D) fully monolithic five-element coupled-oscillator array as a miniature electronic phase-shifter (EPS) will be demonstrated. The bilaterally coupled voltage-controlled-oscillator (VCO) network was designed and fabricated in a 0.18-μm IBM SiGe BiCMOS process. Each VCO unit cell consists of a cross-coupled differential pair with an on-chip L-C tank. A digitally controlled on-chip resistors network was used for controlling the bilateral coupling strength across the array. By adjusting the VCO tuning voltages, the self-locked phased-array antenna prototype has demonstrated a ±14° beam scanning inside an anechoic chamber at L-band. These characteristics make this coupled VCO network an attractive choice for possible use in future DoD phased-array applications.

31.28: Orthopternet Communications

B. Epstein, D. Rhodes
OpCoast, LLC, Point Pleasant Beach, NJ

S. Sayilir, B. Jung, H. Diamond
Purdue University, West Lafayette, IN

H. Liang
Texas A&M University, College Station, TX

OrthopterNets represent an ongoing R&D program which aims to apply insects as relays for chemical sensor and other types of messages over distances of a few meters to hundreds or thousands of meters. The networks may be formed among calling insects (*e.g.*, as with crickets and katydids) via acoustic modulation of their calls or through RF transceivers attached to the insects. Ongoing work towards the development of a viable OrthopterNet implementation will be summarized.

31.29: High-Power Frequency-Independent Antennas for Multiple-Octave Wideband Electronic Attack

D. S. Filipovic, J. Mruk, J. Bargeron III, R. Sammeta
University of Colorado, Boulder, CO

Flush-mounted frequency-independent antennas have been traditionally used for receive-only electronic-warfare applications such as radar warning and direction finding. For the first time, this class of antennas can also be designed and used for different high-power electronic attack missions. A planar log-periodic antenna was designed for 10:1 bandwidth linearly polarized operation with VSWR < 2:1. A spiral-helix was developed for 6:1 exceptional quality circularly polarized far-field and VSWR < 1.5. A sinuous antenna was demonstrated for 5:1 dual-circularly and dual-linearly polarized operations with VSWR < 1.4 for the former. All antennas were built and their theoretical performance validated with the impedance and far-field measurements.

31.30: Trusted Secure Processor IP with Anti-Tamper for FPGA-Based EW Systems

E. C. King, M. E. Scheitrum
Atessa, Inc., Pleasanton, CA

This paper highlights Trusted IP with anti-tamper technology that can secure Critical Program Information within new and existing FPGA-based systems, including EW systems, up to the highest U.S. Government-mandated levels. This approach allows program managers to rapidly meet AT requirements and address global-supply-chain security challenges.

31.31: W-Band Transmitter with Injection-Locking Frequency-Multiplier-Based Phase Shifter for Large Phased-Array Systems

Q. J. Gu
University of Florida, Gainesville, FL

A new W-band transmitter with the proposed injection-locking frequency-multiplier-based phase shifter that enables low-frequency LO distribution will be presented. This scheme eliminates sophisticated high-frequency phase shifters and LO distribution networks to reduce system complexity and power consumption, and, more importantly,, offers great array scalability.

Session 32

STUDENT POSTER

Thursday, 22 March / 9:00 am – 12:00 pm / Gold/Silver Ballroom

32.1: Basic Radiation-Effects Mechanisms in Chalcogenide-Based Nanoionic Structures

D. R. Oleksy, H. J. Barnaby, M. Kozicki
Arizona State University, Tempe, AZ

M. Mitkova, M. Ailavajhala, P. Chen
Boise State University, Boise, ID

A programmable metallization cell (PMC) can be made of a solid electrolyte layer sandwiched by two solid metal electrodes. Radiation (*e.g.,* UV and gamma) is known to induce migration of the silver electrode into the electrolyte, which dramatically increases conductance of the cell. It is a goal to conclude the mechanism of this effect and model the effects of various types of radiation on PMCs.

32.2: S-Band Power Amplifier Implementing a Novel Power Divider with Enhanced Harmonic Suppression

C. W. Waiyaki, M. A. Reece
Morgan State University, Baltimore, MD

E. Viveiros
Army Research Laboratory, Adelphi, MD

Planar power combining is frequently used in order to achieve high power levels in microwave SSPA chip designs. In this work, a planar power combiner/divider that incorporates harmonic suppression is implemented within a 20-W high-power-amplifier (HPA) microwave integrated-circuit (MIC) design. This design is compared to a HPA that utilizes a four-way Wilkinson power divider/combiner. Although both divider/combiner circuits exhibit similar combining efficiencies, the HPA that incorporates the new harmonic-tuned divider/combiner, shows a marked improvement in PA linearity performance by over 20 dBm without degradation to the PA power and efficiency.

32.3: Design Choices for High-Speed RHBD Delay-Locked Loops

P. Maillard, T. D. Loveless, W. T. Holman, L. W. Massengill
Vanderbilt University, Nashville, TN

Design guidelines for high-speed rad-hard–by–design delay-locked loop (DLL) circuits will be reported. Hardening-by-design solutions for DLLs (which can also be applied to PLLs) were compared in order to determine the tradeoffs between SET mitigation, power, and area consumption. The RHBD DLL implementing the best tradeoff has been shown to mitigate single-event effects for LET values up to 80 MeV-cm^2/mg at 1-GHz operation in a 90-nm technology and 100 MeV-cm^2/mg at 500-MHz operation in 180-nm technology.

32.4: Single-Event Hardening Techniques for CMOS Operational Amplifier Design

R. W. Blaine, N. M. Atkinson, J. S. Kauppila, S. E. Armstrong, T. D. Loveless, W. T. Holman, L. W. Massengill
Vanderbilt University, Nashville, TN

Three novel rad-hard–by–design (RHBD) techniques to mitigate single-event (SE) voltage transients in CMOS operational amplifiers (op-amps) will be described. The first two techniques, sensitive node active charge cancellation (SNACC) and differential charge cancellation (DCC) layout, leverage charge sharing prevalent in bulk technologies to mitigate transients. Recent work has shown that these techniques can reduce the effects of single events by orders of magnitude, as measured by the error energy at the amplifier's output node. The third RHBD technique involves "peeling" the baseline amplifier into two parallel amplifiers. This peeled amplifier provides a complementary signal path to either maintain or restore signal integrity following a single-event strike. By itself, this technique greatly reduces SET magnitudes and durations, but it can also be combined with SNACC and DCC hardening for greater effectiveness.

32.5: Radiation Response in Metallic and Semiconducting Single-Wall Carbon-Nanotube Thin Films

J. E. Ellis, A. R. Helenic, C. M. Schauerman, T. Mastrangelo, N. Cox, S. M. Hubbard, B. J. Landi
Rochester Institute of Technology, Rochester, NY

C. D. Cress
Naval Research Laboratory, Washington, DC

A non-ionizing radiation-response study of mono-disperse metallic and semi-conducting single-wall carbon nanotubes (SWCNTs), which evaluates the effects of 150-keV boron ion irradiation on the Raman vibrational modes, will be reported.

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