GOMACTech 2024

Government Microcircuit Applications and Critical Technology Conference

PROGRAM

Community and Collaboration

March 18–21, 2024

Embassy Suites by Hilton
Charleston Convention Center
Charleston, South Carolina

www. gomactech.net

GOMACTech 2024
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WELCOME TO GOMACTech 2024

This year's conference theme is "Community and Collaboration," and our robust program supports this theme by fostering awareness and communications to directly meet US government needs in critical technology areas including artificial intelligence (AI)/machine-learning (ML); electronic warfare; energy-efficient systems; advanced material processes; emerging technologies; high-performance digital and mixed-signal technologies; packaging; photonics; power electronics; radiation-hardened systems; radio frequency components; and trusted, assured, and cyber-secure technologies.

The conference starts on Monday, 18 March, with our signature workshops. The first is our annual Trusted Suppliers Industry Day, designed this year to provoke thoughtful conversations and to provide up-to-date information on the many activities being pursued to restore US leadership in semiconductor manufacturing with a semiconductor supply chain that considers security along with technical performance. Monday also features two additional workshops: the Microelectronics Assurance Workshop, focusing on the needs of key stakeholders to ensure the confidentiality and integrity of microelectronic components used in DoD systems; and the On-shore Advanced Packaging Capabilities Workshop, during which the government Reshore Ecosystem for Secure Heterogeneous Advanced Packaged Electronics (RESHAPE) and Defense Production Act Investment (DPAI) teams will present overviews of currently funded on-shore advanced packaging capabilities.

Our Monday programming will conclude with a welcome reception in the Ballroom Foyer, which is open to *all* registered attendees. Please join us!

GOMACTech 2024 formally opens on Tuesday, 19 March, with an outstanding morning Plenary Session that includes keynote addresses by Dr. Jay Lewis, director of the National Semiconductor Technology Center (NSTC) program for the CHIPS R&D Office at the Department of Commerce; Mr. Maynard Holliday, assistant secretary of defense for critical technologies in the Office of the Under Secretary of Defense for Research and Engineering; and Dr. Tina Kaarsberg, acting program manager for the Advanced Materials and Manufacturing Technologies Office (AMMTO) of the U.S. Department of Energy (DOE).

Dr. Lewis's talk is titled, "A Vision for Innovation Through Collaboration in the National Semiconductor Technology Center (NSTC);" Mr. Holliday's address features a "DoD Microelectronics Overview," and Dr. Kaarsberg's talk focuses on "Microelectronics Energy Efficiency and Power Electronics for Zero Carbon."

The keynote addresses are followed by our 2024 Jack S. Kilby Lecture speakers. Dr. Tim Morgan, acting technical director for the Microelectronics Commons, will be speaking on "Microelectronics Commons: A National Network for Defense Microelectronics Innovation," and Dr. Subramanian Iyer, director of the National Advanced Packaging Manufacturing Program (on assignment from UCLA), will speak on "Packaging: Then, Now and in the Future."

This year, we are also hosting five panel discussions: "DoD Workforce Development Accomplishments and Future Directions," STEM the 'Leaky Pipeline' I," and "Leveraging Startup Innovation within the DoD Microelectronics Community," on Wednesday, 20 March; and "STEM the 'Leaky Pipeline' II" and "The T&AM MPW Program Panel Discussion" on Thursday, 21 March.

The plenary, technical, and topical sessions are the major venues for information exchange at the conference, to help the community understand microelectronics and semiconductor investments, needs, and transition opportunities. Other opportunities for technical interaction are provided by the exhibits program, which includes major semiconductor, integrated circuit, and packaging manufacturers and commercial vendors of devices, equipment, software, intellectual properties, systems, and services for nearly every facet of the electronics business. The exhibition opens on Tuesday, 19 March, at noon, and runs through Wednesday, 20 March, at 4:00 pm. On Tuesday evening, all attendees can network in a relaxing atmosphere during the Exhibitors' Reception.

Wednesday evening features the Evening Social, held this year at the South Carolina Aquarium, one of Charleston's premier attractions. A buffet-style dinner will be included, and we will have ample opportunity to view the attractions. This is a ticketed event with an attendance cap; therefore, if you are planning on attending, please buy your ticket before Wednesday.

On Thursday morning, 21 March, a poster session that includes our annual student poster competition will take place. The poster session is an opportunity for direct networking with the researchers on critical topics that affect the United States Government (USG).

This year's technical program is a result of the hard work and enthusiasm of the GOMACTech 2024 Technical Program Committee. The committee members discussed and collaborated on the technical topic areas, sessions, and presentations. The quality of the conference reflects this comprehensive team effort. We hope that you find GOMACTech 2024 an enlightening, rewarding, and enjoyable experience. Thank you for your active participation.

Luciano Boglione
Naval Research Laboratory
General Chair

Vipul J. Patel
Department of the Air Force
Technical Program Chair

ABOUT GOMACTech

GOMACTech was established primarily to review developments in microcircuit applications for government systems. Established in 1968, the conference has focused on advances in systems being developed by the Department of Defense and other government agencies and has been used to announce major government microelectronics initiatives such as VHSIC and MIMIC, and to provide a forum for government reviews.

GOMACTech 2024 provides a forum for discussing and demonstrating advanced microelectronics and microsystems that can provide the means to develop confidence in transformational, leap-ahead technologies, and capabilities. GOMACTech is the premier forum for reporting on government-funded microcircuit research and other research efforts that focus on the technology needs of government systems.

REGISTRATION

All sessions at GOMACTech 2024 will be held at the Charleston Convention Center. Both check-in and on-site registration will take place in the Ballroom Foyer of the Convention Center.

Conference check-in and on-site registration hours:

March 17	Sunday:	4:30 PM – 6:30 PM
March 18	Monday:	7:00 AM – 6:00 PM
March 19	Tuesday:	7:00 AM – 5:00 PM
March 20	Wednesday:	7:45 AM – 5:00 PM
March 21	Thursday:	8:00 AM – 3:00 PM

Please: No photography or video in sessions or exhibit hall.

SECURITY PROCEDURES

GOMACTech is an unclassified, export-controlled event that requires participants to be U.S. Citizens or legal U.S. Permanent Residents. All registrants, including presenters and exhibitors, must provide proof of U.S. Citizenship or Permanent Resident status prior to being permitted entry into the conference. Additionally, all attendees will be required to complete and sign non-disclosure agreements (NDAs) on site.

You may prove U.S. citizenship with any of the following:

- U.S. Passport
- Birth certificate AND valid government-issued photo ID
- Naturalization certificate AND valid government-issued photo ID
- Permanent resident card

The following cannot be used on their own as proof of citizenship:

- Voter registration card
- Driver’s license

GOMACTech 2024 WORKSHOPS

Trusted Supplier Industry Day

Monday, March 18
8:00 am – 5:00 pm
Ballroom A

The thirteenth Trusted Supplier Industry Day will be an interactive event with an opportunity for all attendees to hear from key leaders and provide input on the critical issues facing our community. We have seen tremendous change since last year's Industry Day. The CHIPS Program office has begun funding projects under the CHIPS and Science Act for the construction, expansion, or modernization of commercial facilities for the fabrication of leading-edge, current-generation, and mature-node semiconductors. DoD announced in August the eight Microelectronics Commons hubs that will form a national network to create direct pathways to commercialization for US microelectronics researchers and designers from "lab to fab," and in December announced the project areas in which hubs can propose projects to be funded. The Industry Day program will feature speakers who will address these areas and topics including evolving microelectronics strategies with a focus on security and integrity. Speakers will also address developments regarding the CHIPS Research and Development Office's National Semiconductor Technology Center as well as the National Advanced Packaging Manufacturing Program (NAPMP) Advanced Packaging Piloting Facility (APPF) where successful advanced packaging innovation development efforts will be evaluated and validated for scaled transition to U.S. manufacturing. The Industry Day is being designed to provoke thoughtful conversations and up-to-date information on the many activities being pursued to restore U.S. leadership in semiconductor manufacturing with a semiconductor supply chain that considers security along with technical performance. Please join us on March 18th to add your voice to the discussion of the most critical electronics issues of the day.

Microelectronics Assurance Workshop

Monday, March 18
8:30 am – 5:00 pm
Ballroom B

Microelectronics Assurance is one of the key technical execution areas (TEA) under the OUSD(R&E) Trusted & Assured Microelectronics (T&AM) program. The Microelectronics Assurance TEA (MAT) meets the needs of key stakeholders to ensure the confidentiality and integrity of microelectronic components used in DoD systems by providing hardware assurance and vulnerability assessments; FPGA supply chain lifecycle assurance; microelectronics supply chain risk and threat assessments; and the development of best practices guidance, assessment tools, technologies, techniques, and mitigations. MAT leverages the expertise and services provided by the Joint Federated Assurance Center (JFAC) Hardware Assurance Labs to meet the goals and objectives of MAT.

On-shore Advanced Packaging Capabilities

Monday, March 18
1:00 – 4:30 pm
Ballroom C4

The government Reshore Ecosystem for Secure Heterogeneous Advanced Packaged Electronics (RESHAPE) and Defense Production Act Investment (DPAI) teams will present overviews of currently funded on-shore advanced packaging capabilities. Program overviews, interactive discussions, and presentations from vendors on their advanced packaging manufacturing capabili-

ties will provide an opportunity for attendees to hear from key stakeholders and provide input on the critical issues facing the advanced packaging community. Awards have been made through the Industrial Base Analysis and Sustainment (IBAS) program, RESHAPE effort, to Osceola County Fl/Skywater/BRIDG and Micross Components. The DPAI program has awarded Calument and GreenSource Fabrication LLC. Speakers will address key needs and developments in packaging to include Fan-Out Wafer Level Packaging (FOWLP), Wafer Prep and High-Density Interconnent/High Density Build-up (HDI/HDBU). Please join us on the afternoon of March 18th to hear the latest in government packaging capability investments and be part of the needs and challenges discussions for this advanced packaging community.

GOMACTech 2024
PANEL DISCUSSIONS

DoD Workforce Development Accomplishments and Future Directions

Wednesday, March 20
10:30 am – 12:10 pm
Room 10/11 (second floor)

There is a big push on workforce development (WFD) in the CHIPS Act to address the gaps identified by the various trade organizations. USG and DoD programs are unable to meet staffing goals for domestic, clearable microelectronics engineers. The Scalable Asymmetric Lifecycle Engagement (SCALE) program continues to assess and aggregate the stakeholders' needs and provide data-driven microelectronics workforce recommendations. The DoD focus areas cover radiation-hardening, heterogeneous integration/advanced packaging, system on a chip, embedded system security/trusted AI, supply chain awareness, and others. The panel will discuss who is responsible for WFD, possible standards, and how the progress is measured. It will look at different groups as post-secondary, kindergarten-12, and others. There is need to grow the research work force to use the key microelectronic investments.

STEM the "Leaky Pipeline" I

Wednesday, March 20
1:30 – 3:10 pm
Room 10/11 (second floor)

Studies show that women and underserved populations leave the STEM workforce at significantly higher rates, which is of particular concern as USG and DoD programs are unable to meet staffing goals for domestic, clearable microelectronics engineers. Human resources initiatives alone have not been able to STEM the "leaky pipeline". It is time to take the problems to the engineers. Peers, technical leads, and managers have a greater impact on the daily experience of the individual engineer than yearly company mandated trainings. The engineering community must own this problem and find the solution. This panel features conversation between members from government, academia, and industry to explore hidden barriers to employee growth and retention while seeking actionable quantifiable solutions. Panelists will share experiences with programs aimed at career development for underserved populations. The panel will identify strategies for enhancing systems for items such as program technical effort, performance evaluations and work allocation, as well as quantitative methods used to evaluate initiatives aimed at improving workforce equity.

Leveraging Startup Innovation within the DoD Microelectronics Community

Wednesday, March 20
3:30 – 5:10 pm
Room 10/11 (second floor)

Small companies that are new to working with the USG often do not have the resources to effectively share their perspectives with government decision-makers and struggle to identify relevant funding opportunities within active research and development (R&D) initiatives. Such companies play a critical role in driving rapid innovation and fueling economic growth. As the microelectronics ecosystem has become more complex, closer collaborations between all stakeholders are critical to maintaining access to the best technology in the industry. The panel will focus on domestic startups and emerging small- and mid-size microelectronics companies with discussion surrounding how such companies can more actively participate within major government-funded R&D initiatives, such as the CHIPS Act. The panel will provide perspectives from small commercial companies and USG government stakeholders, and discuss challenges they face, how they can impact the community, and how to better leverage such companies for USG microelectronics needs and to bolster domestic capabilities.

STEM the "Leaky Pipeline" II

Thursday, March 21
8:30 am – 10:10 am
Room 10/11 (second floor)

Join us Thursday morning as we offer a recap of the Wednesday panel in which we discussed concrete ideas to grow and retain women and underserved populations in the defense microelectronics workforce. Make connections and share ideas for next steps, including coordination with workforce development initiatives and quarterly working groups. It's time to make progress in our workplaces and our industry.

The T&AM MPW Program Panel Discussion

Thursday, March 21
10:30 am – 12:10 pm
Room 10/11 (second floor)

The Trusted and Assured Microelectronics (T&AM) Program within OUSD Research and Engineering (R&E) aims to provide the U.S. warfighter with the state-of-the-art (SOTA), assured microelectronics required to meet DoD system modernization goals. One of the primary objectives of the program is to enable access to commercial industry and government to develop and demonstrate SOTA designs that advance DoD initiatives. T&AM sponsors multi-project wafer (MPW) run opportunities to enable access to SOTA US commercial foundries ≤22 nm in support of the DoD microelectronics goals and to aid in developing specific foundation and functional intellectual properties. Currently, T&AM sponsors MPW opportunities with GlobalFoundries and Intel Foundry Services. The program is available to relevant designs from the defense industrial base (DIB), government laboratories, and academia. The panel will provide an overview of T&AM MPW opportunities and a discussion of technologies currently sponsored.

LUNCHES

Lunches will be provided in the Exhibit Hall Tuesday through Thursday.

TRUSTED SUPPLIER OPENING NETWORKING RECEPTION

Sunday March 17
6:00 – 8:00 pm
Ballroom Foyer

We are pleased to hold a special get-together with the Trusted Supplier Industry Networking Reception on Sunday evening. Please join us for some food and drinks, meet your industry friends and colleagues, and relax before Monday's full agenda begins.

All GOMACTech 2024 registrants are invited to the Sunday evening reception.

WELCOME RECEPTION

Monday March 18
5:00 – 7:00 pm
Ballroom Foyer

All registered attendees are encouraged to join us for an opening reception.

WEDNESDAY EVENING SOCIAL

Offsite Evening at the South Carolina Aquarium
6:30 – 10:30 pm
Wednesday, March 20

Please join us for an evening of delight at the world-renowned South Carolina Aquarium. Enjoy drinks and dinner at sunset on the historic Charleston Harbor. Guests will experience many aquarium exhibits including the stingray touch tanks. Transportation will be provided to and from the aquarium beginning at 5:30 pm and ending at 10:30 pm. Tickets are $75 per person and space is limited. Tickets must be purchased at registration prior to the event.

https://scaquarium.org/

EXHIBITION

An exhibition made up of commercial vendors exhibiting products of interest to the GOMACTech community is an integral part of the conference. All attendees are encouraged to visit the exhibition when they have some free time. The exhibition will be located in the Golden State Ballroom. Coffee breaks will be held in the exhibit area when they coincide with the exhibition's hours of operation. On Tuesday evening, March 19, an Exhibitors' Reception, where attendees can mix in a relaxing atmosphere with food and good spirits, will be held from 6:00 – 8:00 pm.

Exhibition hours are as follows:

Tuesday, March 19 – 12:00 pm – 8:00 pm
Wednesday, March 20 – 9:00 am – 4:00 pm

List of Exhibitors
3D Glass Solutions, Inc.
AARD Technology LLC
AdTech Ceramics
AEM-Central Semiconductor-Renaissance.
Akoustis, Inc.
Alphacore, Inc.

AmTECH Microelectronics
Analog Devices
Andes Technology Corp.
Ansys
Astronics Test Systems
Avalanche Technology
BAE Systems
Battelle
The Boeing Company
BRIDG
Cadence
CAST
Certus Semiconductor
Checkpoint Technologies
Chip Scan
Codasip
CoolCAD Electronics
Cycuity
Defense Technical Information Center
DeUVe Photonics
DMEA TAPO
EndoSec LLC
ENGIN-IC, Inc.
Evatec NA
Extreme Waves
Falcomm
Ferric, Inc.
Finetech
Flex Logix, Inc.
Frontgrade
GlobalFoundries
Graf Research Corp.
Honeywell
HRL Laboratories LLC
IBM
Idaho Scientific
IEEE Computer Society
Indiana Integrated Circuits LLC
Infineon Technologies
Instec, Inc.
Integra Technologies, Inc.
Intel Corp.
Intel Foundry Services
Intrinsic ID
IPC International, Inc.
ISI
JEOL USA, Inc.
JST Manufacturing
JSTF – Jazz Semiconductor Trusted Foundry
Kansas City National Security Campus
KEYENCE Corp. of America
Keysight Technologies
Knowles Precision Devices
Laser Thermal Analysis
LOCH Technologies
MACOM
Marvell Government Solutions
Menta eFPGA, Inc.
Mercury Systems
Metamagnetics
Microchip Technology, Inc.
Micropac
Microsanj
Microsoft
Micross Components
Midwest Microelectronics Consortium
Mirabilis Design, Inc.

MIT Lincoln Laboratory
MITRE
Mosaic Microsystems
MOSIS 2.0 | California DREAMS | USC/ISI
Nalu Scientific
Nano OPS, Inc.
National Security Agency
Nimbis Services, Inc.
Noble Metal Services
Nokomis, Inc.
Northrop Grumman
NSWC Crane
NTek-Litho
Omni Design Technologies
onsemi
PacTech USA, Inc.
Palomar Technologies
Penn State Applied Research Laboratory – Electronics Manufacturing Center
Perforce Software
Photronics, Inc.
Plasma-Therm
Precision Circuit Technologies
proteanTecs
QML, Inc.
QP Technologies
QuickLogic Corp.
Raith America, Inc.
Rambus
Raytheon
Real Intent
Red Balloon Security
Riscure, Inc.
S2MARTS
S-Cubed
Secure-IC
SecureFoundry
Siemens
SiFive
Signature IP Corp.
Silicon Assurance
Silitronics Solutions, Inc.
Silvaco, Inc.
SkyWater Technology
Spectral Design and Test, Inc.
Spirit Electronics
SRI International
Synopsys
Tektronix Component Solutions
Tenet3
Tenstorrent
Toppan Photomasks Round Rock, Inc.
Trusted Semiconductor Solutions, Inc.
Trymax USA
University of Arizona, Center for Semiconductor Manufacturing
Vistec Electron Beam
XTREME Semiconductor
Yield Engineering Systems, Inc.

GOMACTECH 2023 PAPER AWARDS

Paper awards based on audience evaluations from GOMACTech 2023 will include the George Abraham Outstanding Paper Award, a Best Poster Paper Award, and a Best Student Poster Paper Award. Presentation of these well-deserved awards will take place during the Plenary Session on Tuesday morning in Ballroom A-B. The GOMACTech-2023 winners are as follows:

The George Abraham Outstanding Paper Award (35-2)

"Polarization Induced Two-Dimensional Electron-Gas (2DEG) and Hole-Gas (2DHG) in Grafted AlN/GaN Heterostructures"

Seunghwan Min[1], Ranveer Singh[1], Ping Wang[2], Ding Wang[2], Jiarui Gong[3], Haris Naeem Abbasi[1], Jie Zhou[1], Daniel Vincent[1], Moheb Sheikhi[1], Neil Campbell[3], Jingcheng Zhu[3], Yang Liu[1], Timothy Grotjohn[4], Mark Rzchowski[3], Zetian Mi[2], and Zhenqiang Ma[1]

[1]Department of Electrical and Computer Engineering, University of Wisconsin-Madison

[2]Department of Electrical Engineering and Computer Science, University of Michigan

[3]Department of Physics, University of Wisconsin-Madison

[4]Department of Electrical and Computer Engineering, Michigan State University

Best Poster Paper Award (P-75)

"Neutron Radiation In-situ Failure-in-time Characterization of 1200V-1700V SiC Power Transistors"

Moinuddin Ahmed[1], Christopher Stankus[1], John Hryn[1], Stephen Arthur Wender[2], Kranti Gunthoti[2]

[1]Applied Materials Division, Argonne National Laboratory

[2]Los Alamos Neutron Science Center, Los Alamos National Laboratory

The Les Palukti Best Student Poster Paper Award (P-66)

"A Near-Memory Accelerator for Real-Time Emulation of RF Interactions"

Mandovi Mukherjee*, Nael Mizanur Rahman*, Sudarshan Sharma, Uday Kamal, Xiangyu Mao, Payman Behnam, Daehyun Kim, Jianming Tong, Jongseok Woo, Prachi Sinha, Coleman DeLude, Joseph Driscoll, Jamin Seo, Santosh Pande, Tushar Krishna, Justin Romberg, Madhavan Swaminathan, Saibal Mukhopadhyay

School of Electrical and Computer Engineering, Georgia Institute of Technology

*Joint First Authors

SURVEY AND GIFT

We are asking all our attendees to complete a short online survey so we can learn how to improve our conference next year. The survey is available through a link in the mobile app and will also be posted on signs at the conference. When you have finished taking the survey, make a screenshot of your confirmation/thank-you notice and bring it or your confirmation email to the registration desk to receive a gift as our thank-you for completing the survey. (Note: Paper versions of the survey are also available at registration on request. If you are filling out a paper survey, please do not fill out an online version and vice versa.)

USB DIGEST

The GOMACTech USB Digest contains searchable versions of accepted papers for the conference. Previous GOMAC Digests are available to qualified Defense Technical Information Center (DTIC) users.

PARTICIPATING GOVERNMENT ORGANIZATIONS

Participating Government Organizations of GOMACTech 2024 include: CHIPS Program Office, Defense Advanced Research Projects Agency, Defense Logistics Agency, Defense Microelectronics Activity, Defense Threat Reduction Agency, Department of Defense Agencies, Department of Homeland Security, Department of the Air Force, Department of the Army, Department of the Navy, Intelligence Advanced Research Projects Agency, National Aeronautics and Space Administration, National Institute of Standards and Technology, National Nuclear Security Administration, National Reconnaissance Office, National Security Agency

GOMACTech WEB SITE

Information on GOMACTech may be obtained through its web site at www.gomactech.net.

MEETING SPACE AVAILABILITY

A limited amount of private meeting space is still available for rent at GOMACTech 2024. For more information, visit the registration desk and/or contact Danielle Rocco at 646-226-7592 or drocco@pcm411.com.

CONFERENCE ASSISTANCE

Anyone requiring assistance at GOMACTech 2024 should contact the conference coordinators at the registration desk or as below:

Mari Ramirez and Ronnie Stephenson
GOMACTech
411 Lafayette Street, Suite 201
New York, NY 10003
212/460-8090
mramirez@pcm411.com and rstephenson@pcm411.com

TUESDAY, MARCH 19

(All Eastern Daylight Time)

PLENARY SESSION

Tuesday, March 19 / Ballroom A-B

Continental Breakfast **(7:00–7:45)**

Color Guard and National Anthem **(8:00–8:15)**

Opening Remarks and Awards **(8:15–8:45)**

Luciano Boglione
GOMACTech 2024 General Chair

Vipul J. Patel
GOMACTech 2024 Technical Program Chair

Keynote Address I **(8:45–9:30)**

Dr. Jay Lewis

Director of the National Semiconductor Technology Center (NSTC) Program

CHIPS R&D Office at the Department of Commerce

"A Vision for Innovation Through Collaboration in the National Semiconductor Technology Center (NSTC)"

This address discusses a variety of challenges in the microelectronics ecosystem, and how NSTC can unite the community to address those challenges. Some of these are technical – logic, mixed signal, memory, photonics, design/co-design, and architecture all need new breakthroughs to continue to advance the state of technology. Others are ecosystem challenges. Access to design tools, IP, and collaboration environments, as well as increasing use of AI in design and verification flow will all transform the way that the industry does its work. Access to advanced R&D facilities and leading-edge shuttles can accelerate the pace of research. The traditional venture model has been mismatched with hardware investments for decades, and this has been a drag on innovation, but there are new ideas for how this can work better. In closing, we will provide updates on the priorities for this year, and show how the NSTC can change the long-term trajectory for innovation.

Keynote Address II **(9:30–10:15)**

Mr. Maynard Holliday

Assistant Secretary of Defense for Critical Technologies

Office of the Under Secretary of Defense for Research and Engineering

"DoD Microelectronics Overview"

This keynote will emphasize and remind the community of the importance of securing microelectronics that are crucial to multiple critical infrastructure technologies, including those that directly impact our country's security and defense. Featured issues include key microelectronics initiatives championed by our federal government and within the Department of Defense (DoD) to illustrate a whole-of-government approach. The presentation will include highlights of the speaker's critical technology portfolio as well as some of the challenges DoD faces while seeking collaborations with industry.

BREAK **(10:15–10:30)**

Keynote Address III (10:30–11:15)

Dr. Tina Kaarsberg

Acting Program Manager

Advanced Materials and Manufacturing Technologies Office (AMMTO)

U.S. Department of Energy (DOE)

"Microelectronics Energy Efficiency and Power Electronics for Zero Carbon"

This brief overview of micro- and power electronics research at the US Department of Energy will also describe how AMMTO intends to lead DOE's power electronics efforts to achieve net zero carbon with a P.E. Roadmap that enables accelerated deployment of clean energy technologies, the net zero carbon grid, and electrified transportation and industry. Additional focus includes the "Microelectronics Energy Efficiency Scaling for 2 Decades" (EES2) initiative. The goal of this talk is to inspire the community about the EES2 and other microelectronics and power electronics work at the DOE and to provide information about how everyone can contribute.

Jack S. Kilby Lecture Series

Kilby Address I (11:15–11:45)

Dr. Tim Morgan

Acting Technical Director for Microelectronics Commons

"Microelectronics Commons: A National Network for Defense Microelectronics Innovation"

The Microelectronics Commons (Commons) is a key national initiative that is executed with oversight from the Office of the Under Secretary of Defense for Research and Engineering's (OUSD(R&E)'s) Principal Director for Microelectronics as part of the CHIPS and Science Act. This effort benefits both the Department of Defense (DoD) and the United States in spurring development of a domestic microelectronics manufacturing industry by forging critical partnerships with commercial industry, academic, and government partners within eight regional hubs across the country. The Commons supports the acceleration of laboratory to fabrication (lab-to-fab) prototyping through hubs to create a network focused on maturing emerging microelectronics technologies, strengthening microelectronics education and training, and developing a pipeline of talent to bolster local semiconductor economies and contribute to the growth of a domestic semiconductor workforce. In particular, the Commons will address the need for processes, materials, devices, and architectures to be developed and transitioned from research labs to small-volume prototyping in a fab or foundry. The Microelectronics Commons released the first annual Call for Projects (CFP) in December 2023 and released 41 topics across six technical areas: Electronic Warfare, Commercial Leap Ahead, AI Hardware, Quantum, Secure Edge/Internet of Things and 5G/6G. This talk will provide an update on the progress in spurring advances..

Kilby Address II (11:45–12:15)

Dr. Subramanian Iyer

Director

National Advanced Packaging Manufacturing Program

(on assignment from UCLA)

"Packaging: Then, Now and in the Future"

In 2014, Dr. Iyer gave a Kilby Lecture at this conference where he outlined at a very exploratory level the promise of packaging to move Moore's law from a "scale the chip play "to a "scale the system play". Ten years later, things have certainly taken off and those rudimentary concepts that he discussed, such as finer package pitches, simpler communication protocols, three-dimensional stacking, and chiplet concepts have made a significant impact in our ability to build both high-performance and low-power systems that are the very foundation of our incredible current AI/ML and telecommunication capabilities. However, we have barely scratched the surface as far as the incredible potential of advanced packaging. This talk will offer a roadmap for advanced packaging (that was funded by NIST) and a strategic

vision of how the NAPMP will implement this roadmap in a manner that allows for the introduction of on-shore manufacturing of advanced packaging and true heterogeneous integration, in not just the high-performance and low-power arenas, but also in the all-important application of medical electronics.

LUNCH **(12:30–1:30)**
Exhibit Hall

Session 1 **(Packaging, Integration, Thermal and Control Technologies)**

ADVANCES IN MULTI-CHIP INTEGRATION

Tuesday, March 19 / 1:30 – 3:10 pm / Ballroom A

Chair: **Daniel Radack**
Institute for Defense Analyses, Alexandria, VA

Co-Chair: **Vashisht Sharma**
Institute for Defense Analyses, Alexandria, VA

1.1: Technical Challenges and Solutions for an Industry Scale Reuse in the Chiplet Era (1:30)

Salem Abdennadher
Intel, Laguna Beach, CA

Tao Zhou
Intel, San Diego, CA

Reuse from internal, customer, and third-party sources within and between products and generations is an important lever propelling Chiplet benefits such as reducing portfolio product and project costs, helping scale innovation and delivery capabilities, and improving time to solution. This paper addresses the technical challenges and solutions for an Industry Scale Reuse in the Chiplet Era.

1.2: Virtual Prototyping for Early Architecture Design Optimization of Multi-Die Systems (1:50)

Tim Kogel, Holger Keding, Kamal Desai, Frank Malloy
Synopsys, Inc., Sunnyvale, CA

2.5D, 3D, and 3DHI multi-die systems have emerged in response to the economic and technological challenges that are threatening the efficacy of Moore's law. Importantly, multi-die systems facilitate the creation of variants that can be designed to enable a portfolio of low cost, flexible custom or semi-custom solutions. There are a host of considerations for these multi-variant multi-die systems, including the different ways to realize the interfaces to the choices of protocols, system pathfinding for die and chiplet placement, optimal memory utilization and coherency, and power and thermal management. This paper discusses current state of the art, architectural challenges, and the direction of our project to use virtual prototypes for early quantitative architecture analysis. We will present a case study. This project aims to enable system architects to navigate complex design spaces and to shorten the time to market of multi-variant multi-die systems.

1.3: TruPack Secure System in Package: When Size and Security Matter (2:10)

Jonathan Lovseth, John Bendickson, Nathan Van Schaick
Collins Aerospace, An RTX Business, Cedar Rapids, IA

1.4: Die-to-Die Connectivity IP Solutions: Enabling the Path to the Future of Chiplet Ecosystem (2:30)

Salem Abdennadher
Intel, Laguna Beach, CA

Issy Kipnis
Intel, Santa Clara, CA

Tao Zhou
Intel, San Diego, CA

Integrating multiple chiplets in a package to deliver product innovation across market segments is the future of the semiconductor industry and a pillar of Intel's IDM 2.0 strategy. A chip industry group, announced the Universal Chiplet Interconnect Express (UCIe) to increase innovation to foster an open ecosystem. Though, since 2017 Intel has been building its own chiplet ecosystem with its FPGAs using Advanced Interface Bus (AIB), proliferating its portfolio of FPGAs. Intel continues to develop products using the current AIB specification, new products will use today's AIB interface, along with several being developed in concert with the US Government (USG) State-of-the-Art Heterogeneous Integration Prototype (SHIP) program. There are many inquiries and concerns from USG whether these chiplets can be reused as industry is moving to UCIe. To enable AIB-based chiplets to join and contribute value to the UCIe chiplet ecosystem, we identified viable options for transition from AIB to UCIe.

1.5: Advanced Packaging Substrates – Silicon and Glass Cores (2:50)

Vineeth Harish, Subramanian S. Iyer
UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS), Los Angeles, CA

Venky Sundaram
3D System Scaling LLC, Johns Creek, GA

This paper delves into the transformative trends and innovations reshaping PCBs and advanced IC substrates, and how the United States can build a supply chain resilience with both innovative and existing materials to usher in a new era of integrated electronic systems.

BREAK (3:10–3:30)
Ballroom Foyer

RADIATION HARDENED CHARACTERIZATION MECHANISMS

Tuesday, March 19 / 1:30 – 3:10 pm / Ballroom B

Chair: **Pauline Paki**
DHS Science and Technology, Washington, DC

Co-Chair: **Megan Casey**
NASA Goddard Space Flight Center, Greenbelt, MD

2.1: Investigation into Alternative Radiation Hardened Photovoltaic Materials for Planetary Missions (1:30)

Cole Lush, Ishaan Rao, Sayam Roy, Peter Bermel
Purdue University, West Lafayette, IN

Photovoltaic (PV) cells provide power for many satellite applications, but can substantially degrade in space radiation environments. In order to mitigate the cost of implementing and launching shielding that might be needed for conventional photovoltaic materials, this study seeks to identity lightweight, inherently radiation-hardened alternatives. Initial candidates are identified through software simulations modelling the nonionizing energy loss (NIEL) of different materials and by translating NIEL into tangible, physical damage mechanisms.

2.2: In-situ Single Event Effect Characterization of 650 V–1700 V Wide Bandgap Power Transistors under Neutron Irradiation (1:50)

Moinuddin Ahmed, Christopher Stankus, John Hryn
Argonne National Laboratory, Lemont, IL

Stephen Arthur Wender, Kranti Gunthoti
Los Alamos National Laboratory, Los Alamos, NM

This work is focused on the in-situ single event effect (Failure-in-time) characterization of wideband gap (WBG) SiC and GaN power transistors due to terrestrial neutron radiation. Wide bandgap SiC and GaN power transistors are attractive candidates for aerospace and satellite communication which offer smaller footprint, lower weight, higher-temperature operation, lower power losses, and higher operating frequency. We have tested 650 V–900 V GaN and 1200 V–1700 V power transistors in this work. The devices were in-situ tested for failure-in-time (FIT) analysis method at Los Alamos Neutron Science Center (LANSCE) in the ICE House-1 facility at a flux of 10^6 n/cm^2-s above 1.5 MeV energy. The devices were tested at room temperature (25 C) and an elevated temperature of 150 C. The corresponding failure-in-time parameters have been calculated, and the dependence of failure-in-time with voltage and temperature has been demonstrated.

2.3: In-Situ Measurement of 1.8 MeV Proton Radiation Effects on Comb-Drive MEMS Resonators (2:10)

Jaesung Lee
University of Florida, Gainesville, FL
and
University of Central Florida, Orlando, FL

Michael W. McCurdy, Robert A. Reed,
Ronald D. Schrimpf, Michael L. Alles
Vanderbilt University, Nashville, TN

Philip X.-L. Feng
University of Florida, Gainesville, FL

We report on the first in-situ measurement of proton radiation effects on silicon comb-drive microelectromechanical resonators. The specially designed comb-drive resonators can be operated both in linear and contact impacting (i.e., 'tapping') modes which are versatile and can be used for resonant sensing and switching applications. In-situ, continuous monitoring of radiation effects induced by impinging 1.8 MeV protons with controlled dosage, in both linear and tapping modes of the resonators, have been performed. The devices exhibit highly sensitive responses while maintaining robust operations. Upon radiation flux of $9.15 \times 10^8/cm^2/s$, both temporal and permanent radiation effects (i.e., frequency shift) on the comb-drive MEMS resonators have been clearly resolved. These in-situ observations of radiation effects on the comb-drive devices show that MEMS resonators can be a promising platform for making new radiation sensors and radiation-hard information processing components.

2.4: Radiation-hard Low-loss β-Ga_2O_3 High-Power Diodes (2:30)

Esmat Farzana
Iowa State University, Ames, IA

Nolan S. Hendricks, James S. Speck
University of California Santa Barbara, Santa Barbara, CA

Sajal Islam, Aditha S. Senarath, Rick M. Cadena,
Dennis R. Ball, Arijit Sengupta, Daniel M. Fleetwood,
Ronald D. Schrimpf
Vanderbilt University, Nashville, TN

Enxia Zhang
University of Central Florida, Orlando, FL

We report here vertical β-Ga_2O_3 diode combining Schottky barrier and field-plate engineering that enabled high breakdown voltage and low-loss devices. A composite Schottky contact, PtO_x/Pt/β-Ga_2O_3, was formed that achieved both enhanced reverse blocking by PtO_x and low turn-on voltage by Pt, leading to less power dissipation than PtO_x/β-Ga_2O_3 diodes at all duty cycles. The high permittivity (κ) dielectric (ZrO_2) field-plate further increased the breakdown voltage of the PtO_x/Pt/β-Ga_2O_3 diodes to ~2.34 kV. Moreover, the PtO_x contact and high-κ field-plate also increased single-event burnout (SEB) resistance against heavy ion and Cf-252 exposure, revealing a promising way to develop radiation-hard β-Ga_2O_3 devices.

2.5: Tungsten and Hexagonal-Boron Nitride Hybrid Shielding for Space Radiation Sources (2:50)

Elliot Wong, Sayan Roy, Stylianos Chatzidakis, Aaron Fernandes, Andres Gomez, Allen Garner, Peter Bermel
Purdue University, West Lafayette, IN

With growing interest in satellite applications, ensuring the reliability of microelectronics in space is paramount. Spacecraft face the constant threat of system failure caused by charged particles. However, constraints in mass and space impose limitations on shielding solutions. To address this, we employ a Monte Carlo simulation tool to assess the shielding effectiveness of various materials. Initial investigations reveal protons as the primary radiation source in space. We evaluate materials systematically based on ion distribution, ionization, energy to recoils, and collision events to safeguard microelectronics. Recent simulations highlight hexagonal-boron nitride as a superior low Z material for efficient energy blocking with reduced weight. This model data will be cross-referenced with experimental results, and further experiments are planned to reconcile any disparities. Additionally, a 3D Monte Carlo simulation tool will validate the significance of alternating shielding layers.

BREAK **(3:10–3:30)**
Ballroom Foyer

ADVANCED GAN TECHNOLOGIES AND APPLICATIONS

Tuesday, March 19 / 1:30 – 3:10 pm / Ballroom C4

Chair: **David Meyer**
Naval Research Laboratory, Washington, DC

Co-Chair: **Gregg Jessen**
MACOM Technology Solutions, Lowell, MA

3.1: An X-band GaN MMIC for Self-Interference Cancellation in Full-Duplex Phased Array (1:30)

Seth Johannes, Zoya Popovic
University of Colorado, Boulder, CO

Kenneth E. Kolodziej
Massachusetts Institute of Technology, Lexington, MA

In this paper, we present a front-end MMIC that samples the transmit signal for aperture-level in-band full-duplex phased arrays with digital self-interference cancellation. The circuit is a linear low-noise amplifier co-designed with a variable attenuator and switching network for transmit and receive operation. When the array element is in transmit mode, the MMIC couples a portion of the transmitted signal through the capacitance of an “off” switch, and the signal is then fed through a variable attenuator, downconverted and sampled as an observation signal for digital SIC. The MMIC is implemented in a 150-nm GaN on SiC process for operation from 8–12 GHz. In transmit mode, the switch insertion loss is less than 1 dB, return loss greater then 10 dB, and the sampled transmit signal has a range of 25 dB to 40 dB. Co-designed LNA using complex-to-complex impedance matching has a gain greater than 12.4 dB and a NF below 2.6 dB

3.2: 2 to 18 GHz High Efficiency Power Amplifier (1:50)

Steve Nelson, Dumitru Grecu, Danny Bryant, Rajah Vysyaraju, Chris Ison, Rajesh Mongia, Howard Sheehan
ENGIN-IC, Inc., Plano, TX

3.3: PA and Supply Modulator GaN MMICs for Efficient High-PAR Signals in the 8–14 GHz Band (2:10)

Stefan Stroessner, Connor Nogales, Zoya Popović
University of Colorado Boulder, Boulder, CO

Paul Flaten
NSWC Crane, Crane, IN

3.4: Millimeter-Wave Watt-Level Stacked PA Design in HRL’s T3 and T3.5 40-nm GaN HEMT Processes (2:30)

Clint Sweeney, Donald Y.C. Lie, Jill Mayeda
Texas Tech University, Lubbock, TX

Jerry Lopez
NoiseFigure Research Inc., Lubbock, TX
and
Texas Tech University, Lubbock, TX

3.5: 40–107 GHz GaN Active Circulator MMIC with Cascode Amplifiers **(2:50)**

Anthony Romano, Timothy Sonnenberg, Zoya Popović
University of Colorado Boulder, Boulder, CO

Nicholas Miller
Michigan State University, East Lansing, MI

This paper presents an active circulator designed to operate from 40–107 GHz implemented in a 40 nm HEMT GaN MMIC process. Three amplifiers are connected with Lange couplers in a ring architecture. The cascode amplifiers use two 4 × 25 μm HEMTs, with a simulated small signal gain of 5 dB at 70 GHz designed to be well matched over the octave frequency range. The circulator is stable and demonstrates 29 dB of isolation and –6.4 dB of insertion loss at 70 GHz in full-duplex mode with all amplifiers biased on. The isolation with only one amplifier biased on is referred to as half-duplex, and shows similar isolation over a broader bandwidth. The measured gain compression agrees well with simulations and demonstrates good linearity up to the available 9 dBm input power at 101 GHz. The presented circuit can be bias-switched between full and half-duplex operation.

BREAK **(3:10–3:30)**
Ballroom Foyer

NONTRADITIONAL APPROACHES TO TRUST

Tuesday, March 19 / 1:30 – 3:10 pm / Ballroom C1-3

Chair: **Joel Goodman**
Naval Research Laboratory, Washington, DC

Co-Chair: **Robert Freeman**
Synopsys, Inc., Sunnyvale, CA

4.1: LLM4Sec: Embracing Large Language Model for System-on-Chip Security (1:30)

Dipayan Saha, Katayoon Yahyaei, Sujan Kumar Saha, Farimah Farahmandi
University of Florida, Gainesville, FL

The widespread use of System-on-Chip (SoC) in modern electronic devices has highlighted the challenges of incorporating security. Existing SoC security analysis methods and secure design approaches have limitations in scalability, adaptability, and coverage, suggesting a need for better security approaches. Concurrently, the rise of Large Language Models (LLMs) is marking a transformative era of applications. Given the complexity and diversity of SoC security issues, the proven capabilities of LLMs, and the promise of integrating LLMs into the SoC security paradigm, we propose LLM4Sec, an LLM-integrated SoC security framework. This framework shows how LLM, specifically GPT-3.5, can be adeptly used for SoC security tasks, including vulnerability insertion, detection, threat recognition, and mitigation, with the help of in-context learning and effective prompting techniques. Our experimental findings indicate that the framework is capable of performing these complicated SoC security tasks, achieving notable accuracy through natural language descriptions.

4.2: From AI to Cryptography: Masking Floating-Point Multiplication Hardware for Side-Channel Attacks (1:50)

Emre Karabulut
MithrilAI Corp., Raleigh, NC

Aydin Aysu
North Carolina State University, Raleigh, NC

4.3: Pre-Silicon Vulnerability Assessment for AI/ML Hardware (2:10)

Furkan Aydin, Emre Karabulut, Aydin Aysu
North Carolina State University, Raleigh, NC

Machine learning (ML) and artificial intelligence (AI) applications have become crucial for current and future information systems. Meanwhile, hardware security threats are emerging for AI/ML applications, such as the possibility of private input/model leakage as a result of hardware side-channel leakage. Yet such vulnerabilities are only evaluated after deployment and as ad-hoc instances, which is too late and too costly. The development of a framework is necessary in order to evaluate attacks and defenses comprehensively, quickly, and accurately prior to their deployment. In our research, we have developed the first hardware security simulation framework capable of identifying and quantifying side-channel leaks caused by instructions and processor stages and analyzing potential defenses in ML applications. As a case study, we have performed security evaluation of a RISC-V based FPGA implementation of an ML application at an early design stage and compared its leakage on real hardware.

4.4: Non-Destructive Evaluation of Repackaged Counterfeit FPGAs via Machine Learning (2:30)

Whitney Batchelor, James Koiner, Cody Crofford, Kevin Paar, Margaret Winslow, Mia Taylor, Scott Harper
Graf Research Corporation, Blacksburg, VA

With ongoing microelectronic supply chain issues, the demand for genuine field-programmable gate arrays (FPGAs) is increasing — but so is the occurrence of counterfeit devices. Frequently, devices are used, salvaged from old systems, and repackaged as new. Graf Research Corporation has developed a methodology for using telemetry bitstreams to characterize an FPGA device and subsequently classify whether a device is a repackaged counterfeit via statistical and machine learning models. The new method utilizes minimal external equipment, is non-destructive, and can be employed at any point throughout the supply chain.

4.5: Continuous Time Convolution Based Trust Verification for Wireless Microelectronics (2:50)

Mohammad Monjur, Qiaoyan Yu
University of New Hampshire, Durham, NH

In heterogeneous wireless network environments, distinct security vulnerabilities in hardware emerge as a big concern. Wireless mesh networks, in particular, are susceptible to various cyber-physical threats, such as jamming and relay attacks. To keep up with the evolution of attack methodologies, it is imperative to develop advanced security modules to simultaneously mitigate multiple attacks. To save the overhead cost, this work investigates a multi-dimensional detection approach at the hardware tier to detect multiple attacks with one detection scheme. A Continuous Time Convolution (CTC) method is proposed to detect numerous attack scenarios at low overhead costs for mesh network setups. Experimental results show that the proposed CTC achieves 100% detection rate for jamming attacks and 90% detection rate for replay attacks. Our proposed detection scheme stands out for its accuracy and seamless integration with LoRa's inherent characteristics, ensuring robust and power-efficient protection against malicious threats.

BREAK (3:10–3:30)
Ballroom Foyer

LASERS FOR UNIVERSAL MICROSCALE OPTICAL SYSTEMS (LUMOS)

Tuesday, March 19 / 1:30 – 3:10 pm / Room 6/7

Chair: **Anna Tauke-Pedretti**
DARPA MTO, Arlington, VA

Co-Chair: **Chelsea Haughn**
Booz Allen Hamilton, Washington, DC

5.1: Hetero-Epitaxial Quantum Dot Laser Integration On Silicon (HELIOS) (1:30)

G. Leake, J. Herman, N. Fahrenkopf, I. Ok, D. Harame
AIM Photonics / Research Foundation SUNY, Albany, NY

K. Feng, C. Shang, R. Korsica, B. Shi, J. Klamkin, J. Bowers
University of California Santa Barbara, Santa Barbara, CA

M. Watts, M. Zylstra, H. Yang, J. Wu, J. Jahn
Analog Photonics, Marina Park, Boston, MA

A. Clark, A. Liu
IQE, Inc., Greensboro, NC

Quantum-dot solid-state amplifiers (SOA) and lasers are integrated with silicon photonics by using hetero-epitaxy to grow the III-V quantum-dot gain region in pockets defined during the silicon photonics process integration flow. Fully functional lasers are demonstrated as well as coupling to silicon nitride waveguides. Compatibility with an AIM Photonics base MPW component library was also verified. This work demonstrates the feasibility of the HELIOS approach for developing a robust wafer-scale fabrication process for efficient on chip coupling of compact dense integrated light sources.

5.2: Foundry Photonics Process Platforms: An Overview – Enabling Si, III-V, Passives, Actives and Heterogeneous Integration for the PIC Revolution (1:50)

David Howard, Edward Preisler
Tower Semiconductor, Newport Beach, CA

Wafer foundry involvement in the “photonics revolution” is underway with many players engaged in delivering wafer processes (die) and services predicted to sum to almost $1B in 2027. Transceivers are the largest market, but other applications – sensors, lidar, and health – are growing. In this paper, we will review the foundry-available process families within Tower Semiconductor’s photonics offerings, some key metrics of select device features within those offerings, and demonstrations of performance. In addition, new features and roadmap items will be reviewed. We discuss the following processes. PH18M: baseline 200mm production silicon photonics (SiPho) feature rich processes. PH18D: heterogeneous integration of lasers with 200 mm SiPho (InP, GaAs). PN18: ultra-low-loss silicon-nitride waveguides (loss below 500 dB/km at 1550 nm). TPS45PHD: a newer 300 mm offering (Si WG 1 dB/cm loss at 1310 nm). And select roadmap items: DBR & DFB GaAs QD lasers (DARPA LUMOS), as well as LiNbO3 modulators and packaging features.

5.3: Photonics Integration with On-chip Sources from Visible to Infrared (2:10)

Chong Zhang, Minh Tran, Tin Komljenovic
Nexus Photonics, Goleta, CA

We present recent results in developing a heterogeneously integrated photonic platform with on-chip sources supporting operation from visible (400 nm) to IR (1700+ nm) using die-to-wafer bonding. The platform enables state-of-the-art performance, and wafer scale fabrication, testing and singulation for significant size, weight, power, and cost reduction of future systems.

5.4: High-coherence Visible Light on a Chip (2:30)

Kerry Vahala, Bohan Li
Caltech, Pasadena, CA

Jingwei Ling, Qiang Lin
University of Rochester, Rochester, NY

John Bowers
University of California, Santa Barbara, Santa Barbara, CA

Emission of high-coherence visible and near-visible lightwaves on-chip is demonstrated. The devices rely upon a new approach wherein wavelength conversion and coherence increase by self-injection locking are combined within a single nonlinear resonator. This simplified approach is demonstrated in hybridly-integrated devices using thin-film lithium niobate resonators (emission at 780 nm, 589 nm and 514 nm). The method is also demonstrated using the photogalvanic effect in ultra-lowloss silicon nitride resonators. Short-term linewidths as low as 25 Hz are realized at 780 nm by self-injection locking of a DFB laser at 1560 nm.

5.5: Nonlinear Nanophotonics for Visible-Emission Lasers (NOVEL) **(2:50)**

Scott Papp, Grant Brodnik, Alexa Carollo, Scott Diddams, Haixin Liu, Lindell Williams, Tsung-Han Wu
University of Colorado, Boulder, Boulder, CO

Jennifer Black, Ali Dorche, Lauren Kennedy, Richard Mirin, Nima Nader, Eric Stanton
NIST-Boulder, Boulder, CO, USA

David Carlson, Grisha Spektor
Octave Photonics LLC, Louisville, CO

Kartik Srinivasan, Xiyuan Lu, Gregory Moille, Edgar Perez, Jordan Stone
NIST-Gaithersburg, Gaithersburg, MD
and
University of Maryland, Gaithersburg, MD

Jelena Vuckovic, Amir Safavi-Naeini, Geun Ho Ahn, Oguz Tolga Celik, Melissa Guidry, Taewon Park, Hubert Stokowski, Alex White
Stanford University, Stanford, CA

Masoud Jafari, Tasneem Fatema, Andreas Beling
University of Virginia, Charlottesville, VA

Many laser applications require access to specific wavelength bands. For example, optical-atomic clocks provide a leap in performance for critical sensing and communication applications, but they demand compact lasers at wavelengths spread across the visible and near infrared. Integrated photonics enables high-performance, scalable laser platforms, however customizing laser gain to support wholly new bands is challenging and often prohibitively mismatched in scale to early quantum-based sensing and information systems. We describe the research project Nonlinear Nanophotonics for Visible-Emission Lasers (NOVEL) enabled by heterogeneous integration of nonlinear wavelength converters and a 980 nm pump laser. Our platform supports wavelength conversion from the visible to shortwave infrared with a common backbone of waveguide and resonator nonlinear devices.

BREAK **(3:10–3:30)**
Ballroom Foyer

MICROELECTRONICS PACKAGING TECHNOLOGIES

Tuesday, March 19 / 3:30 – 5:10 pm / Ballroom A

Chair: **Robert Harris**
Georgia Tech Research Institute, Atlanta, GA

Co-Chair: **Jeremy Rodgers**
Department of Defense

6.1: Developing High Density Thin Glass Interposers (3:30)

David H. Levy, Brittany L. Hedrick, Kyle Liddle, Sabina Kanjic, Shelby F. Nelson
Mosaic Microsystems LLC, Rochester, NY

Glass substrates show potential for high performance interposers, with low loss-tangent, low surface roughness enabling fine line lithography, and dielectric properties that do not change with humidity. Thin glass is required to keep signal lines short, and form-factor contained. Building on existing competence in precision, custom through-glass vias, and in-house metallization for via-fill, in this work five layers of redistribution layer (3 on one side, and 2 on the other) are explored in order to fabricate of thin glass interposers that can accommodate relatively high density of interconnects. Daisy-chains explore continuity as functions of RDL trace line/space and dielectric via opening. Bow measurements on thin glass are reported, exploring the effects of film stress of multiple RDL layers on glass.

6.2: Additively Manufactured High Density Interconnects for Defense Microelectronics (3:50)

Ian Armstrong
BAE Systems Inc., Merrimack, NH
and
University of Massachusetts Lowell, Lowell, MA

Alkim Akyurtlu, Guinevere Strack
University of Massachusetts Lowell, Lowell, MA

This paper discusses the fabrication of high-density interconnects (IO) for defense microelectronics using aerosol jet (AJ) printing technology. Multi-chip packages that incorporate mixed-signal and digital components often require packaging that supports IO with a large number of signal and ground pins. As the number of IO increases, IO line width and spacing decrease to accommodate the larger volume of IO. The approach presented herein utilizes AJ processes to fabricate copper interconnects with narrow line widths and spacing. The fabricated IO are evaluated in the context of an exemplar Multi-chip Module.

6.3: Printed Hybrid Electronics (PHE) in a Flight Environment: 3D Printed Electronics on Suborbital Technology Experiment Carrier 9 (SubTEC-9) (4:10)

Beth Paquette, Margaret Samuels, Matthew Minogue
Goddard Space Flight Center, NASA, Greenbelt, MD

Jason Fleischer, Donghun Park
Laboratory for Physical Sciences, College Park, MD

Curtis Hill, Jennifer Jones
Marshall Space Flight Center, NASA, Huntsville, AL

Brian Banks
Wallops Flight Facility, NASA, Wallops Island, VA

Additive manufacturing methods are being developed for the fabrication of high-quality, electronic circuits. Direct-write printing is emerging as one of the more promising additive manufacturing methods for the fabrication of what is being referred to as printed hybrid electronics (PHE). This is the idea of “print what you can and place what you can’t.” Of the various direct-write printing methods, aerosol jet printing offers several advantages over syringe and ink jet printing, such as providing ink stream widths as small as 10–20 microns, and nozzle-to-build plate stand-off heights of 2–5 mm. These capabilities have enabled aerosol jet printing to be used for the fabrication of printed hybrid electronics micro-controller circuits with functionality on par with that of a standard Arduino Mini board. Such a printed hybrid electronics demonstrator circuit was designed and fabricated onto the internal surface of a sounding rocket door panel which launched in April 2023 on Sub TEC 9 from Wallops Flight Facility. The manufacturing methods used to fabricate this printed hybrid electronics circuit are being matured to: 1.) establish design rules; 2.) create standard operating procedures for both design-to-toolpath creation and parts fabrication; and 3.) for the performance of full reliability testing. Progress in all these areas of effort will be presented as well as preliminary results from the sounding rocket flight.

6.4: Sustainable Additive Manufacturing of Fine-resolution Electronic Components and Interconnects for 3D Heterogenous Integration Applications (4:30)

Ahmed Busnaina
Nano OPS, Inc., Burlington, MA

We introduce a new sustainable and scalable technique to manufacture nano and microelectronics additively. The technique eliminates chemical reactions, vacuum-based processes, and etching, by utilizing direct assembly of nanoscale particles or other nanomaterials at room temperature and atmospheric pressure onto a substrate. The technology enables making passive and active components at the nano and microscale using a purely additive process utilizing inorganic semiconductor, metal, and dielectric nanoparticles suspended using colloid chemistry followed by sintering. The process demonstrates the manufacturing of nano and microscale transistors with an on/off ratio greater than 106. The technology enables electronics manufacturing while reducing the cost by 10–100 times. The nano and microscale printing platform enables the heterogeneous integration of interconnected circuit layers of printed electronics on rigid or flexible substrates. Printed applications such as transistors, inverters, diodes, NAND, AND, NOR, and inverters at the micro and nanoscale using inorganic and organic materials will be presented.

6.5: Fiber-Based Interconnect for High Bandwidth and High Performance Co-Packaged Optics **(4:50)**

Kumar Abhishek Singh, Ziyin Lin, Peter A Williams, Darren A Vance, Stephanie Arouh, Henry Vincent Wladkowski, Yiqun Bai, Joel Wright, Bilas Chowdhury, Todd R Coons, Shahin Mani, Vamsi Chandra Meesala, Wei Gong, John C Decker, Allen Chan, John Oh, Sergey Yuryevich Shumarayev, Saikumar Jayaraman
Intel Corporation, Santa Clara, CA

Exhibitor Reception **(6:00–8:00)**
Exhibit Hall

Session 7 (RF Technologies, Components, and Systems)

ADVANCED SI RF TECHNOLOGIES AND APPLICATIONS

Tuesday, March 19 / 3:30 – 4:50 pm / Ballroom B

Chair: **Matthew LaRue**
DEVCOM Army Research Laboratory, Adelphi, MD

Co-Chair: **Christopher Coen**
Georgia Tech Research Institute, Atlanta, GA

7.1: An 8-bit ENOB, 1024-Length, 5 GS/s RF Correlator based on Charge Thresholding (3:30)

Kareem Rashed, Arun Natarajan
Oregon State University, Corvallis, OR

Aswin Undavalli, Shantanu Chakrabartty, Aravind Nagulu
Washington University in St. Louis, St. Louis, MO

This paper presents our initial efforts to develop efficient, high dynamic-range analog correlators as part of the DARPA Massive Cross-correlation (MAX) program. In this paper, a wideband RF correlator based on the margin-propagation (MP) paradigm is presented. The proposed analog correlator replaces traditional multiply-and-accumulate with analog addition and thresholding to enable energy-efficient correlation. The 65 nm CMOS correlator IC supports 5 GS/s inputs, large correlation length of 1024 and 8-bit computing accuracy with high energy efficiency of 152TOPs/J. Practical applications in radar signal detection, code-domain processing, and spectrum sensing are also demonstrated.

7.2: A Robust Near-ZERO Power Wake-up Receiver with –108 dBm Sensitivity (3:50)

Jesse Moody, Benjamin Magstadt, Robert Costanzo, Sean Yen, Travis Forbes, Keith Tracey
Sandia National Laboratory, Albuquerque, NM

Natalie Ownby, Prerana Singaraju, Suprio Bhattacharya, Divya Duvvuri, Steven M. Bowers, Benton H. Calhoun
University of Virginia, Charlottesville, VA

This work presents the first sub-microwatt wakeup receiver with better than –100 dBm RF sensitivity operating over a wide range of temperatures and showing excellent resilience in the face of adversarial RF jamming. This device operates in multiple mission relevant RF bands spanning 100 MHz to over a GHz, with an ultra-compact form factor. At the minimum power consumption level, the device can continually operate for decades powered from a coin-cell battery. This monolithic design includes integrated power management, frequency reference, bias generation and a calibration temperature sensor leading to an ultra-compact form factor. The device operates from –40 C to 70 C with better than –100 dBm sensitivity, and shows significant improvement in figure of merit compared to non-robust state of the art.

7.3: A 26.6–64.6 GHz LNA with Transformer Load Bandwidth Extension in 16 nm FinFET (4:10)

Mingi Yeo, David Dolt, Yu-Lun Luo, David Reents, Samuel Palermo
Texas A&M University, College Station, TX

This paper presents a 26.6–64.6 GHz low-noise amplifier (LNA) designed in a 16 nm FinFET process. The LNA uses a three stage cascode architecture with resistive feedback to achieve wideband input matching (S11) under –10 dB between 26.6–65.8 GHz, and a novel transformer load feedback technique to simultaneously achieve a wide 3 dB gain (S21) bandwidth of 26.1–64.6 GHz. Moreover, by adding a parallel de-Q resistor at the output in parallel with the transformer load, a wideband (S22) match under –8 dB between 24.4–64.7 GHz is achieved. The novel transformer load with coupling extends the bandwidth by creating low and high frequencies peaking in the LNA tank impedance. Overall, the LNA achieves a noise figure (NF) of 4.0–6.2 dB within the operating bandwidth, and has a low power consumption of 17.4 mW. To the author's best knowledge, the LNA achieves the highest FoM of designs with effective bandwidths greater than 20 GHz.

7.4: Wide Tuning Range Millimeter-Wave VCOs in 45 nm SiGE BiCMOS Technology (4:30)

Lauren Pelan, Wil Gouty, Trevor Dean, Samantha McDonnell, Tony Quach
Air Force Research Laboratory, WPAFB, OH

David Dolt, Samuel Palermo
Texas A&M University, College Station, TX

Waleed Khalil
Ohio State University, Columbus, OH

Exhibitor Reception **(6:00–8:00)**
Exhibit Hall

ADVANCES TOWARDS NEXT GENERATION SENSING AND COMMUNICATIONS

Tuesday, March 19 / 3:30 – 5:10 pm / Ballroom C4

Chair: **Manny Trejo**
Department of Defense, Fort Meade, MD

Co-Chair: **Marcia Sawhney**
Department of Defense, Fort Meade, MD

8.1: GaN Microelectromechanical Resonators Operating at High Temperature up to 800 °C (3:30)

Wen Sui, Philip X.-L. Feng
University of Florida, Gainesville, FL

We report on the first experimental demonstration of GaN microelectromechanical Lamb wave resonators (LWRs) operating at high temperature (T) up to 800 °C, while retaining robust electromechanical resonances at ~32 MHz and good quality (Q) factor of Q~450 even at 800 °C. Measured resonances exhibit clear consistency and stability during heating and cooling processes, validating the GaN LWRs can operate at high T up to 800 °C, the highest to date for such all-electrically transduced resonant microelectromechanical systems (MEMS), without noticeable degradation. This study paves the way for advancing GaN MEMS transducers into high-T and hostile environments.

8.2: Giant Ratchet Effect for Terahertz Sensing (3:50)

Michael Shur
Rensselaer Polytechnic Institute, Troy, NY

John Mikalopas, Gregory Aizin
Kingsborough College, The City University of New York, Brooklyn, NY

We show that by launching a terahertz (THz) radiation induced propagating wave in a THz plasmonic TeraFET array and engineering matching between the unit cells could increase the sensor responsivity by orders of magnitude. The resulting coherent response represents a Giant Ratchet Effect (GRE). Specifically, we use the width-varying design of a plasmonic array for achieving a proper matching between the units of the plasmonic crystal.

8.3: Simplified Circuit Models for THz Operating Field Effect Transistors (4:10)

Adam Gleichman, Kindred Griffis, Sergey V. Baryshev
Michigan State University, East Lansing, MI

The electron fluid model in plasmonic field effect transistor (FET) operation is related to the behavior of a radio-frequency (RF) cavity. This new understanding led to finding the relationships between physical device parameters and equivalent circuit components in traditional parallel resistor, inductor, and capacitor (RLC) and transmission models for cavity structures. Verification of these models is performed using PSpice to simulate the frequency dependent voltage output and compare with analytical equations for the drain potential as a function of frequency.

8.4: Numerical Analysis of Dyakonov-Shur Instability in p-Diamond TeraFET (4:30)

Muhammad Mahmudul Hasan, Nezih Pala
Florida International University, Miami, FL

Michael Shur
Rensselaer Polytechnic Institute, Troy, NY

We present the results of the numerical simulation of the Dyakonov and Shur instability in the p-diamond 2D hole gas channel using the hydrodynamic model. Our simulation results predict the instability frequency range at cryogenic and room temperatures and show that p-diamond FETs could operate as sources in the 300 GHz range for 6G communications.

8.5: mmWave Reconfigurable and Miniature On-Chip Filter Based on Vanadium Dioxide for Array Applications (4:50)

Thomas G. Williamson, T. Robert Harris, George Che
Georgia Tech Research Institute, Atlanta, GA

Nima Ghalichechian
Georgia Institute of Technology, Atlanta, GA

This paper presents a prototype reconfigurable filter for use at mmWave band designed for the 25–50 GHz range. This prototype bandpass filter (BPF) incorporates two poles, and has two bands. In band insertion losses (IL) are 1.0 and 1.2 dB respectively, and there is a canonical 12 dB per octave IL roll-off from the pass band. This novel filter uses vanadium dioxide, a phase change material, to vary the length of its coupled transmission lines (TLs). The prototype filter is partially fabricated, and complete results will be presented in the final version of this paper.

Exhibitor Reception (6:00–8:00)
Exhibit Hall

TOOLS FOR TRUST

Tuesday, March 19 / 3:30 – 5:10 pm / Ballroom C1-3

Chair: **Mona Massuda**
Department of Defense, Fort Meade, MD

Co-Chair: **Gail Walters**
Parallax Advanced Research, Colorado Springs, CO

9.1: Full Signal Integrity Analysis Flow for Heterogenous Integration in a Secure Azure Cloud Environment (3:30)

Finbarr McGrath, Shawn Mills
Cadence Design Systems, San Jose, CA

Joe Tostenrude
Microsoft, Redmond, WA

Demand for secure cloud-based technologies within advanced microelectronics ecosystems is upon us. Integrated and full signal and power integrity analysis is required to meet the objectives for enhanced performance, lower costs and cross fabric integration. Industry leaders recognize the utmost importance of enabling secure full design and analysis of these microsystems architectures. A detailed design flow to support data rates of 960 Gbps over 24 AIB channels will be presented. This flow allows detailed simulation of transmission line effects on an interposer. A secure Azure cloud design environment was established with 10 engineering hours of effort allowing Engineers from Cadence, Intrinsix and Microsoft to optimize the design flow and facilitate a seamless collaborative remote cross-company effort. Cadence Sigrity/Clarity, Allegro and Virtuoso platforms were required to comprise Full flow including a full 3D Extraction for a silicon interposer. A 3× improvement over local simulations done for similarly sized devices was achieved.

9.2: HeisenTrojans: A New Class of Hardware Attacks (3:50)

Akshita Reddy Mavurapu, Dean Sullivan
University of New Hampshire, Durham, NH

Xiaolong Guo
University of Kansas, Lawrence, KS

Orlando Arias
University of Massachusetts, Lowell, Lowell, MA

The hardware security community has made significant advances in detecting Hardware Trojan vulnerabilities using software fuzzing-inspired automated analysis. However, the Electronic Design Automation (EDA) code base itself remains under-examined by the same techniques. Our experiments in fuzzing EDA tools demonstrate that, indeed, they are prone to software bugs.

As a consequence, this paper unveils HeisenTrojans attacks, a new hardware attack that does not generate harmful hardware, but rather, exploits software vulnerabilities in the EDA tools themselves. A key feature of HeisenTrojan attacks is that they are capable of deploying a malicious payload on the system hosting the EDA tools without triggering verification tools because HeisenTrojan attacks do not rely on superfluous or malicious hardware that would otherwise be noticeable.

9.3: A Security Engine Solution for Protecting SoC Designs Against Supply-Chain Threats **(4:10)**

Kshitij Raj, Atri Chatterjee, Swarup Bhunia, Sandip Ray
University of Florida, Gainesville, FL

System-on-chip security architecture is a critical, complex, and timing-consuming activity, consuming months of effort. Furthermore, the architecture design can include subtle errors that compromise the security of the entire system. In this paper, we develop a security engine infrastructure, SENTRY for systematically creating security architectures for protecting SoC designs against a variety of security subversions. SENTRY provides a plug-and-play, configurable subsystem composed of custom IPs that can be integrated into the platform to derive different security primitives. We develop an instance of SENTRY for supply-chain attacks. We discuss the spectrum of challenges involved in developing a unified architecture for systematic protection against the variety of attacks involved and the SENTRY approach to address them.

9.4: Security Mitigations Enforcer (SeME): Rapid FPGA Assurance Utility for DoD Systems **(4:30)**

Zachary Jordan, Christopher Sozio, Isaac Stier, Adam Duncan
NSWC Crane – GXV Trusted & Assured Microelectronics, Crane, IN

Grant Skipper
Amentum, Odon, IN

9.5: Point-and-Click Analysis and Hardening to Enhance FPGA Bitstream Security **(4:50)**

David Torres, Andrew Taub
Red Balloon Security, Inc., New York, NY

Grant Skipper
Naval Surface Warfare Center, Crane, U.S. Navy, Crane, IN

FPGAs are notoriously difficult to secure. The intersection between FPGA designers and FPGA security experts is very small. Most engineers view FPGA configuration as black magic and don't have expertise to secure their bitstreams. While FPGA manufacturers provide their own software suites, no independent tools exist for operators to perform vulnerability analysis, testing, and hardening of FPGA bitstreams. Moreover, there are no bitstream security tools that are actually easy and intuitive to use. To address this problem, Red Balloon Security – with the support and funding of JFAC – has developed Bitwise which allows for rapid analysis and modifications of FPGA bitstreams to harden and secure them without requiring access to source code or project design files. Bitwise delivers a variety of FPGA bitstream manipulation techniques without requiring pre-requisite expertise or reverse engineering capabilities, as well as provides operators with recommendations for how to mitigate risks posed by identified threats.

Exhibitor Reception **(6:00–8:00)**
Exhibit Hall

PHOTONIC INTEGRATED CIRCUITS

Tuesday, March 19 / 3:30 – 5:10 pm / Room 6/7

Chair: **Nicholas Usechak**
Air Force Research Laboratory, Wright-Patterson AFB, OH

Co-Chair: **Jim Aldeman**
SPAWAR, San Diego, CA

10.1: High-Performance RF Photonics System Integration via Silicon Photonics (3:30)

Bill P.-P. Kuo, Liangshun Han, Ivan Shubin
Raytheon Advanced Photonics Group, San Diego, CA

Carl Dohrman, Jack W. Holloway
Raytheon Advanced Technology, Arlington, VA

10.2: Wide Temperature Range Uncooled 2.5D Integrated Silicon Photonic DWDM Receiver (3:50)

Maarten Hattink, James Robinson, Liang Yuan Dai, Ziyi Zhu, Asher Novick, Madeleine Glick, Keren Bergman
Columbia University, New York, NY

Padraic E. Morrissey, Peter O'Brien
Tyndall National Institute, University College Cork, Cork, Ireland

Seth Robertson
Peraton Labs, Basking Ridge, NJ

We demonstrate an eight channel dense wavelength division multiplexed 2.5D integrated photonic microring receiver operating error-free at 16 Gbps per wavelength over a 75 degrees Celsius range, while tracking fluctuations of 3.1 degrees Celsius per second, addressing the microring's sensitivity to challenging thermal environments in co-packaged optics in an eight wavelength package, and achieving an aggregate bandwidth of 128 Gbps across the full temperature range. In addition, we also demonstrate the receiver operating at 25 Gbps per wavelength with a slightly increased bit error rate over a range of at least 65 degrees Celsius, providing, in this operating regime, an aggregate bandwidth of 200 Gbps. Appropriate measurement techniques and routes for future improvement in thermal range of integrated photonic receivers are also identified and discussed.

10.3: RF-CMOS Electronic-Photonic Sensing Elements for Millimeter-wave Front-end Systems-on-Chip: Enabling mm-wave Array Scaling/Disaggregation for Radar and Extreme Massive MIMO **(4:10)**

Manuj Singh, Deniz Onural, Hayk Gevorgyan, Xinchang Zhang, Bohan Zhang, Miloš Popović
Boston University, Boston, MA

Ruocheng Wang, Sidney Buchbinder, Vladimir M. Stojanović
University of California, Berkeley, CA

We demonstrate a path to scalable, wavelength-multiplexed RF/mm-wave-photonic front-end systems-on-chip for radar and extreme massive MIMO arrays, in 300 mm-foundry 45 nm RF SOI CMOS. We demonstrate mm-wave-to-optical sensing elements comprising low-noise amplifiers (LNAs) monolithically integrated with triply-resonant photonic microring-resonator based modulators. The "photonic molecule" modulator concept breaks the conventional ring modulator conversion efficiency-bandwidth tradeoff and provides optimal performance RF-photonic applications, while supporting high bandwidth densities. We show a first experiment with projected noise figure of 24 dB at 57 GHz (30 mW/element, –45 dBm RF-input, 6 dBm laser LO). The elements are tileable at small pitches, enabling photonic disaggregation of large-scale phased arrays.

10.4: Co-Design of Monolithic RF and Photonic Integrated Circuits with Packaging **(4:30)**

Jacob Alward, Christian Bottenfield, Jacob Campbell, Meredith Caveney, Christopher Clark, Christopher Coen, Theodore Franklin, Stephen Hurst, Paul K. Jo, Robert Lingle Jr., Nelson Lourenco, Brandon Lovelace, Peter McMenamin, Taylor Peterson, Leif Sandstrom, Billbang Sayasean, Maxwell Tannenbaum, Tucker Turner, Benjamin Yang, Anthony Zenere, Andrew Stark
Georgia Tech Research Institute, Atlanta, GA

Dmitry Kozak, Eric Kamp, Joshua Hawke
Naval Surface Warfare Center, Crane, IN

10.5: Reconfigurable Photonic Chips, Applications, & Integration **(4:50)**

Russell L. T. Schwartz, Nicola Peserico, Hangbo Yang, Hamed Dalir, Volker J. Sorger
University of Florida, Gainesville, FL

Exhibitor Reception **(6:00–8:00)**
Exhibit Hall

ULTRA WIDE BANDGAP MATERIALS

Tuesday, March 19 / 3:30 – 5:10 pm / Room 10/11

Chair: **Thomas Kazior**
DARPA MTO, Arlington, VA

Co-Chair: **David Meyer**
Naval Research Laboratory, Washington, DC

11.1: Ultrawide-Bandgap Semiconductors: Opportunities and Challenges **(3:30)**

Mark A. Hollis
UWBG Group, Celina, TX

David J. Meyer
Naval Research Laboratory, Washington, DC

11.2: Ultra-Wide-Bandgap Nitride Semiconductors: Recent Progress and Ongoing Challenges **(3:50)**

Robert Kaplar, Andy Allerman, Andy Armstrong, Brianna Klein, Andrew Binder, Luke Yates, Mihai Negoita, Jason Neely, Jack Flicker
Sandia National Laboratories, Albuquerque, NM

Nitride-based ultra-wide-bandgap semiconductors such as aluminum nitride, aluminum gallium nitride, and scandium aluminum nitride have outstanding potential for power switching and RF applications. This is based not only on the scaling of their breakdown electric field with bandgap, but also on other properties such as their polar nature and their ability to form heterostructures. While excellent progress has being made to date developing these materials, challenges related to fundamental materials as well as device processing remain. This talk will present a summary of the current state of research in this promising materials system.

11.3: Vertical and Lateral Gallium Oxide Microelectronics **(4:10)**

Andrew Green, Ahmad Islam, Kyle Liddy, Dan Dryden, Nolan Hendricks
Air Force Research Laboratory, Wright-Patterson AFB, OH

11.4: Current Status of Diamond RF Semiconductor Technology **(4:30)**

Tony G. Ivanov, James D. Weil, Leonard M. De La Cruz, Dmitry A. Ruzmetov, Pankaj B. Shah, Bradford B. Pate, Mahesh R. Neupane, Derwin F. Washington, Stephen B. Kelley, Sergey I. Rudin, Brittany T. Kaufmann, Sonja R. Nedeljkovic, Elias J. Garratt, A. Glen Birdwell, Nicholas R. Jankowski
DEVCOM Army Research Laboratory, Adelphi, MD

The drive for higher performance RF semiconductor technologies has spurred research in Ultra-Wide Band-Gap (UWBG) materials. Some of the more extensively studied material systems are high Al content nitrides, alloys of gallium oxide, boron nitride and diamond. This work will give an overview of the current status of the Diamond RF semiconductor technologies, including material choices, reported device performance, and possibilities for future research.

11.5: Panel Discussion – UWBG Semiconductor Technologies **(4:50)**

Tony Ivanov
DEVCOM Army Research Laboratory, New York, NY

Exhibitor Reception **(6:00–8:00)**
Exhibit Hall

WEDNESDAY, MARCH 20

Continental Breakfast, Ballroom Foyer **(7:30–8:30)**

Session 12 **(Packaging, Integration, Thermal and Control Technologies)**

DARPA THERMONAT

Wednesday, March 20 / 8:20 – 10:00 am / Ballroom A

Chair: **Yogendra Joshi**
DARPA MTO, Arlington, VA

Co-Chair: **Sumit De**
Booz Allen Hamilton, Washington, DC

12.1: Efficient Physics-Informed Deep Learning Model for Multiscale Thermal Analysis **(8:20)**

Jiahang Zhou, Ruiyang Li, Wenjie Shang, Bo Zhang, Zhihao Xu, Jyoti Panda, Jianxun Wang, Tengfei Luo
University of Notre Dame, Notre Dame, IN

Thomas Beechem, Edward Walker
Purdue University, West Lafayette, IN

12.2: Full Stack Thermal Solution with Fast Circuit Model Supporting Gate-All-Around Transistor Exploration **(8:40)**

Robert R. Robison, Henry Trombley, Nicholas A. Lanzillo
IBM Research Semiconductors, Albany, NY

Lang Lin, Norman Chang, Xiang Mao, Tianhao Zhang, P. Len Orlando III
Ansys, Inc., Exton, PA

We present a novel thermal solution composed of commercial tools and a multi-scale, multi-tool workflow to address the scalability challenges of modeling static/transient thermal behavior of design structures to predict r eliability risks across the atomistic materials level, transistor, and circuit. Our methodology leverages existing fabricated Gate All Around (GAA) Nanosheet CMOS devices to validate our Technology Computer Aided Design (TCAD) analysis through measurement and simulation comparison prior to generating reduced order models (ROM) that will enable a computationally efficient mechanism to scale across multi-finger multi-device simulations needed to compose an SRAM structure and perform detailed thermal analysis. Utilizing commercial tools, we are able to leverage the existing commercial tech base to rapidly converge on a solution that has strong commercialization opportunity for the defense community within the semiconductor industry.

12.3: Machine Learning Enabled High Precision and Fast Thermal Model of Nanoscale Transistors **(9:00)**

Mayur Singh, Rinku Dutta, Rakshith Saligram, Priyabrata Saha, Saibal Mukhopadhyay, Suman Datta, Satish Kumar
Georgia Institute of Technology, Atlanta, GA

As the channel length is scaled in nanoscale transistors, the self-heating effect gets progressively worse due to increased thermal resistances, reduced thermal capacitance, and dominant thermal boundary resistances at the interfaces of materials. We are developing a high-fidelity atomistic model to predict the thermal properties of Si, SiGe, and their interfaces relevant to a 14 nm node FinFET test-chip and a fast and accurate multi-scale temperature prediction model for the functional block. We are fabricating structures relevant to interfaces in FinFETs and will be using domain thermo-reflectance (TDTR) and time-resolved magneto-optic Kerr effect (TR-MOKE) for high-precision measurements of thermal properties. We will use a frequency-dependent capacitance-based method to extract the channel temperature of FinFETs, which is benchmarked against S-parameter measurements and will help in validating computational models. The experimentally validated fast and high-fidelity multi-scale temperature prediction model will enable accurate reliability assessment of ICs due to self-heating effects.

12.4: Toward Self-Consistent Simulations of Electron-Phonon Transport in Nanoscale Transistors **(9:20)**

Sanjiv Sinha, Shaloo Rakheja
University of Illinois, Urbana, IL

This paper describes the state of electrothermal modeling in nanotransistors and introduces a new combination of models for treating the transport of electrons and phonons in a self-consistent manner. We discuss accuracy and speedup tradeoffs and discuss implementation for deeply scaled three-dimensional transistor geometries.

12.5: Accelerated Multi-Scale Thermal Modeling of Advanced Integrated Circuits **(9:40)**

Alexander J. Gabourie, Connor J. McClellan
DeepSim, Inc., Mountain View, CA

Carlos A. Polanco, Davide Donadio
University of California, Davis, Davis, CA

Subhasish Mitra, Srabanti Chowdhury, Eric Pop
Stanford University, Stanford, CA

Transistor scaling and 3D integration have led to high power densities and temperatures, which degrade circuit reliability and performance. At the same time, circuit complexities and nanoscale features make temperature difficult to measure and predict. As such, new modeling and simulation techniques are needed to simulate temperature accurately and efficiently in nanoscale transistors and circuits. Here, we present our progress on developing a new thermal simulation pipeline from ab initio, atomistic material modeling to single transistors. This pipeline avoids thermal model calibration via costly experimental measurements and accounts for electron-phonon interactions to accurately estimate power dissipation. Future work will focus on validating this simulation pipeline with experiments and developing a complete multi-scale thermal simulator for a full atoms-to-circuits thermal simulation framework.

BREAK **(10:00–10:30)**
Ballroom Foyer

COMPACT FRONT-END FILTERS AT THE ELEMENT-LEVEL (COFFEE)

Wednesday, March 20 / 8:20 – 10:00 am / Ballroom B

Chair: **Todd Bauer**
Sandia National Laboratories, Albuquerque, NM

Co-Chair: **Zachary Fishman**
Booz Allen Hamilton, Washington DC

13.1: A Manufacturable, High Performance, Micro-Acoustic 10.7 GHz RF Filter based on Periodically Polarized Piezoelectric Film (P3F) AlScN BAW Resonators (8:20)

Ramakrishna Vetury, Kamran Cheema, Jeffrey Shealy
Akoustis Technologies, Inc., Huntersville, NC

Jeff Leathersich, Craig Moe, Mary Winters
Akoustis Technologies, Inc., Canandaigua, NY

P3F BAW resonator technology enables a new class of micro-acoustic RF filters at C, X, Ku and beyond. P3F benefits from a significantly larger film thickness than the traditional BAW thickness-frequency scaling approach, enabling a manufacturable and high frequency resonator technology with high coupling and Q-factor and creating high performance micro-acoustic RF Filters at C, X, Ku and beyond.

We report a manufacturable, Periodically Polarized Piezoelectric Film (P3F) Bulk Acoustic Wave (BAW) RF Filter using Aluminum Scandium Nitride (AlScN) materials. Using P3F AlScN BAW resonator technology, we designed and fabricated an RF filter operating at 10.7 GHz, sized 1.8 mm by 1.6 mm and with a pass-band insertion loss of 2 dB, a bandwidth of 600 MHz and out of band rejection significantly better than 30 dB.

13.2: 18 GHz Microacoustic ScAlN Lamb Wave Resonators for K_u Band Applications (8:40)

Luca Colombo, Gabriel Giribaldi, Matteo Rinaldi
Northeastern University, Boston, MA

Jeffrey R. Laroche
RTX, Tewksbury, MA

Adam E. Peczalski, Eduardo M. Chumbes
RTX, Andover, MA

Vikrant J. Gokhale, Brian P. Downey, Matthew T. Hardy
U.S. Naval Research Lab, Washington, DC

13.3: Thin-Film Lithium Niobate as Compact Acoustic Resonator and Filter Platforms at Millimeter Wave (9:00)

Jack Kramer, Vakhtang Chulukhadze, Omar Barrera, Sinwoo Cho, Ruochen Lu
University of Texas at Austin, Austin, TX

Lezli Matto, Kenny Huynh, Michael Liao, Mark S. Goorsky
University of California Los Angeles, Los Angeles, CA

This paper presents our recent work using transferred periodically poled piezoelectric (P3F) lithium niobate (LN) thin films for demonstrating low-loss and compact acoustic resonators and filters at millimeter wave (mmWave) bands. Based on the novel platforms, thickness shear mode piezoelectric resonators are fabricated for mmWave operation. The measured compact acoustic resonators show high electromechanical coupling (k^2) of 7.55% and quality factor (Q) of 222, leading to a figure of merit (FoM, $Q \cdot k^2$) of 16.8 at

50.07 GHz, 50 times higher than the state of the art (SoA) at 50 GHz. Consequently, compact acoustic filters are built with electrically coupled resonators, showing low insertion loss (IL) of 1.29 dB, and fractional bandwidth (FBW) of 20.1% at 21.2 GHz, doubling the operating frequency of SoA acoustic filters while keeping low-loss and wideband.

13.4: Micromachined High-Q and High-coupling Thin-Film Yttrium Iron Garnet Magnetostatic Forward Volume Wave Resonators **(9:20)**

Renyuan Wang, Bill Zivasatienraj
BAE Systems, Inc., Nashua, NH

Sudhanshu Tiwari, Connor Devitt, Anuj Ashok, Sunil Bhave
Purdue University, West Lafayette, IN

13.5: Demonstrating the Disruption of COFFEE Technology **(9:40)**

Zack Fishman
Booz Allen Hamilton, New York, NY

BREAK **(10:00–10:30)**
Ballroom Foyer

ALTERNATIVE COMPUTING PARADIGMS

Wednesday, March 20 / 8:20 – 10:00 am / Ballroom C4

Chair: **Brian Hoskins**
Department of Commerce, Washington, DC

Co-Chair: **Sina Najmaei**
Army Research Laboratory, Adelphi, MD

14.1: Implementation of Neuromorphic Computing Tasks Using Stochastic Computing in Computational Random-Access Memory (SC-CRAM) Based on CMOS+X Platform **(8:20)**

Brandon Zink, Yang Lv, Robert Bloom, Jian-Ping Wang
University of Minnesota Twin Cities, Minneapolis, MN

William A. Borders, Matthew Daniels, Daniel B. Gopman, Brian Hoskins
National Institute of Standards and Technology, Gaithersburg, MD

Pravin Khanal, Weigang Wang
University of Arizona, Tucson, AZ

Advait Madhavan
University of Maryland College Park (UMCP), College Park, MD

Stochastic computing (SC) is a promising solution in neuromorphic computing for two reasons. One is that SC is more noise resilient than conventional data encoding methods. The second is that key arithmetic functions for neuromorphic tasks can be done using a small number of logic gates. However, the hardware needed for stochastic bit generation (SBG) drastically increases the circuit area and energy consumption, making SC unfeasible for large-scale neuromorphic tasks. In this work, we present a novel method called SC-CRAM that significantly alleviates the cost of SBG by embedding SBG and SC processing within the same array using the computational random-access memory (CRAM) architecture. Moreover, we illustrate how arithmetic functions can be performed in SC-CRAM with significantly less hardware than conventional SC methods and conventional data encoding schemes. We also report our recent progress to integrate CMOS with magnetic tunnel junctions (MTJs), a so-called CMOS+X platform, for SC-CRAM experimental demonstrations.

14.2: Neuromorphic Hebbian Learning with Magnetic Tunnel Junction Synapses (8:40)

Peng Zhou, Alexander J. Edwards, Joseph S. Friedman
University of Texas at Dallas, Richardson, TX

Frederick B. Mancoff, Sanjeev Aggarwal
Everspin Technologies Inc., Chandler, AZ

Stephen K. Heinrich-Barna
Texas Instruments, Inc., Dallas, TX

Conventional approaches for neuromorphic computing store synaptic weights in non-volatile memory devices with analog resistance states, permitting in-memory computation of neural network operations while avoiding the costs associated with transferring synaptic weights from a memory array. However, the use of analog resistance states for storing weights is impeded by stochastic writing, weights drifting over time through stochastic processes, and limited endurance. Here we propose and experimentally demonstrate neuromorphic networks that provide high-accuracy inference thanks to the binary resistance states of magnetic tunnel junctions (MTJs), while leveraging the analog nature of their stochastic spin-transfer torque (STT) switching for unsupervised Hebbian learning. We performed the first experimental demonstration of a neuromorphic network directly implemented with MTJ synapses, for both inference and spike-timing-dependent plasticity learning. We also demonstrated through simulation that the proposed system for unsupervised Hebbian learning with stochastic STT-MTJ synapses can achieve competitive accuracies for MNIST handwritten digit recognition.

14.3: Exploring Synaptic Topologies for Mixed-signal Spiking Neural Network (9:00)

Sayma Nowshin Chowdhury, Taseen Forhad, Sahil Shah
University of Maryland, College Park, MD

This work explores the effects of synaptic topologies on overall accuracy, area and power of mixed-signal Spiking Neural Network (SNN). Mixed-signal SNN can process data in real-time with significantly high energy-efficiency. The study uses hardware aware models of synapses and neurons to design a fully connected spiking neural network in a python-based simulation framework. The hardware aware models are based on the measurement results obtained from 65nm CMOS process. Specifically, we use Floating-Gate (FG) synapses to store the weights of the synapses and an adaptive Leaky-Integrate and Fire circuit to model the neurons in the SNN. Additionally, we use localized gradient-based algorithm to learn the FG voltage of the analog synapses of SNN. We evaluate two SNN architecture (Fully-Connected and Recurrent) with different synaptic circuit topologies using neuromorphic MNIST dataset.

14.4: Neuromorphic-P^{2}M: Processing-in-Pixel-in-Memory Paradigm for Neuromorphic Image Sensors **(9:20)**

Md Abdullah-Al Kaiser, Gourav Datta, Peter A. Beerel
University of Southern California, Los Angeles, CA

Ajey P. Jacob
Information Sciences Institute, Marina del Rey, CA

Akhilesh R. Jaiswal
University of Wisconsin-Madison, Madison, WI

The high volume of data transmission between the edge sensor and the cloud processor leads to energy and throughput bottlenecks for resource-constrained edge devices focused on computer vision. Hence, researchers are investigating different approaches by executing computations closer to the sensor to reduce the transmission bandwidth. In this work, for the first time, we propose a non-von-Neumann analog processing-in-pixel paradigm to perform convolution operations inside the pixel array that consume significantly less energy than their digital MAC alternative. To make this approach viable, we incorporate the circuit's non-ideality, leakage, and process variations into a novel hardware-algorithm co-design framework that leverages extensive HSpice simulations of our proposed circuit using the GF22FDX technology node. We verified our framework on state-of-the-art neuromorphic vision sensor datasets and show that our solution consumes 2× lower backend-processor energy on the IBM DVS128-Gesture dataset than the state-of-the-art while maintaining a high test accuracy of 88.36%.

14.5: Object Tracking in 3D Space via Stereoscopic Artificial Compound Eyes Implemented with In-Sensor Computing **(9:40)**

Byungjoon Bae, Kyusang Lee
University of Virginia, Charlottesville, VA

Arthropod eyes offer superior object tracking and a broad field of view due to their distinct structure. In this work, we emulated the Arthropodal vision system with artificial compound eyes linked stereoscopically, allowing us to detect and track objects in 3D over a wide view. To ensure rapid response and minimal latency, data storage, transportation, and energy use, we processed visual data in the edge of the system. We integrated artificial synapses at the sensor's pixel level, and microprocessor near to the sensor that implements federated split learning (FSL). Our designed stereoscopic artificial compound eye excels in precise object detection and optical flow tracking, showcasing a small root mean square errors (RMSE). It uses significantly lower power per detection compared to traditional methods. This biomimetic imager highlights the potential of merging nature’s designs with co-developed hardware and software technologies, pushing the boundaries of edge computing and sensing capabilities.

BREAK **(10:00–10:30)**
Ballroom Foyer

ADVANCED VERIFICATION AND VALIDATION

Wednesday, March 20 / 8:20 – 10:00 am / Ballroom C1-3

Chair: **Vivian Kammler**
Sandia National Laboratories, Albuquerque, NM

Co-Chair: **Wayne Churaman**
Army Research Laboratory, Adelphi, MD

15.1: A Framework for Post-silicon Analog Design Verification and Validation **(8:20)**

Vince McKinsey, Andrew Elliott, Benjamin Hayden, Yaser Helal, Adam R. Waite, Jon Scholl, Adam Kimura
Battelle Memorial Institute, Columbus, OH

Jamin McCue
Air Force Research Lab, Dayton, OH

Shane Smith
SenseICs, Columbus, OH

15.2: Considerations for Incorporation of 3D Heterogenous Integration Packaging into a Monolithic Post-silicon Verification and Validation Workflow **(8:40)**

Jon Scholl, Yash Patel, Noah Padro, Adam R. Waite, John Kelley, and Adam Kimura
Battelle Memorial Institute, Columbus, OH

Matt Sale
Air Force Research Laboratory, Wright-Patterson AFB, OH

15.3: Increasing Microelectronics Security Assurance with Information Flow Analysis **(9:00)**

Jagadish Nayak
Cycuity, Inc., San Jose, CA

Monir Zaman
Raytheon, An RTX Business, McKinney, TX

Hardware security assurance for systems and custom microelectronics is a critical focus area for the Department of Defense. Identifying potential security weaknesses in hardware designs is crucial for maintaining data integrity and protecting against potential threats. However, conventional security verification approaches often overlook unknown or unexpected security weaknesses, leaving blind spots that can be exploited. Verification teams struggle to handle the scale and complexity of security requirements, making it challenging to map them into actionable verification constructs. Information flow-based techniques have proved to be effective at addressing these concerns. We present an approach that leverages information flow for security analysis and assurance. Our focus is on eliminating unintended data path vulnerabilities that could compromise the Hardware Root-of-Trust, secure data paths, and overall system operation, and highlight a successful implementation by Raytheon showcasing the effectiveness of leveraging information flow analysis to enhance the security and hardware assurance of a design.

15.4: Third-party Intellectual Property Verification Flow for Central Information Repository **(9:20)**

Kyle Ahearn, Ryan Walker, Mark Labbato, Marshall Grady, Harrison Evans, Angelo Maggiacomo, Russell Emmert, Barry Vincent, Saverio Fazzari
Booz Allen Hamilton, Beavercreek, OH

Scott Wartenberg
Wartenberg Consulting, LLC, Vienna, VA

Kevin J. McCamey, Matthew D. Sale, Vipul J. Patel
Air Force Research Laboratory, Wright-Patterson AFB, OH

15.5: Third-Party IP Verification and Validation for Post-Silicon Recovered Designs **(9:40)**

Joshua Delozier, Noah Taylor, Tim McDonley, Katie Liszewski, Adam Kimura
Battelle Memorial Institute, Columbus, OH

Richard Ott, Matt Sale
Air Force Research Lab, Dayton, OH

BREAK **(10:00–10:30)**
Ballroom Foyer

APPLIED PHOTONICS

Wednesday, March 20 / 8:20 – 9:40 am / Room 6/7

Chair: **Paul Devgan**
Air Force Research Laboratory, Wright-Patterson AFB, OH

Co-Chair: **Nicholas Usechak**
Air Force Research Laboratory, Wright-Patterson AFB, OH

16.1: Signal-driven Assured Detection and Digital IQ Capture of Transient RF Events (ADDiqCT) **(8:20)**

Kris D. Merkel, Justin Hogan, Clint Gauer, Kevin Winn, Trent Jackson
S2 Corporation, Bozeman, MT

16.2: Photonics Enabled Nyquist Zone Folding Receiver **(8:40)**

Wenlu Chen, Han Hsieh, Daniel Esman, Mark Laliberte, Oliver King
Raytheon / Collins Aerospace, Columbia, MD

The signals intelligence community is facing a daunting challenge as the swath of the electromagnetic (EM) spectrum used by military and commercial applications grows wider and moves to ever higher frequencies. At the same time, increasing signal complexity is driving the need for digital receivers capable of capturing wide bandwidths with high dynamic range. Collins Aerospace has developed a non-uniform sampling Nyquist zone folding receiver (NZFR) that leverages the performance advantages of RF photonic sampling and novel photonic - electronic interfaces. The NZFR allows for the capture of large bandwidths spanning many Nyquist zones while unambiguously determining the signal frequency. We have demonstrated the capture of signals spanning 8 folded 4 GHz wide Nyquist zones, reducing the data handling burden by a factor of 8. The recovered signals have a resolution of over 5 effective number of bits (ENOB) for frequencies up to 50 GHz in this initial demonstration.

16.3: Simultaneous Multi-Mission Optical Link Analog RF Over Fiber Optic Transport with Multiple Outputs **(9:00)**

Christopher K. Huynh, Chunyan L. Lin
NIWC Pacific, San Diego, CA

16.4: Military Avionics Fiber-Optic Transceiver Technology and Link Loss Budget Implications at 100 Gb/s and Higher **(9:20)**

Mark Beranek, Obidon Bassinan
Naval Air Warfare Center Aircraft Division, Patuxent River, MD

Anthony Campillo
US Naval Research Laboratory, Washington, DC

Jim Tatum
Dallas Quantum Devices, McKinney, TX

Sandra Skendzic, Charles Kuznia, Joe Ahadian
Ultra Communications, Vista, CA

An Ly, Jason Holmstedt, Andrew Tahk, Roy Huallpa
Intellisense Systems, Inc., Torrance, CA

BREAK **(10:00–10:30)**
Ballroom Foyer

THERMAL TECHNOLOGIES

Wednesday, March 20 / 10:30 am – 12:10 pm / Ballroom A

Chair: **Christal Gordon**
Booz Allen Hamilton, Arlington, VA

Co-Chair: **Daniel Radack**
Institute for Defense Analyses, Alexandria, VA

17.1: A Commercial Perspective on the Thermal Challenges of DoD 3DIC Heterogenous Integration (10:30)

P. Len Orlando III, Lang Lin, Norman Chang, Wenbo Xia, Tianhao Zhang
Ansys, Inc., Exton, PA

Rob Aitken
Synopsys, Inc., Mountain View, CA

Jointly, Ansys and Synopsys provide their commercial perspective on the DoD's pursuit of 3D Heterogenous Integration as a pathway to achieve adversarial overmatch capability for U.S. National Security. The authors will utilize their unique perspective to identify overlapping technologies that benefit both commercial and DoD sectors as it relates to leap-ahead fine grain thermal aware place and route. Discussion will include comparing and contrasting commercial and DoD drivers to map capability and function to a multi-tier volume.

17.2: Improved Thermal Boundary Conductance at Au/Ultra-Wide Bandgap Semiconductor Interfaces using a Phonon Bridge (10:50)

LeighAnn S. Larkin, Gregory A. Garrett, A. Glenn Birdwell, Nicholas R. Jankowski, Tony G. Ivanov, M. Wraback
DEVCOM Army Research Laboratory, Adelphi, MD

Nolan S. Hendricks, Andrew J. Green
Air Force Research Laboratory, Wright-Patterson AFB, OH

Optimizing the thermal boundary conductance of metal contact/ultrawide bandgap interfaces offers a promising thermal management strategy at the device-level. The "phonon bridge," a thin layer with intermediate vibrational properties inserted between the metal and ultrawide bandgap, provides an opportunity for improving the thermal boundary conductance beyond the baseline interface. In this work, we present thermal boundary conductance measurements on Au/diamond and Au/β-Ga_2O_3 interfaces that incorporate a phonon bridge to improve the thermal transport. For Au/diamond, an oxygen termination layer enhanced the thermal transport from 10 to 99 MW/m^2K. At Au/β-Ga_2O_3 interfaces, a thin layer of Ti improved the thermal transport from 30 to 150 MW/m^2K.

17.3: Enhancing AlN Crystallographic Properties and Thermal Conductivity Using HiPIMS + Kick Deposition (11:10)

Ping-Che Lee, Diego A. Contreras Mora, Aaron McLeod, Andrew Kummel
University of California, San Diego, La Jolla, CA

Mingeun Choi, Satish Kumar
Georgia Tech, Atlanta, GA

This report demonstrates sub-micron-scale single-crystal-like AlN thick films deposited by Advanced High-Power Impulse Magnetron Sputtering (HiPIMS) Plus Kick on lattice-mismatched Si (111) at 120 °C. A 25 V kick with a 50 us pulsing length followed by each main negative voltage pulse generated a highly ionized flux species, which was experimentally proven to be a crucial element for achieving single texture and ultra-smooth AlN. Further frequency-domain Thermoreflectance (FDTR) measurements show a record-high thermal conductivity (112 W/m-K), indicating the potential application of this advanced PVD in the next generation of Back-End-of-Line Dielectric heat spreader.

17.4: A Novel Interlayer for Diamond Integration with (U)WBG Semiconductors for Thermal Management (11:30)

Ariful Haque, Saif Taqy, Pallab Sarkar
Texas State University, San Marcos, TX

Thermal management in ultrawide-bandgap (UWBG) high-power devices has become a major issue due to the insufficient thermal conductivity of the semiconductors for efficient heat dissipation during device operation and increased power density requirements in modern microelectronic systems. This research utilizes a thin Q-carbon (quenched carbon) interlayer on GaN, AlN, and Ga_2O_3 using laser annealing in order to facilitate diamond integration while removing the requirement for any seed layer or non-carbon interlayer. The Q-carbon on these materials acts as the nucleation layer for consistent, high-quality, and low-stress diamond development, shields the underlying semiconductor film from degradation of the harsh growth environment of diamond, and eliminates the thermal mismatch between the UWBG materials and diamond. Thus, this unique combination holds the potential to solve UWBG-based high-power devices' heat management problem and get us closer to materials' theoretical potential for wireless/5-g communications, high-power devices, and other sophisticated microelectronic systems.

17.5: Multi-Temperature Zone Optimization of Cryogenic Systems (11:50)

Nurzhan Zhuldassov, Rassul Bairamkulov, Eby G. Friedman
University of Rochester, Rochester, NY

Heterogeneous computing utilizes different distinct technologies within a single system. The individual components of such a system are often located within distinct temperature regions. Selecting the appropriate operating temperature has a significant impact on various factors such as power dissipation, heat load, cooling power, system performance, and the ambient temperature. To this date, no multi-temperature design methodology exists. To address these limitations, a framework for optimizing the performance of heterogeneous computing systems is presented in this paper. A graph representation is used to address the effects of operating temperature on delay and power consumption of a system. Additionally, thermal interactions between the components in a system are considered to provide a more accurate assessment of the total power usage and heat load. In a practical case study, the target temperature of each component within a quantum computing system is determined to minimize the total power under target performance constraints.

LUNCH **(12:10–1:30)**
Exhibit Hall

NOVEL RF DESIGNS AND IMPLEMENTATIONS

Wednesday, March 20 / 10:30 am – 12:10 pm / Ballroom B

Chair: **Lauren Pelan**
Air Force Research Laboratory, Wright-Patterson AFB, OH

Co-Chair: **Gerald DeJean**
RTX Corporation, Atlanta, GA

18.1: Frequency Stability of Single-Crystal Silicon Thermal-Piezoresistive Resonators with Phase-Locked Loop (10:30)

Connor A. Watkins, Jaesung Lee
University of Florida, Gainesville, FL

Jonathan P. McCandless
Air Force Research Laboratory, Wright-Patterson AFB, OH
and
Case Western Reserve University, Cleveland, OH

Harris J. Hall
Air Force Research Laboratory, Wright-Patterson AFB, OH

Philip X.-L. Feng
University of Florida, Gainesville, FL
and
Case Western Reserve University, Cleveland, OH

This paper reports on a single-crystal silicon (Si) thermal-piezoresistive resonator (TPR) achieving very high frequency stability in phase-locked loop (PLL) measurements. A pair of resonators operating in a balanced-bridge configuration is presented, with one device being driven at resonance and the other used to null the background response. The resonance frequency of the single TPR is collected over 40 hours with closed-loop tracking by PLL and yields Allan deviation of 2.66 ppb for an averaging time of 4.95 seconds, which is the lowest reported value among all Si TPRs studied to date. This result is significant as it suggests that such TPRs can potentially achieve frequency stabilities comparable to, or better than, existing state-of-the-art resonators used in oscillator circuits, with significantly reduced external thermal control requirements and power demands.

18.2: Autonomous Magnet-free Integrated Circuit L-band Circulators (10:50)

Chris May, Karun Vijayraghavan
Nanohmics Inc., Austin, TX

Dimitrios Sounas
Wayne State University, Detroit, MI

18.3: A D-band Frequency-Doubling Solid-State Traveling-Wave Amplifier **(11:10)**

Lei Li, Tianze Li, James C. M. Hwang
Cornell University, Ithaca, NY

Patrick Fay
University of Notre Dame, Notre Dame, IN

We report a solid-state traveling-wave amplifier (TWA) realized through monolithic integration of transistors with a substrate-integrated waveguide (SIW). The TWA uses a stepped-impedance microstrip line as the input divider, but a low-loss, high-power-capacity SIW as the output combiner. The input signal is distributed to four GaN high-electron-mobility transistors (HEMTs) evenly in magnitude but successively delayed in phase. To overcome the limited speed of the GaN HEMTs, they are driven nonlinearly to generate second harmonics and their fundamental outputs are suppressed with the SIW acting as a high-pass filter. Under an input at 70 GHz and 15 dBm, the output at 140 GHz is 38-dB above that at 70 GHz. Under an input around 70 GHz and 20 dBm, the output around 140 GHz is 14 dBm with a 3-dB bandwidth of approximately 6%. This proof-of-concept demonstration opens the path to improving the gain, power and efficiency of sub-terahertz TWAs.

18.4: Advancements in Photoconductive Solid-State Plasma Circuits and Antennas **(11:30)**

Thomas R. Jones
Purdue University, West Lafayette, IN
and
Jones Microwave Inc., Edmonton, AB, Canada

Dimitrios Peroulis
Purdue University, West Lafayette, IN

This paper reports recent advancements by our group in photoconductive solid-state plasma (SSP) high-power and high-speed circuits and antennas. Our work has demonstrated clear advantages of SSP over typical microwave switching technologies including measured insertion losses <0.1 dB, isolation >20 dB, power handling >100 W, linearity >68.8 dBm, hot switching at 30 W, and switching speeds <4 μs. For millimeter-wave to sub-THz applications, SSP waveguide switches operating in W-band have demonstrated insertion loss <0.2 dB and isolation >40 dB, with direct connection into standard flanges. The SSP switches are also manufactured in a low-cost well-established semiconductor platform for ease of integration. Our experiments into reconfigurable SSP antennas have shown good ON state gain while becoming indistinguishable from standard substrates in the OFF state. Additional technological highlights and measured performance of our work with this exciting technology will be presented, along with its comparison to the state-of-the-art and future directions.

18.5: An Aerosol Jet Printed Ka-Band Wilkinson Power Divider **(11:50)**

Koltin Grammer, John Albrecht, Prem Chahal, Matt Hodek, John Papapolymerou
Michigan State University, East Lansing, MI

Aerosol jet printing (AJP) is gaining attention in additive manufacturing research, especially in the discipline of microwave engineering. This manufacturing method allows for easily customizable designs that give designers more freedom to fabricate components that can be customized to facilitate integration and assembly at minimal cost. Additionally, this process can print features as small as 10 μm, which is necessary for high frequency devices. To display the effectiveness of AJP a Wilkinson power divider that operates in the Ka frequency band was designed and fabricated using only additive materials. Measurements of the divider show a good input match, high isolation between output ports, and low insertion loss. Future applications of this process could be used to fabricate N-port dividers that are not commercially available as well as other RF components that are not power dividers.

LUNCH **(12:10–1:30)**
Exhibit Hall

Session 19 **(RF Technologies, Components, and Systems)**

RF SYSTEM DESIGN AND IMPLEMENTATION

Wednesday, March 20 / 10:30 am – 12:10 pm / Ballroom C4

Chair: **Peter Buxa**
Air Force Research Laboratory, Wright-Patterson AFB, OH

Co-Chair: **Adilson Cardoso**
Raytheon, Atlanta, GA

19.1: Micro-Small Form Factor (uSFF) Staring Receiver (Low SWaP Ultra-Wideband Spectral Sensor) **(10:30)**

Orion Davies
Collins Aerospace, An RTX Business, Cedar Rapids, IA

19.2: A 4–40 GHz SiGe Reconfigurable Superheterodyne Transceiver for Multi-Function Arrays **(10:50)**

Arya Moradinia, Christopher T. Coen, Peter McMenamin, Nelson E. Lourenco, Joji Joseph, Craig Swanson, Jacob Alward, Meredith Caveney, Paul Jo, John Morse
Georgia Tech Research Institute (GTRI), Atlanta, GA

Wonsub Lim, Sanghoon Lee, Clifford D. Cheon, John D. Cressler
Georgia Institute of Technology, Atlanta, GA

19.3: Miniature Ka-band Down-Converter Module for Electronic Warfare **(11:10)**

Christopher Moncsko, Steve Huettner, Tim Cruz, Christopher Hatfield, Robert Nowosielski, J. Robert Reid
Cubic Nuvotronics, Durham, NC

Carlos Rezende
Zoetis, Durham, NC

A state-of-the-art millimeter-wave downconverter module is realized using Nuvotronics' PolyStrata® fabrication process. It features a 12th-order pre-select filter, an image-rejection mixer, and an IF output chain divided into three sub-harmonic bands to greatly reduce spurious emissions. The module provides 30 dB gain, 5 dB noise figure, 12 dBm output P1dB with 5 watts DC dissipation. It is being fully qualified for airborne applications.

19.4: Reinforcement Learning Applied to Reconfigurable Hardware in Contested Environment **(11:30)**

JinHong Chen, Waleed Khalil
Ohio State University, Columbus, OH

Russell Wyse, Orion Davies
Collins Aerospace, Cedar Rapids, IA

Samantha McDonnell, Tony Quach, Stephen Hary
Air Force Research Laboratory, Dayton, OH

This paper reports on the demonstrations of Reconfigurable Electronics for Multi-function Agile RF (REMAR) project. The modern electromagnetic (EM) spectrum has become a very dense and crowded place. Maintaining efficient spectrum management will be the difference between a failed connection and a successful link. Complex hardware is required to implement systems that can yield relevant research results in this field with the precision and speed to both block and maintain data links. Reconfigurable hardware exists so that it can provide efficient use of the spectrum, but optimal settings must be determined for a span of wide parameters. Reinforcement learning algorithms can be applied to reconfigurable hardware to achieve a strategy of exploiting action-value estimates to obtain the optimal balance between identifying local rewards and exploring the environment. With reinforcement learning applied, the previous reconfigurable hardware was able to recover approximately 5 dB of SNR with a static in-band interferer present.

19.5: Multichip Synchronization of a X-Band Direct Sampling Digital Beamforming System **(11:50)**

Sam Ringwood, Ian Beavers
Analog Devices, Inc., Durham, NC

This paper outlines a system platform developed by Analog Devices, Inc. that enables direct sampling at X-Band for digital beamforming applications with an emphasis on multichip synchronization. The system platform consists of 16 transmit channels, 16 receive channels with a complete DC power design, clock architecture, and RF front end circuitry centered around the latest mixed-signal front end data converter chipset. Included in this paper is an overview of the system platform with a focus on the clock architecture and the synchronization protocol required to synchronize distributed data converter sample clocks to achieve phase determinism.

LUNCH **(12:10–1:30)**
Exhibit Hall

COUNTERFEIT DETECTION AND AVOIDANCE

Wednesday, March 20 / 10:30 am – 12:10 pm / Ballroom C1-3

Chair: **Saverio Fazzari**
Booz Allen Hamilton, Washington, DC

Co-Chair: **Christian Eakins**
Air Force Research Laboratory, Wright-Patterson AFB, OH

20.1: Self-Referencing Electrical Tests Using SRAM Power-up States for Detecting Recycled ICs (10:30)

Gaines Odom, Zakia Tamanna Tisha, Ujjwal Guin
Auburn University, Auburn, AL

Recycled ICs continue to persist due to the lack of effective detection techniques. To develop an effective detection method, one of our previous works introduced the concept of detecting recycled ICs using SRAM power-up states, exploiting the inherent symmetry of 0 and 1 logic states in newly manufactured SRAM cells. However, often in SRAMs manufactured with older technology nodes, the reference parameter of 50% 1s is less prominent due to systematic design variation that biases all cells in one direction. This paper proposes a robust self-referencing approach for detecting recycled ICs to address this problem. In this proposed method, the power-up states of an IC under test are divided into subregions for similarity analysis of the percentage of 1s in them. Our study establishes that the percentage of 1s in all subregions of a newly manufactured IC is statistically more similar to each other than that in a recycled IC.

20.2: A Process Attestation Time-Based Sensor Leveraging Back-End-of-Line Resistance and Capacitance (10:50)

Jen-Chieh Hsueh, Michael Kines, Shane Smith, Waleed Khalil
Ohio State University, Columbus, OH

Jamin McCue, Brian Dupaix, Vipul J. Patel
U.S. Air Force Research Laboratory, Dayton, OH

20.3: Reconfigurable Pre-Amplifier Physical Unclonable Function and True Random Number Generator **(11:10)**

Eric Hunt-Schroeder
Marvell Technologies, Burlington, VT
and
University of Vermont, Burlington, VT

Tian Xia
University of Vermont, Burlington, VT

A Reconfigurable Physical Unclonable Function that can transform into a True Random Number Generator. The combination of static and dynamic entropy in one IP block reduces area, power, and integration complexity over designs with independent PUF and TRNG blocks. Static entropy is achieved by exploiting transistor variation in a 7-transistor bitcell. The bitcell is divided into a PMOSFET pull-up network and NMOSFET pull-down network with independent control. This independent addressing allows for bitcell regrouping and key refreshes. Dynamic entropy for a TRNG is achieved by enabling multiple bitcells to force the differential voltage used during sensing into state that is highly susceptible to noise. We then randomize the number of bitcells active, the duration active, the address and operating conditions of the underlying cells, which resulting in random, unique, and unpredictable number generations. All these functions are achieved with zero additional array area overhead.

20.4: Comparison of Approaches for Detecting Recycled FPGA Devices **(11:30)**

Frank T. Werner, Stephen Hurst, Christopher R. Clark
Georgia Institute of Technology, Atlanta, GA

Recycled microelectronic devices are a major concern for the electronics industry. They have a shortened lifespan and can cause the systems that rely on them to fail early. While Field-Programable Gate Arrays (FPGAs) are an attractive target for recycling given their price and widespread usage, few approaches for detecting them have been proposed. This paper investigates two promising approaches: electromagnetic (EM) reflectance and internal ring oscillators (ROs). The effectiveness of both approaches at detecting recycled FPGAs is evaluated.

20.5: Metastable Metal Particles as Physically-Timed Keys **(11:50)**

Andrew Martin, David Sky Kanoy, Eva Boyce,
Aydin Aysu, Martin Thuo
NC State University, Raleigh, NC

LUNCH **(12:10–1:30)**
Exhibit Hall

POWER ELECTRONICS PACKAGING AND MAGNETICS

Wednesday, March 20 / 10:30 – 11:50 am / Room 6/7

Chair: **Karl Hobart**
Naval Research Laboratory, Washington, DC

Co-Chair: **Travis Anderson**
Naval Research Laboratory, Washington, DC

21.1: A History of Silicon Carbide (SiC) Wide Bandgap (WBG) Advancement through Power Electronic Building Blocks (PEBB) and Implications for the Future (10:30)

LJ Petersen
ONR, Carlisle, PA

In 1994, the Power Electronic Building Block (PEBB) program was initiated by ONR. The PEBB program was an integrated program of material, device, circuit, and system science and technology (S&T) development The program's core objective was to reduce the size, weight, and cost (SWaP-C) of power electronics (PE) to realize PE shipboard power systems enabling future affordable and powerful electric warships. Since then much has been completed through PEBB advancement to include revealing science and technology (S&T) gaps, (i.e., the need for soft magnetic materials to realize even higher power density PEBB systems.) The past half century has seen the advancement of material development of WBG technologies through the concerted efforts of ONR and the other DOD agencies, and have most recently harvested the fruit of the material advances of SiC into applications that will benefit both the DOD and industry. The future is bright for SiC WBG PEBB based technology.

21.2: Advances in Soft Magnetics for Wide and Ultrawide Bandgap Semiconductor Power Electronics (10:50)

P. Ohodnicki, L. Wewer, Y. Wang, T. Paplham, S. Mullurkara, B. Bhandari, D. Mandal, C. Zheng, T. Marzec, B. Grainger
University of Pittsburgh, Pittsburgh, PA

R. Raju
Fastwatt, LLC, Clifton Park, NY

Recent advances in wide bandgap (WBG) semiconductor-based power electronics have driven the urgent need for concomitant advances in enabling soft magnetic materials and component technologies. Looking further into the future, the promise of ultra-wide bandgap (UWBG) semiconductor technologies can potentially open a new operational envelope of frequency – power – voltage that will place even more demands on the soft magnetics. However, there remain significant challenges in developing new materials and magnetic component designs specifically for UWBG applications. This paper and presentation will overview latest state of art in soft magnetics technologies being explored for aggressive operational envelopes relevant for both WBG and UWBG semiconductor materials. Emphasis will be placed upon novel concepts in ferrite based soft magnetics, however new ideas in nanocrystalline metallic alloy based soft magnetics will also be briefly reviewed and discussed.

21.3: Magnetic Paste Feedstock for Additive Manufacturing Power Magnetics (11:10)

Guo-Quan Lu, Khai D. T. Ngo
Virginia Tech, Blacksburg, VA

The ability to additively manufacture power inductors and transformers would accelerate innovations in switch-mode power converters. However, the advanced manufacturing technique has been challenged by the lack of appropriate feedstocks for making high performance cores. To overcome the challenge, we formulated pastes of magnetic powders as feedstocks for a multi-extruder extrusion printer. Two types of feedstocks were fabricated: powdered-iron and ferrite. The powdered-iron paste could be printed and then cured at temperatures below 250 °C, while the ferrite paste could be printed and then sintered at temperatures below 1000 °C. Cores made with the powdered-iron pastes could have a relative permeability ranging from 10 to 40, while those with the ferrite pastes from 10 to 500. The cores could also have core-loss densities comparable to or lower than their respective commercial cores in the MHz frequency range. Our findings show the promise of additive manufacturing high performance power magnetic components.

21.4: Challenges with 3DHI Technologies for High Power and High Voltage Electronics (11:30)

Andrea Wallace, Jeffrey Ewanchuk, Parag Kshirsagar
RTX Technology Research Center (RTRC), East Hartford, CT

This paper addresses the concerns and roadblocks associated with implementing 3D heterogeneous integration (3DHI) technologies for high-power (kW-MW) and high voltage (kV) power electronic packages. Advancements and innovation in interconnect technology, substrate and printed wiring board manufacturing, thermal management integration, and EDA co-design tools are needed for 3D architectures and technologies to be realized for high power and high voltage packaging. This talk will dive deeper into the inadequacies of the current technologies and speak to the improvements needed to tackle the difficulties of 3DHI in high power and high voltage packaging.

LUNCH **(12:10–1:30)**
Exhibit Hall

DoD WORKFORCE DEVELOPMENT ACCOMPLISHMENTS AND FUTURE DIRECTIONS PANEL

Wednesday, March 20 / 10:30 am – 12:10 pm / Room 10/11

LUNCH **(12:10–1:30)**
Exhibit Hall

RADIATION HARDENED TECHNOLOGIES AND SYSTEMS

Wednesday, March 20 / 1:30 – 3:10 pm / Ballroom A

Chair: **Pauline Paki**
DHS Science and Technology, Washington, DC

Co-Chair: **Patrick Nsengiyumva**
The Boeing Company, Huntington Beach, CA

22.1: Total Ionizing Dose Results from the Yellowstone TCV for Comprehensive Radiation Testing in a 12/14n m FinFET Process Node **(1:30)**

J. S. Kauppila, S. T. Vibbert, M. S. Evans, G. D. Poe, A. K. Wright, P. G. Megginson, N. S. Hoffer, E. J. Rodenkirch, V. Pundith, T. D. Haeffner, D. S. Vibbert, C. J. Moyers, D. J. Pauls, L. W. Massengill
Reliable MicroSystems LLC, Franklin, TN

A. I. Vidana, N. A. Dodds, R. N. Nowlin
Sandia National Laboratories, Albuquerque, NM

T. M. Wallace, H. J. Barnaby
Arizona State University, Tempe, AZ

22.2: A Study of Total Dose Radiation Effects in Ka-Band Fractional-N PLLs in 45 nm SiGe BiCMOS **(1:50)**

David Dolt, David Reents, Samuel Palermo
Texas A&M University, College Station, TX

Lauren Pelan, Samantha Mcdonnell, Trevor Dean, Will Gouty, Tony Quach
Air Force Research Laboratory, WPAFB, OH

Shane Smith, Waleed Khalil
The Ohio State University, Columbus, OH

22.3: FIERA: An FPGA Emulation-based Hardware Soft Error Tolerance Evaluation Platform for SoCs **(2:10)**

Oguz Atli, Prashanth Mohan, Ken Mai
Carnegie Mellon University, Pittsburgh, PA

Michael P. King
Intel Corporation, Santa Clara, CA

22.4: Radiation Hardness Assurance: Automated Single Event Latch-up Identification Prior to Device Fabrication **(2:30)**

Melanie Berg
Space R^3 LLC, Melbourne, FL

Karen Henderson
Siemens EDA, Boston, MA

We present an automated approach for identifying circuits that are vulnerable to single event latch up (SEL). It involves the application of Siemens Calibre® PERCTM reliability-verification tool throughout an integrated circuit's design process. A benefit of the tool's usage is that it requires no radiation testing;

and it is used prior to device fabrication. In addition, the tool has proven to be more effective than other methods of SEL identification such as dynamic-simulation and design rule checks (DRC).

22.5: GlobalFoundries RadHard Ecosystem (2:50)

Deniz Civay
GlobalFoundries, Malta, NY

Lloyd Massengill
Reliable Microsystems

Kristine Schroeder
Avalanche Technologies, Fremont, CA

Felicia James
Apogee

Ian Land, Jeff Wetch
Synopsys

Stephanie Pusch
Trusted Semiconductor Solutions

Robert DeMoulin
Menta

Michael Walton
Spectral Design

Afusat Dirisu, Adam Sherer, Darin Heckendorn
Cadence

Patrice Parris
VORAGO Technologies

Zohair Zia, Karen Henderson, Brett Attaway
Siemens Government Solutions

Dan Benveniste
Northrop Grumman

Tom Wolf, Tom McKay
Silicon Technologies

Klas Lilja
Robust Chip

To withstand the extreme environment of space chips must be customized, either in the design, tuned process changes to the technology platform or through the use of intrinsic platforms. The timeline from idea to implementation takes many years, relying on coordinated handoffs between many companies. The GF RadHard (RH) Ecosystem is working to accelerate this window by improving efficiencies, quality and access to radiation hardening chip technology through collaboration between commercial and DoD stakeholders. The GF RH EcoSystem currently has four lanes, targeting the most pressing categorical challenges faced by the community: RH by Design Methodology, RH IP Storefront, RH Data Sharing and RH by Process. Lane teams are focused on identifying and developing collaborative whitepapers to address these challenges with intent toward more actionable outcomes. Working to align DoD needs with a commercial lens will aid long term supply assurance and focus limited budgets on innovation, not duplication.

BREAK **(3:10–3:30)**
Ballroom Foyer

ELECTRONICS FOR G-BAND ARRAYS (ELGAR)

Wednesday, March 20 / 1:30 – 3:10 pm / Ballroom B

Chair: **Thomas Kazior**
DARPA MTO, Arlington, VA

Co-Chair: **Sharon Woodruff**
Booz Allen Hamilton, Washington, DC

23.1: Efficient GaN Integrated G-band Monolithic Arrays **(1:30)**

Jonathan Roderick, George Siddiqi, Jonathan Lynch, Dan Denninghoff, Daniel Berkoh, Joe Tai, Sunil Rao, Clayton Tu, Hasan Sharifi, Daniel Kuzmenko, Jana Georgieva, and James Krieger
HRL Laboratories, Malibu, CA

Warren McArthur, Seyed Sadreddin Mirshafieyan, Dave Howard
TowerSemi, Newport Beach, CA

23.2: Advanced 3D Heterogenous Integration (3DHI) for ELectronics for G-band ARrays (ELGAR) **(1:50)**

Augusto Gutierrez-Aitken, Vesna Radisic, Cedric Monier, Bill Deal, Max Duffy, KK Loi, Wesley Chan, Nancy Lin, Kevin Leong, Zhongzhong Dong, Xiang Zeng, Alex Poyneer, Gerry Mei, Xing Lan, Michael Eller, Mason Fordham, Dimas Pascua, Patrick Marshall, Reidly Yogi, Truong Minhdao
Northrop Grumman Corp., Redondo Beach, CA

Roger Quon, Ying Trickett, Eva Smith, Viet Nguyen
Applied Materials, Albany, NY

John Papapolymerou, John Albrecht, Matt Hodek
Michigan State University, East Lansing, MI

There are several challenges for high performance, high frequency multi-function 3DHI components, including active technology RF performance, interposer in-plane x-y connectivity, 3D z-connectivity, heterogeneous integration interfaces, thermal and mechanical stability. An additional challenge in high frequency electronic steering arrays (ESAs) is the area available for each array element, which is constrained by λ/2 spacing requirements. It is clear that a mix of advanced active technologies, heterogeneous integration stacking and optimum materials need to be used to achieve the required performance. In out approach we use advanced InP HBT and HEMT for the transmit and receive functions, respectively. These technologies have demonstrated high power added efficiency and low noise figure. For the antenna layer we use a low-K quartz substrate that enables wider bandwidth. The 3D stack up is integrated on a SiC interposer that offers excellent RF connectivity, thermal and mechanical performance.

23.3: Progress Towards Planar MMICs and Phased Arrays **(2:10)**

Jeffrey LaRoche, Brian Schultz, Nick Kolias, Clay Long, Eduardo Chumbes, Lovelace Soirez, Jason Milne, Amada Castro, David Crouch, Adam Peczalski, Charles Wang
Raytheon, Tewksbury, MA

Benjamin Powers, Haley Steffen
Collins Aerospace

David Howard
Tower Semiconductor

Robert Patti
NHanced Semiconductors

David Meyer, Virginia Wheeler, Brian Downey
Naval Research Laboratory

Harish Krishnaswamy, Moitreya Adhikary
Columbia University

Michael Elliott
Air Force Research Laboratory

23.4: Advanced InP Integrated Circuit and Integration Technologies for G-band Phased Arrays **(2:30)**

M. Urteaga, Z. Griffith, A. Young, J. Bergman, J. Hacker, P. Rowell, A. Papavasiliou, M. Gomez, A. Paniagua, D. Regan, K. Shinohara
Teledyne Scientific Company, Thousand Oaks, CA

M. Rodwell, J. Buckwalter
University of California Santa Barbara, Santa Barbara, CA

M. Lueck, K. Morris
Micross Advanced Interconnect Technology (AIT), Research Triangle Park, NC

23.5: Millimeter-Wave On-Wafer Measurement Support for the DARPA ELGAR Program **(2:50)**

Jerome Cheron
National Institute of Standards and Technology, Boulder, CO and University of Colorado Boulder, Boulder, CO

Ari Feldman, Jeffrey Jargon
National Institute of Standards and Technology, Boulder, CO

Antonio Crespo, Paul Watson
Air Force Research Laboratory Sensors Directorate, Wright-Patterson AFB, OH

Michael Elliott, Ryan Gilbert
KBR, Inc., Beavercreek, OH

BREAK **(3:10–3:30)**
Ballroom Foyer

ADVANCES IN NEXT GENERATION MICROELECTRONICS

Wednesday, March 20 / 1:30 – 2:50 pm / Ballroom C4

Chair: **Mona Massuda**
Department of Defense, Fort Meade, MD

Co-Chair: **Marcia Sawhney**
Department of Defense, Fort Meade, MD

24.1: The First CMOS-Integrated Voltage-Controlled MRAM with sub-1 ns Switching Time **(1:30)**

Haris Suhail, Haoran He, Jiyue Yang, Vinod Kurian Jacob, Qingyuan Shu, Puneet Gupta, Kang L. Wang, Sudhakar Pamarti
University of California, Los Angeles, CA

24.2: Magnetic Sensing with Silicon Vacancies in Isotopically-Purified Silicon Carbide **(1:50)**

I. Lekavicius, R. Myers-Ward, D. Pennachio, S. T. White, J. R. Hajzus, A. P. Purdy, A. L. Yeats, T. L. Reinecke, E. R. Glaser
Naval Research Laboratory, Washington, DC

S. G. Carter
Laboratory for Physical Sciences, College Park, MD

We describe improved sensitivity of a magnetic sensor system based on an ensemble of silicon vacancies in silicon carbide. The use of an isotopically purified host crystal leads to a maximum sensitivity an order of magnitude better than the best previously reported values.

24.3: Aligned Carbon Nanotubes for Advanced Radiofrequency Devices **(2:10)**

Katherine R. Jinkins
SixLine Semiconductor, Inc., Middleton, WI

Michael S. Arnold
SixLine Semiconductor, Inc., Middleton, WI
and
University of Wisconsin-Madison, Madison, WI

Sean M. Foradori
University of Wisconsin-Madison, Madison, WI

Radiofrequency (RF) devices are crucial electronic components used in defense applications, such as radar, secure wireless communication, and weapon guidance. The next generation of RF devices will require access to higher frequencies at lower power while minimizing size, weight, and power (SWAP). Carbon nanotubes (CNTs) are expected to offer significant performance and integration gains as the semiconducting channel of RF devices, such as low-noise amplifiers. When organized and aligned into arrays, semiconducting CNTs can exhibit superior RF characteristics, including high frequency and linearity, which are vital for next-generation communication. CNTs can also be deposited at room temperature onto almost any substrate, enabling smaller devices with opportunities for unusual form-factors or mechanical flexibility. Devices based on aligned CNTs are critical to maintaining superior RF performance globally. In this article, we discuss CNT alignment techniques that produce highly aligned arrays of semiconducting CNTs to meet the needs of next-generation RF performance.

24.4: Delay Generation Based on Differential Sawtooth Waveforms for 3-D Heterogeneous Integration **(2:30)**

Andres Ayes, Eby G. Friedman
University of Rochester, Rochester, NY

Emerging technologies in the semiconductor industry, such as three-dimensional (3-D) integration and sub-10 nm technology nodes, have revolutionized the next generation of microelectronic systems. Deeply scaled systems demand both coarse and precise, compact delay elements for applications such as time-to-digital conversion (TDC), digital timers, and phase compensation. A sawtooth waveform-based delay generation technique for periodic clock signals is proposed here to produce large, high resolution delays within a compact area. The technique uses a differential sawtooth waveform to extract delay information from the input signal. This approach is a natural match for heterogeneous 3-D integration because it is highly tolerant to process, voltage, and temperature (PVT) variations and exploits through silicon via (TSV) embedded capacitors.

BREAK **(3:10–3:30)**
Ballroom Foyer

DATA PROTECTION IN VIRTUAL ENVIRONMENTS (DPRIVE)

Wednesday, March 20 / 1:30 – 3:10 pm / Ballroom C1-3

Chair: **Bryan Jacobs**
DARPA MTO, Arlington, VA

Co-Chair: **Johnny Marsh**
DARPA MTO SETA, Arlington, VA

25.1: DPRIVE Introduction (1:30)

Bryan Jacobs
DARPA, Arlington, VA

Introductory talk to the session.

25.2: BASALISC: Programmable Hardware Accelerator for BGV and CKKS FHE (1:50)

Daniel Wagner, James LaMar, Ben Selfridge, David W. Archer
Galois, Inc., Portland, OR

Georgios Dimou, Tynan McAuley
Niobium Microsystems, Dayton, OH

Robin Geelen, Michiel Van Beirendonck, Hilder V. L. Pereira, Ingrid Verbauwhede, Frederik Vercauteren
COSIC, KU Leuven, Leuven, Belgium

25.3: TREBUCHET Fully Homomorphic Encryption Accelerator: Lessons Learned at Tape-out ... So Far (2:10)

Matthew French, Ajey Jacob, Benedict Reynwar, Kellie Canida, Clynn Mathew
USC, Information Sciences Institute, Arlington, VA

David Bruce Cousins, Ahmad Al Badawi
Duality Technologies, Hoboken, NJ

Austin Ebel, Negar Neda, Deepraj Soni, Brandon Reagen
New York University, New York, NY

Zeming Chen, Massoud Pedram
University of Southern California, Los Angeles, CA

Fully Homomorphic Encryption (FHE) is a cryptographic technology that keeps data encrypted during computation, even in untrusted environments. However, FHE requires significant computer power compared to similar operations on unencrypted data. The TREBUCHET project is developing a hardware accelerator for deep FHE machine learning applications, under the DARPA MTO Data Privacy for Virtual Environments (DPRIVE) program. Our goal is to close this computation gap to within 10×, making encrypted processing practical for everyday use. We integrate with the OpenFHE library and accelerate its standard FHE schemes. This paper is an update with lessons learned as we close our highly parallel chip design for final tape-out on an 150 mm^2 design on GF 12LP.

25.4: TREBUCHET Fully Homomorphic Encryption Accelerator: Phase Two Performance Estimation Results **(2:30)**

David Bruce Cousins, Yuriy Polyakov, Ahmad Al Badawi
Duality Technologies, Inc., Hoboken, NJ

Matthew French, Andrew Schmidt, Ajey Jacob, Bene-dict Reynwar, Kellie Canida, Akhilesh Jaiswal, Clynn Mathew
USC, Information Sciences Institute, Arlington, VA

Austin Ebel, Negar Neda, Brandon Reagen
New York University, New York, NY

Naifeng Zhang, Franz Franchetti
Carnegie Mellon University, Pittsburgh, PA

Patrick Brinich, Jeremy Johnson
Drexel University, Philadelphia, PA

Mike Franusich
SpiralGen, Inc., Pittsburgh, PA

Bo Zhang, Zeming Cheng, Massoud Pedram
University of Southern California, Los Angeles, CA

25.5: Intel HERACLES: Homomorphic Encryption Revolutionary Accelerator with Correctness for Learning-oriented End-to-End Solutions **(2:50)**

Rosario Cammarota, Suvadeep Banarjee, Flavio Berghamaschi, Jeremy Bottleson, Jeremy Casas, Jack Crawford, Hubert de Lassus, Huijing Gong, Lalith Kethareswaran, Duhyeong Kim, Hamish Hunt, Raghavan Kumar, Poornima Lalwaney, Sanu Mathew, Kylan Race, Ernesto Ramos, Fillipe Souza, Michael Steiner, Vasantha Srirambhatla, Sachin Taneja, Anupam Golder, Adish Vartak, Wen Wang, Chris Wilkerson, Jin Yang
Intel Labs, Santa Clara, CA

Intel HERACLES is a novel near-memory computer architecture with tightly connected functional units and distributed memory, that accelerates FHE programs through the native execution of ring polynomial arithmetic. Intel is developing HERACLES in the DARPA DPRIVE program. HERACLES supports features such as on-line twiddle factor generation and key-switching material generation to reduce the overhead of meta-data movement for critical NTT/iNTT and key-switching operations. HERACLES delivers massive speedup relative to a state-of-the-art data center CPU. HERACLES is fully implemented in RTL. Emulated performance show that it can deliver 11,000× better NTT latency for log q = 128, N = 64 K and within <8 W, and 9,300× better latency for a Logistic Regression Training task. Lastly, the hardware and software components are formally verified to ensure end-to-end correctness. The estimated chip area is 200 sq mm in Intel3.

BREAK **(3:10–3:30)**
Ballroom Foyer

ADVANCED POWER ELECTRONICS

Wednesday, March 20 / 1:30 – 3:10 pm / Room 6/7

Chair: **Fritz Kub**
Naval Research Laboratory, Washington, DC

Co-Chair: **Travis Anderson**
Naval Research Laboratory, Washington, DC

26.1: Power Devices for Improved Grid Control, Resilience, and Reliability (1:30)

Olga Blum Spahn
U.S. Department of Energy, Washington, DC

Igor Cvetkovic, Eric Carlson, Chelsea Haughn
Booz Allen Hamilton, Washington, DC

Technological advances in power electronics have enabled unprecedented growth of renewable energy sources in the electrical power grid. Power electronics bring significant improvements in grid control and performance that are fundamentally changing the nature of the grid. Decarbonization efforts rely on the electrification of everything from transportation to industrial processes, causing a dramatic increase in demand for electricity. Power electronics have the potential to minimize the increased demand, but new approaches are needed to improve the performance and actuation speeds. ARPA-E has an extensive power electronic portfolio with significant efforts in key technology enablers to improve grid control, resilience, and reliability. The ARPA-E Unlocking Lasting Transformative Resiliency Advances by Faster Actuation of power Semiconductor Technologies (ULTRAFAST) program seeks to advance the performance limits of silicon, wide bandgap, and ultra-wide bandgap semiconductor devices and significantly improve their actuation methods to support a more capable, resilient, and reliable future grid.

26.2: Radiation Hard Low Voltage Point-of-Load Switch Mode Power Converters (1:50)

Andrew Armstrong, Rafmag Cabrera, Albert Colon, Brianna Klein, Matt McDonough, Jason C. Neely, Greg Pickrell
Sandia National Laboratories (SNL), Albuquerque, NM

26.3: SiC Superjunction Switches for Next Generation of Power Converters (2:10)

Reza Ghandi
GE Research Center, Niskayuna, NY

In this paper, we present recent progress on two complementary technologies in SiC Medium-Voltage (MV) power devices. These technologies include charge-balanced (CB) and deep-implanted vertical-pillar superjunction (SJ) structures, which serve as two scalable alternatives to conventional superjunction technologies, including multi-epitaxial growth and trench-refill. We review the fabrication steps for >3 kV SiC CB and SJ diodes and MOSFETs, with a particular emphasis on implementations using high-energy (MeV) implantations. We will summarize the static and switching characterization results at both room and elevated temperatures and report on the experimental demonstration of SiC switches with a specific Ron below the SiC unipolar limit. These switches can enable the next generation of MV power converters and can replace MV unipolar SiC switches with limited performance at higher frequencies.

26.4: Analytical Determination of Unipolar Diode Losses in Power Switching and Perspective for Ultra-Wide Bandgap Semiconductors **(2:30)**

Nolan S. Hendricks, Joshua J. Piel, Ahmad E. Islam, Andrew J. Green
Air Force Research Laboratory, Wright-Patterson AFB, OH

26.5: Enhancing Electrical Insulation of Medium-Voltage Power Modules by a Nonlinear Resistive Polymer Nanocomposite Coating **(2:50)**

Zichen Zhang, Khai D.T. Ngo, Guo-Quan Lu
Virginia Tech, Blacksburg, VA

Medium-voltage silicon carbide power modules are being evaluated for more compact and efficient power conversion in grid-tied applications. However, the challenge of module insulation is slowing the technological progress. This paper offers an overview of an insulation enhancement solution: field-grading by a nonlinear resistive coating of a polymer nanocomposite. Applying a thin layer, about 15 microns thick, of the polymer nanocomposite at the triple points inside the module can reduce the local electric field stress by about 50%, resulting in an increase of measured partial discharge inception voltage by more than 80%. The insulation enhancement remains effective at 200 °C. Moreover, the coating-enhanced insulation of a SiC MOSFET module enables the device to switch at >300 V/ns under 10 kV, the fastest medium-voltage operation of a SiC device. These results strongly support the polymer nanocomposite coating as a promising solution to overcome the insulation challenge of medium-voltage power modules.

BREAK **(3:10–3:30)**
Ballroom Foyer

Wednesday, March 20 / 1:30 – 3:10 pm / Room 10/11

BREAK **(3:10–3:30)**
Ballroom Foyer

DIGITAL ACCELERATORS AND VERIFICATION

Wednesday, March 20 / 3:30 – 5:10 pm / Ballroom A

Chair: **Abirami Sivananthan**
InQTel, Arlington, VA

Co-Chair: **Saverio Fazzari**
Booz Allen Hamilton, Washington, DC

27.1: Edge Super Compute (ESC) 2.0 – A Low Power System-on-Chip AI Accelerator for the Edge (3:30)

Jamal L. Molin, Sergio Montano, Arnaldo J. Noyola, Michelle A. Williams, Thomas Janowski, Sida Zhou, Bingxin Tian, Peter J. Mackus, Bouchaib Cherif, Kayode Sanni, Doyle T. Nichols, Isidoros Doxas, Nishant Zachariah
Northrop Grumman, Linthicum Heights, MD

Philippe O. Pouliquen, Michael Tomlinson, Daniel R. Mendat, Andreas G. Andreou
Johns Hopkins University, Baltimore, MD

State-of-the-art defense systems requiring low computational power consumption and high data throughput for on-the-edge processing (e.g., drones, wearables) are limited by traditional von-Neumann architectures. Advanced sensors generate large volumes of data, which must be ingested and intelligently processed for data reduction and time-critical, intelligent decision-making. Traditional architectures require data movement between memory and processing units, which has a high energy and latency cost. We present our next generation compute-in-memory (CIM) based system-on-chip (SoC), Edge Super Compute (ESC) 2.0, implemented in 12 nm FinFET technology. ESC 2.0 is an enhanced version of the prior ESC chip. It is capable of highly parallel, low power multiply-accumulate (MACC) operations — applicable to military tasks including AI, radar, and image processing. ESC 2.0 consumes 28.6 fJ per 1-bit MACC at a throughput of 6.7 TOPS on a single 8 mm × 8 mm chip, and 1.83 pJ per 8-bit MACC at a throughput of 104.6 GOPS.

27.2: A Convolutional Neural Network Mapping Enabling an All Digital Synthesizer (3:50)

Chris M. Thomas
Boeing BR&T, Huntington Beach, CA

Luke McCubbin, Rod DiCiro, Liang Dong, Vincent Leung
Baylor University, Waco, TX

A convolutional neural network architecture is proposed to control an All-Digital-to-RF synthesizer (12 nm FinFet CMOS) intended for digital beamformer arrays. Each channel of the synthesizer has an expansive control space, in the order of $2^{28} \times 4$ for I/Q, and exhibits a highly non-linear response to the control code. A control vector mapping to grey-thermometer encoding is proposed to characterize the control state-space by a convolutional neural network architecture. The result produced a 1.44° RMS prediction error with only 0.01% of the input state space as a training set. The proposed approach enables reduced chip measurement characterization and highly non-linear all-digital (inverter based) synthesizer array control.

27.3: Industry Trends in Functional Verification: A Quantitative Analysis **(4:10)**

Harry Foster
Siemens EDA, Plano, TX

This paper unveils the outcomes of a comprehensive two-decade-long double-blind industry study focusing on the functional verification of Application-Specific Integrated Circuit (ASIC) and Field-Programmable Gate Array (FPGA) designs. The insights derived from this extensive research endeavor shed light on a myriad of pressing challenges, notably the growing prevalence of bug escapes into production and the persistent issue of missed project schedules. In conclusion, we offer valuable insights and strategies for mitigating these trends, providing a roadmap towards enhanced verification practices and more reliable product development processes.

27.4: Trusted IP through Automated Attestation – A Secure IP Repository Concept **(4:30)**

Serge Leef
Microsoft Corporation, Redmond, WA

Warren Savage
Rocksavage Technology, Inc., Campbell, CA

Access to high-quality semiconductor intellectual property cores (IP) is essential to modern System-on-Chip (SoC) design. However, the commercial market for IP is highly fragmented, dominated by a few large companies and hundreds of smaller ones. This supply chain represents a significant challenge for government customers who need to utilize commercial-grade technology for use in their secure designs. We propose a concept for a Secure IP Repository that allows government agencies and their subcontractors to access a curated set of IPs that has been instrumented such that the provenance of each IP can be tracked from a supplier through its instantiation in an SoC. Additional security protections such as watermarking, mitigations against hardware trojan insertion, and quantification of side-channel leakage can be performed automatically at cloud-scale as optional features available to users.

27.5: One Billion Point FFT at 4 GSPS Using FPGA **(4:50)**

Michael Parker
Raytheon Technologies, El Segundo, CA

Michael Cervantes
Raytheon Technologies, Tewksbury, MA

Edwin Lee, Ben Plotner
Raytheon Technologies, Hanover, MD

Wednesday Evening Social **(6:30–10:30)**
South Carolina Aquarium

Session 28 (RF Technologies, Components, and Systems)

RF SYSTEM APPLICATIONS

Wednesday, March 20 / 3:30 – 5:10 pm / Ballroom B

Chair: **Mark Yeary**
Advanced Radar Research Center (ARRC) at the University of Oklahoma, Norman, OK

Co-Chair: **Adilson Cardoso**
Raytheon, Atlanta, GA

28.1: Enabling mm-Wave 5G Joint Communication and AI-based Sensing for Urban Situational Awareness (3:30)

Arun Paidimarri, Asaf Tzadok, Sara Garcia Sanchez, Atsutse Kludze, Alexandra Gallyas-Sanhueza, Alberto Valdes-Garcia
IBM T.J. Watson Research Center, Yorktown Heights, NY

We present an antennas-to-AI platform for joint communication and sensing. It leverages the hardware and processing required for standard mm-Wave 5G communications to perform sensing tasks. It's key capabilities and metrics include (i) synchronization of I/Q data (up to 200 MSPS) with beam steering (among 9601 beams) with 10ns accuracy; (ii) a signal processing pipeline that extracts communication features such as the SNR and channel response from received 5G waveforms; and (iii) system orchestration that synchronizes the receiver (RX) to the 5G frame structure of the base station (gNodeB) and maintains it within a worst-case OFDM cyclic prefix of 0.29 µs. The platform is also able to emulate gNodeB transmissions. We demonstrate AI-based object classification only using the directional communication features derived by the platform from ambient 5G signals transmitted by a gNodeB. Six objects are classified with 98% accuracy in an indoor environment.

28.2: Arrays at Commercial Timescales Generation 2.1 Common Module Characterization and Demonstration (3:50)

Peter Buxa, Kelly Cheung, Thomas Dalrymple, Kelly Darnell, Hunter Doster, Matthew Longbrake
Air Force Research Laboratory, Wright-Patterson AFB, OH

Richard Umbach
Matrix Research Inc., Dayton, OH

28.3: Flight Test Results for RFSoC-Based UAS Sensor Payload (4:10)

Jonathan Dixon, Nathan Blood, Nicholas Haglof, Nicholas Chillemi, James Martin
SI2 Technologies, Inc., an ARA Company, North Billerica, MA

Adam Propst, Jonathan Rasche, Anthony Jones, William Vourazeris
Platform Aerospace, Inc., Hollywood, MD

Kris Kim, Alex Burwell, Damon Kelly, Colin Beck, Karleigh Pine, Andrew Homan, Ken Ellzey
Matrix Research, Inc., Dayton, OH

Jay Weitzen
University of Massachusetts Lowell, Lowell, MA

28.4: Radio Disruption of Electronic Systems (4:30)

Glen Garner, Byron Byars, Josh Wetherington
Vadum, Inc., Raleigh, NC

Jordan Besnoff, David Ricketts
North Carolina State University, Raleigh, NC

28.5: Jamming Resilient 5G System Leveraging Commercial Hardware (4:50)

Karen Gettings, Iain Donnelly, Joshua Geyster, Paul Monticciolo, Matthew Rebholz, William Song
MIT Lincoln Laboratory, Lexington, MA

Wednesday Evening Social (6:30–10:30)
South Carolina Aquarium

Session 29 (RF Technologies, Components, and Systems)

RF TOOLS FOR MODELING, ANALYSIS, AND FABRICATION

Wednesday, March 20 / 3:30 – 4:50 pm / Ballroom C4

Chair: **Tony Quach**
Air Force Research Laboratory, Wright-Patterson AFB, OH

Co-Chair: **Steve Hary**
Air Force Research Laboratory, Wright-Patterson AFB, OH

29.1: State of the Art Heterogeneous Integrated Packaging (SHIP) RF Design Mixed Signal Flow (MSF) Validation Co-simulation of Electrical and Physical Parameters for Reduced Complex Microwave Packaging Development Cycle Time (3:30)

Matthew Poulton, Raj Pandey, Spencer Pace, Ehsan Hosseinzadeh
Qorvo, Richardson, TX

Paul Mosinskis, John Bennett
Cadence Design Systems, San Jose, CA

The DoD SHIP RF program provides the opportunity to develop highly integrated mixed function modules. The paper will describe the next generation of cosimulation design flow being developed under the SHIP RF program. The paper will describe the tool set, design flow from layout floor planning and schematic starting points, Assembly Design Kit (ADK) and cosimulation capabilities of the Mixed Signal Flow (MSF). Critically, under SHIP RF, the new design flow has been validated against real world multichannel microwave laminate module product designs. This paper includes comparisons to previous simulation results in other commercially available design tools and also to lab measured data.

29.2: Understanding Fab Variability Using a Full Physics-Based Compact Modeling Framework (3:50)

Jose Jimenez, Kirk Ashby, Gergana Drandova, Sourabh Khandelwal
Qorvo, Inc., Richardson, TX

Tony Quach, Bryan Sanbongi, Steven McKeown
Air Force Research Labs, Dayton, OH

Larry Dunleavy, Hugo Morales, Jiang Liu, Chris DeMartino
Modelithics, Inc., Tampa, FL

An innovative physics-based GaN compact modeling framework, funded by AFRL and developed by Qorvo and Modelithics, is introduced in this paper. The GaN framework is built upon a general ASM-HEMT core model with geometry and epi parameter wrapper which provides designers a new degree of freedom in terms of scaling foundry device geometry parameters far beyond gate-width scaling. It also provides finger level heating thermal model to account for self and remote heating effect and a degradation module with which one can perform aging simulations directly on a MMIC. This framework is exercised with historic process monitoring geometric and material measured data as input and Monte-Carlo analysis is performed on large signal simulation of the actual monitoring MMIC. This exercise helps to understand which of the geometrical and compositional variability dominates the MMIC performance and thus requires tighter control.

29.3: Thermal Performance in Broadband GaN MMIC Power Amplifiers **(4:10)**

Michael Litchfield
BAE Systems, Nashua, NH

Though thermal performance of GaN power amplifier (PA) MMICs is critical to module and system performance, only recently have design tools enabled consistent and quick thermal analysis of MMIC technology. BAE Systems has adopted the connection of Cadence Microwave Office and Cadence Celsius Thermal Solver through a custom GaN process design kit (PDK) to enable this capability. Insightful analysis, design improvements, and lessons learned have enabled significant improvements in peak junction temperature for GaN MMIC PAs: 4–18 GHz, 35 W non-uniform distributed power amplifier (NDPA), and 32–37 GHz, 35 W reactively matched power amplifier (RMPA).

29.4: Migrating a 28 GHz 5G mmWave PA from GF 45RFSOI to 22FDX Technology Using an AI Driven EDA Platform **(4:30)**

Shafi Syed, Mayuri Wanve
GlobalFoundries, Inc., Dallas, TX

Jignesh Patel
GlobalFoundries, Inc., Santa Clara, CA

Mayuri Wanve
GlobalFoundries, Inc., Bangalore KA, India

Neel Gopalan
Synopsys, Inc., Sunnyvale, CA

Priyanka Dadwal
Synopsys, Inc., Bangalore KA, India

Keith Lanier
Synopsys, Inc., Morrisville, NC

While AI/ML approaches have been shown to be successful for FinFet based logic migration, little has been published on migrating Analog/RF between device technologies and technology nodes. This task is exacerbated by the uniqueness of different CMOS analog/RF foundry technologies. In this paper, we propose a unique Artificial Intelligence (AI) based approach that enables fast migration of leading-edge Analog/RF designs between advanced specialty technology nodes. The novelty of this paper is that it demonstrates RF design migration across both device type (PDSOI/FDSOI) and technology (high resistance/bulk). It also demonstrates a more design efficient method that delivers the same or better performance.

Wednesday Evening Social **(6:30–10:30)**
South Carolina Aquarium

DESIGN OF SECURE SYSTEMS

Wednesday, March 20 / 3:30 – 5:10 pm / Ballroom C1-3

Chair: **Shawn Fetterolf**
Intel, Santa Clara, CA

Co-Chair: **Adam Kimura**
Battelle Memorial Institute, Columbus, OH

30.1: DEFENSER: Defense Framework for Secure Accelerator Sharing in Expeditionary Systems (3:30)

Arsalan Ali Malik, Emre Karabulut, Amro Awad, Aydin Aysu
North Carolina State University, Raleigh, NC

30.2: Designing a Hardware Root-of-Trust for Zero-Trust Mission Systems (3:50)

Michael Vai, Alice Lee, Eric Simpson, Huy Nguyen, Jeffrey Hughes, John Dean, Gabriel Torres, Jeffery Lim, Ben Nahill, Roger Khazan
MIT Lincoln Laboratory, Lexington, MA

Fred Schneider
Cornell University, Ithaca, NY

Zero-trust is a set of security principles that treats every component, service, and user of a system as continuously exposed to and potentially compromised by a malicious adversary. Through the implementation of compartmentalized access with continuous monitoring and adjustment, zero-trust is an effective approach for the development of mission-critical and safety-critical systems. In this paper, we describe our effort to address the challenges in the design of zero-trust mission systems using microelectronics with limited security features. In particular, we explain the ongoing development of a hardware root-of-trust that facilitates zero-trust system designs.

30.3: EDA Workflow for Optimization of Robust Model Probing-Compliant Masked Hardware Gadgets (4:10)

David S. Koblah, Domenic Forte
University of Florida, Gainesville, FL

Dev Mehta, Mohammad Hashemi, Fatemeh Ganji
Worcester Polytechnic Institute, Worcester, MA

Side-channel leakage allows attackers to compromise cryptographic systems by extracting sensitive information through signals inadvertently emitted by devices. Various types of side-channel signals, such as power consumption and electromagnetic emissions, can be used. To counteract side-channel attacks, masking has emerged as a means of protecting integrated circuits from probing and side-channel attacks. Masking techniques focus on secret sharing to enhance security. While Boolean masking has been commonly used for its simplicity, it doesn't defend against glitches that can expose sensitive data. However, glitch-resistant masking provides robust protection against glitches. This work focuses on optimizing and improving glitch-resistant, side-channel resilient designs, using technology mapping, retiming, and resynthesis to meet power, performance, and area constraints while maintaining security. The toolchain uses the above-stated methods to create secure and efficient designs. The security of the mask gadget outputs is verified using VERICA, a tool used to assess benchmark resilience against side-channel attacks.

30.4: Propelling Innovation to Defeat Data-Leakage Hardware Trojans: From Theory to Practice (4:30)

Kevin Kwiat
CAESAR Group, Sarasota, FL

Jason Kulick
Indiana Integrated Circuits, South Bend, IN

Paul Ratazzi
AFRL, Rome, NY

Many design companies have gone fabless and rely on external fabrication facilities to produce chips due to increasing cost of semiconductor manufacturing. However, not all of these facilities can be considered trustworthy; some may inject hardware Trojans and jeopardize the security of the system. One common objective of hardware Trojans is to establish side channel for data leakage. While extensive literature exists on various defensive measures, almost all of them focus on preventing the establishment of side channels, and can be compromised if attackers gain access to the physical chip and can perform reverse engineering between multiple fabrication runs. In this paper, we advance (from theory to practice) RECORD: Temporarily Randomized Encoding of COmbinational Logic for Resistance to Data Leakage. RECORD is a novel scheme of temporarily randomized encoding for combinational logic that, with the aid of Quilt Packaging, prevents attackers from interpreting the data.

30.5: Vulnerability of State Variable Filter and Switched Capacitor Filters to Self-oscillatory Mode of Operation (4:50)

Kwabena Oppong Banahene, Matthew Strong, Bryce Gadogbe, Degang Chen, Randall Geiger
Iowa State University, Ames, IA

Vulnerability of some widely used filter structures to an undesired non-destructive stationary nonlinear mode of oscillation is discussed. This undesired mode of operation can be very difficult to detect during design, verification, and testing, yet when triggered the filter operation ceases until power is cycled to resume normal operation. The major non-linearities that cause this undesired mode of operation is also discussed.

Wednesday Evening Social (6:30–10:30)
South Carolina Aquarium

GaN POWER ELECTRONICS

Wednesday, March 20 / 3:30 – 4:50 pm / Room 6/7

Chair: **Travis Anderson**
Naval Research Laboratory, Washington, DC

Co-Chair: **Fritz Kub**
Naval Research Laboratory, Washington, DC

31.1: High-Current (390 A) Large Area Vertical GaN PN Diodes with 1600 V Breakdown (3:30)

Luke Yates, Andrew Binder, Anthony Rice, Andrew Armstrong, Jeffrey Steinfeldt, Michael Smith, Richard Floyd, Andrew Allerman, Robert Kaplar
Sandia National Laboratories, Albuquerque, NM

Due to defects present in gallium nitride (GaN) epitaxial layers, the development of large area devices that are capable of >100 A current conduction and low leakage breakdown has been challenging. In this work, we will discuss recent efforts to utilize metallic interconnects to allow for the paralleling of vertical GaN diodes that achieve significant pulsed forward conduction while maintaining a low leakage, high voltage breakdown. Forward pulsed conduction of 390 A was achieved for a 13.85 mm^2 vertical GaN PN diode with a 1600 V reverse breakdown.

31.2: Demonstration of Planar 1.2 kV and 3.3 kV Vertical GaN PiN Diode High-Yield Manufacturing (3:50)

Alan G. Jacobs, James C. Gallagher, Jennifer K. Hite, Nadeem A. Mahadik, Karl D. Hobart, Travis J. Anderson
U.S. Naval Research Laboratory, Washington, DC

James S. Lundh
National Research Council, Washington, DC

Robert J. Kaplar
Sandia National Labs, Albuquerque, NM

31.3: Examination of Hybrid Edge Termination on Vertical GaN Planar MOSFETs (4:10)

Tolen Nelson, Prakash Pandey, Daniel G. Georgiev, Raghav Khanna
University of Toledo, Toledo, OH

Alan G. Jacobs, Andrew D. Koehler, Karl D. Hobart, Travis J. Anderson
U.S. Naval Research Laboratory, Washington, DC

James Spencer Lundh
National Research Council Postdoctoral Fellow Residing at U.S. Naval Research Laboratory, Washington, DC

Vertical GaN planar MOSFETs formed on epitaxial grown p-n--n+ wafers are examined in simulation. The n-type plug and source depositions are modeled and designed considering ion implanted Silicon counter-doping. The hybrid termination consisting of superimposed guard ring on a junction termination extension is validated through fabrication of 1350 V vertical GaN diodes and utilized for terminating the peripheral MOSFET p-n junction. The effect of the geometry of the MOSFET on breakdown voltage and on-resistance is examined. It is shown using double pulse test mixed-mode simulations that devices terminated with the hybrid edge termination have lower switching losses than those terminated with an equivalent width, ideal planar termination.

31.4: The Effects of Hole Transport on Super-Heterojunction FET Switching Time (4:30)

Jesse T. Kemmerling, Rongming Chu
Pennsylvania State University, University Park, PA

While GaN Super-heterojunction (SHJ) MOSFETs have been demonstrated experimentally with 10 kV blocking voltage and mitigated current collapse switching at 3 kV, there is a lack of understanding of the device switching behavior. The SHJ length scalable for larger blocking voltage comprises of an Mg-doped p-GaN layer, known for low hole mobility, and Si-doped δ-doping layer. TCAD simulation of a simple Schottky-gate SHJ-FET shows low hole mobility can increase turn-on time significantly, into the micro-second-range, with minimal impact on turn-off time. Long SHJ length design for high voltage capability have longer turn-on time; however, no effect on turn-off time is present due to depletion behavior of low-mobility holes.

Wednesday Evening Social (6:30–10:30)
South Carolina Aquarium

LEVERAGING STARTUP INNOVATION WITHIN THE DoD MICROELECTRONICS COMMUNITY PANEL

Wednesday, March 20 / 3:30 – 5:10 pm / Room 10/11

Wednesday Evening Social **(6:30–10:30)**
South Carolina Aquarium

THURSDAY, MARCH 21

Continental Breakfast, Ballroom Foyer **(7:30–8:30)**

Session 32 **(Packaging, Integration, Thermal and Control Technologies)**

STATE-OF-THE-ART HETEROGENEOUS INTEGRATION PACKAGING (SHIP)

Thursday, March 21 / 8:20 – 10:00 am / Ballroom A

Chair: **Brian Olson**
Department of the Navy Crane, Crane, IN

Co-Chair: **Saverio Fazzari**
Booz Allen Hamilton, Washington, DC

32.1: Building the State-of-the-Art Heterogenous Integrated Packaging (SHIP) Model **(8:20)**

Samuel Stark, Christopher Rice, Christopher Riso, Saverio Fazzari, Doug Palmer
Booz Allen Hamilton, Mclean, VA

Darren Crum, Brian Olson
U.S. Department of the Navy, Crane, IN

32.2: Stimulating Transition for Advanced Microelectronics Packaging **(8:40)**

Christopher Riso, Saverio Fazzari
Booz Allen Hamilton, Arlington, VA

Carmine Pagano, Ben Esposito, John Sotir
Intel Corporation, Parsippany, NJ

Darren Crum, Brian Olson
U.S. Department of the Navy, Crane, IN

32.3: Glass-Core Substrate Prototype for RF Systems-in-Package **(9:00)**

David Shahin, Matthew Doerflein, Andrew Cogliano, Michael Langlois, Sarah Woodworth
Northrop Grumman Mission Systems, Baltimore, MD

Kirk Ashby, Kevin Anderson, Anthony Chiu, Ajay Bodade, Lidia El Bouanani, Andrew Ketterson, Tarak Railkar
Qorvo, Inc., Richardson, TX

32.4: Validating Reliability Standards for Microelectronics Advanced Packaging in Military Applications **(9:20)**

Ryan Eames, Fernando Roa, Doug Palmer
Booz Allen Hamilton, McLean, VA

Laura Jean Weidman, Ruth Hidalgo-Hernandez, Aaron Clough-Paez
Department of Defense, Fort Meade, MD

Darren Crum, Brian Olson
U.S. Department of the Navy, Crane, IN

32.5: Strategic Transition of Microelectronics to Accelerate Modernization by Prototyping and Innovating in the Packaging Ecosystem **(9:40)**

Brian Olson, Darrick Korte, Darren Crum
U.S. Department of the Navy, Crane, IN

BREAK **(10:00–10:30)**
Ballroom Foyer

RF FILTERS AND CANCELERS

Thursday, March 21 / 8:20 – 9:40 am / Ballroom B

Chair: **Timothy Hancock**
Raytheon Technologies, Tewksbury, MA

Co-Chair: **Christal Gordon**
Booz Allen Hamilton, Arlington, VA

33.1: Ka/Ku-band Substrate Embedded Microscale Filters for Electronically Scanned Arrays **(8:20)**

Alexander B. Kozyrev
Collins Aerospace, An RTX Business, Cedar Rapids, IA

33.2: Broadband Metal Mode Magnetostatic Wave Filters for Enhanced Analog-to-Digital Converter Dynamic Range **(8:40)**

Augustine Kelty, David Connelly
Metamagnetics Inc., Marlborough, MA

33.3: An Autonomous Magnetostatic Based Frequency Selective Canceller **(9:00)**

Randy Camasso, Reena Dahle, Scott Gillette
Metamagnetics, Marlborough, MA

33.4: Compact, Mode-selective Magnetostatic-wave Resonators for mmWave Applications **(9:20)**

David Connelly, Augustine Kelty, Alexander Sokolov, Scott Gillette
Metamagnetics Inc., Marlborough, MA

Matthew Laurent, David Eaves, Nancy Lin, Dino Ferizovic
Northrop Grumman Corporation, Redondo Beach, CA

BREAK **(10:00–10:30)**
Ballroom Foyer

EXTREME WIDE BANDGAP TECHNOLOGY

Thursday, March 21 / 8:20 – 10:00 am / Ballroom C4

Chair: **Tony Ivanov**
Army Research Laboratory, Adelphi, MD

Co-Chair: **Nian Sun**
Northeastern University, Boston, MA

34.1: Attempts on WBG and UWBG Semiconductor Bipolar Devices (8:20)

Sang June Cho, Jisoo Kim, Dong Liu, Jie Zhou, Jiarui Gong, Donghyeok Kim, Moheb Sheikhi, Hokyung Jang, Haris Abbasi, Yang Liu, Yi Lu, Shubhra S Pasayat, Chirag Gupta, Zhenqiang Ma
University of Wisconsin-Madison, Madison, WI

Fikadu Alema, Andrei Osinsky
Agnitron Technology Inc., Chanhassen, MN

Clincy Cheung, Vincent Gambin
Northrop Grumann, Redondo Beach, CA

Timothy Grotjohn, John D. Albrecht
Michigan State University, East Lansing, MI

Zetian Mi
University of Michigan, Ann Arbor, MI

Tien Khee Ng, Boon S. Ooi
King Abdullah University of Science and Technology, Thuwal, Saudi Arabia

Jung-Hun Seo
University at Buffalo, The State University of New York, Buffalo, NY

Wide-band-gap (WBG) and ultra-wide-band-gap (UWBG) semiconductors are poised to revolutionize power electronics in the next generation. However, challenges persist due to the lack of effective dopants of both types and the difficulty in achieving bipolar devices via direct epitaxy growth. In response, this study adopts a novel approach: semiconductor grafting. By employing this technique, we successfully established PN junctions on GaN, β-Ga_2O_3, and diamond substrates. Notably, preliminary results of GaN-based and diamond-based heterojunction bipolar transistors are demonstrated. Our work pioneers WBG/UWBG semiconductor bipolar devices through the utilization of semiconductor grafting, offering promise for high-performance power electronic applications.

34.2: Dielectric Integration and Interface Defect Engineering for β-Ga_2O_3 MOS DSevices (8:40)

Ahmad E. Islam, Kevin D. Leedy, Kyle J. Liddy, Daniel Dryden, Kelson D. Chabak, Andrew J. Green
Air Force Research Laboratory, Dayton, OH

Aaron Arehart, Siddharth Rajan
Ohio State University, Columbus, OH

Guru Subramanyam
University of Dayton, Dayton, OH

Weisong Wang
Wright State University, Dayton, OH

We highlight the challenges for integrating dielectrics on β-Ga_2O_3, the associated requirements for the dielectric and dielectric/β-Ga_2O_3 interface and present our recent works on the electronic-grade integration of different dielectrics on β-Ga_2O_3.

34.3: Field Effect Transistors Based Upon the Emerging Wide Bandgap Semiconductor: $CaSnO_3$ (9:00)

Prafful Golani, Fengdeng Liu, Jiaxuan Wen, Steven J. Koester, Tristan K. Truttmann, Anusah Kamath Manjeshwar, Bharat Jalan
University of Minnesota, Minneapolis, MN

We report the demonstration of field-effect transistors (FETs) based upon the emerging ultra-wide bandgap semiconductor, $CaSnO_3$. High doping densities were achieved in these films grown by hybrid MBE with mobilities as high as 42 cm^2V/s at 3.3×10^{19} cm^{-3} carrier density. Metal-semiconductor FETs were fabricated, and devices with L_G = 3 µm showed on-off ratio >10^6 and remained operational at V_{DS} = 100 V. These results open the door to exploration of high-power applications of a new class of ultra-wide bandgap materials.

34.4: Impact of High Permittivity Dielectrics on Short Channel Effects in GaN HEMTs (9:20)

Joe F. McGlone, Siddharth Rajan
Ohio State University, Columbus, OH

An investigation of the impact of the high-k dielectric $BaTiO_3$ on short channel effects using TCAD simulations is done. The scaled devices indicate a parasitic channel in the buffer from source-to-drain punch through due to a lack of gate control and high fields in the buffer. The reduction in field due to $BaTiO_3$ field management is prevalent even in the buffer where the source-drain punch through is occurring. The $BaTiO_3$ layer is also found to improve the source-drain punch through with improved buffer designs utilizing an AlGaN buffer.

34.5: Manufacturing of High-Performance Crystalline Diamond for High-Technology Applications **(9:40)**

Paul Quayle, Ramón Diaz, Alex Grotjohn, Sandra Cita, Keith Evans
Great Lakes Crystal Technologies (GLCT), East Lansing, MI

Sergey Baryshev, Timothy A. Grotjohn
Michigan State University, East Lansing, MI

Great Lakes Crystal Technologies (GLCT) launched in August 2019 with a mission to become the leading provider of high-performance crystalline diamond materials for high-technology applications. This paper presents GLCT's analysis of the diamond materials requirements for a range of high-technology applications including quantum sensors, x-ray optics, high-energy particle detection, and ultra-high performance electronics. We present our progress towards meeting those requirements for select applications along with select elements of our crystalline diamond materials product and technology roadmaps.

BREAK **(10:00–10:30)**
Ballroom Foyer

TESTING AND ASSURANCE

Thursday, March 21 / 8:20 – 10:00 am / Ballroom C1-3

Chair: **Samson Melamed**
GLC Technologies, Inc., Owens Cross Roads, AL

Co-Chair: **Michael Wehrmeister**
Department of Defense, Fort Meade, MD

35.1: Independent Functional Testing for Intel Stratix 10 **(8:20)**

Travis Haroldsen, Ting-Yuan Sung, Osaze Shears
University of Southern California

Dallon Glick, Jay Danner
Georgia Institute of Technology, Atlanta, GA

35.2: Test Fixture De-embedding for Increased Measurement Accuracy in Second Order Effect Testing **(8:40)**

Casey Kauf
KBR, Inc., Beavercreek, OH
and
The Ohio State University, Columbus, OH

Carl Bohman, Aaron Jennings, Ryan Lachey
KBR, Inc., Beavercreek, OH

Jamin McCue, Christian Eakins
Air Force Research Laboratory, Wright-Patterson AFB, OH

35.3: Multi-Modal Approach Including X-Ray and SAM for Thorough Analysis of Advanced IC Packaging **(9:00)**

Patrick Craig, Nitin Varshney, Hamed Dalir, Navid Asadizanjani
University of Florida, Gainesville, FL

Charles Woychik
Skywater Technology Foundry, Kissimmee, FL

The semiconductor industry's advancements in advanced packaging and heterogeneous integration have outpaced traditional failure analysis and quality assurance capabilities. Existing non-destructive characterization methods face challenges regarding the small-scale interconnections and multi-layer stack structure of HI packaging. This paper explores the challenges in assuring the reliability of these heterogeneously integrated ICs and proposes a multi-modal approach combining Scanning Acoustic Microscopy and X-ray imaging for comprehensive analysis. SAM offers high-resolution acoustic imaging but faces difficulties in characterizing small-scale interconnects. Similarly, X-ray imaging provides advantageous resolution, but struggles with large sample sizes and long acquisition times. By combining these modalities, this research aims to bolster failure analysis and quality assurance for these up-and-coming technologies.

35.4: Navigating Microelectronics Quantifiable Assurance (MQA) for Custom Integrated Circuits (CIC) **(9:20)**

Robert Narumi, George Gerace
Raytheon, An RTX Business, El Segundo, CA

35.5: IP-Agnostic Foundational Cell Array Offering Tamper Resistance and Supply Chain Resilience **(9:40)**

Christopher Talbot, Deepali Garg, Lawrence Pileggi, Ken Mai
Carnegie Mellon University, Pittsburgh, PA

Supply chain disruption, high costs associated with low-volume production, and intellectual property (IP) security requirements of DoD applications preclude them from using advanced fabrication facilities. As such, the DoD largely depends on FPGAs. FPGAs, however, rely on software-programmed configurations, introducing mutability concerns and making them sub-optimal for many high-reliability applications. To mitigate these concerns, we propose an IP-agnostic Standard Cell Fabric (SCF) platform that can be re-targeted to multiple functions. Combined with existing split manufacturing techniques, the FEOL of this fabric can be mass-produced to stockpile offering supply chain resilience and semantically secure IP protection. SCF relies entirely on foundry-verified standard cells and industry-standardized EDA tools, for us to retain most of ASICs' power and performance benefits without the associated high NRE cost. We test our SCF design across various benchmarks under low-power and high-performance scenarios, to observe a worst-case power penalty of just 1.60× over standard cell ASIC.

BREAK **(10:00–10:30)**
Ballroom Foyer

CO-PACKAGED ANALOG-DRIVE HIGH-BANDWIDTH OPTICAL INPUT/OUTPUT (KANAGAWA)

Thursday, March 21 / 8:20 – 10:00 am / Room 6/7

Chair: **Joshua Hawke**
Naval Surface Warfare Center – Crane Division, Crane, IN

Co-Chair: **Dmitry Kozak**
Naval Surface Warfare Center – Crane Division, Crane, IN

36.1: **Integrated 2-Terabit-per-second Silicon Photonics Optical I/O Chiplet for Co-Packaging** **(8:20)**

Thomas Liljeberg, Saeed Fathololoumi, David Hui, Christian Malouin, Reece A. Defrees, Yen-Jung Chen, Kadhair Al-hemyari, Ankur Agrawal, Zhe Xuan, Preston T. Myers, Ling Liao
Intel Corporation, Santa Clara, CA

36.2: **Optical Assembly Challenges and Opportunities in Silicon Photonics Optical I/O Chiplets** **(8:40)**

Chong Zhang, Nhat Nguyen, Soumen Karmakar, Li-Fan Yang, Jianhua Li, Bob Paddison, Steve McGowan, Chen Sun, Mark Wade
Ayar Labs, Inc., Santa Clara, CA

36.3: **Advancements in Co-Packaged Optics Technology – Integrated Optical I/Os and FPGAs for New Platform Architectures** **(9:00)**

John Oh, Allen Chan, Sergey Shumarayev, Saikumar Jayaraman, Kumar Abhishek Singh
Intel Corporation, Santa Clara, CA

Vladimir Stojanovic, Mark Wade
Ayar Labs, Inc., Santa Clara, CA

36.4: **Co-packaged Optics for RF Sensor Applications** **(9:20)**

Tarak A. Railkar, Kevin J. Anderson, Dennis Quaintance, Joshua Hinz, Walid M. Meliane, Craig Steinbeiser, Kurt Cimino, Jeffrey Miller
Qorvo, Richardson, TX

Ted Hoffmann, Jack Holloway
Raytheon Company, Arlington, VA

Thomas Liljeberg, Sang Yup Kim
Intel Corporation, Santa Clara, CA

Co-packaged optics (CPO) is emerging as a new class of microelectronics which promises to transform the methods in which RF signals are digitized, processed, and transported between compute elements for future sensor systems. Through the Office of the Under Secretary of Defense (OUSD) Co-Packaged Analog-Drive High Bandwidth Optical Input/Output (KANAGAWA) program, and in harmony with the State of the Art (SOTA) Heterogeneous Integrated Packaging (SHIP) RF program, Qorvo and our partners have initiated efforts to establish compelling CPO technology and products to serve USG needs through a domestically sourced commercially viable manufacturing supply chain.

36.5: Edge and Distributed Computing (EDC) Enabled by Co-Packaged Optics (CPO) (9:40)

Michael T. Hoff, Isaac C. Leffler, Patrick D. Zarnas, Garrett H. Tan, Harsha N. Torke, Rick C. Stevens
Lockheed Martin, Eagan, MN

This paper proposes that critical Edge and Distributed Computing (EDC) necessary for coordinated, distributed, real-time decisions and actions across a dynamic and heterogeneous battle space will depend on a large amount of information movement. This information movement will be enabled by Co-Packaged Optics (CPO). However, for broad adoption of CPO-based architectures by the Defense Industrial Base (DIB), the following openly available characteristics are critical: 1) an electrical chiplet interface that is applicable to a variety of interposer solutions, 2) an optical interface standard ensuring interoperability and multiple sources, 3) a fiber attach process that is suitable to a variety of Photonic Integrated Circuit (PIC) designs, and 4) packaging and thermal solutions applicable to various CPO designs.

BREAK (10:00–10:30)
Ballroom Foyer

POSTER SESSION

Thursday, March 21 / 10:30 am – 12:00 pm / Exhibit Hall

Emerging Technologies Posters

P.1: Bio-Inspired Hyperdimensional Intelligent Sensing

Sanggeon Yun, Hanning Chen, Mohsen Imani
University of California Irvine, Irvine, CA

Defense applications often analyze collected sensor data using machine learning algorithms. Unfortunately, the existing sensing systems lack intelligence about the target and naively generate large-scale data, making communication and computation significantly costly. However, in many cases, the data generated by sensors only contain useful information for a small portion of the sensor activity. For example, machine learning algorithms continuously process the visual sensors used for environmental/security monitoring to detect sensitive activities. Still, these sensors only carry out useful information for a short time. On the other hand, biological sensors intelligently generate orders of magnitude less amount of data. In this project, we develop brain-inspired learning algorithms that provide real-time feedback to sensors to ensure they only generate data needed for learning purposes. This feedback also enables an attention mechanism that makes sensors aware of the target task, enabling situational awareness. We also develop a novel framework that tightly integrates with a sensing circuit and brain-inspired algorithms to dynamically control the sensor functionality in a fully self-supervised manner. Our approach is providing up to four orders of magnitude data reduction from sensors. The results from this research will broadly impact many sensors used in DoD applications, including national security, energy management, infrastructure, and autonomous systems.

P.2: Reliable Hyperdimensional Reasoning on Unreliable Emerging Technologies

Hamza Bakram, Sanggeon Yun, Hanning Chen, Mohsen Imani
University of California Irvine, Irvine, CA

While Graph Neural Networks (GNNs) have demonstrated remarkable achievements in knowledge graph reasoning, their computational efficiency on conventional computing platforms is impeded by the memory wall problem. To overcome these challenges, we introduce an innovative algorithm-hardware solution that harnesses the potential of hyperdimensional computing (HDC) for robust and memory-centric computation on computing in-memory (CiM) platforms. Departing from traditional graph neural networks, the proposed HDC reasoning model employs a symbolic approach to effectively encode graph entities and their relationships as high-dimensional neural activity. Complementing this approach is a customized Computing-in-Memory (CiM) architecture based on advanced Ferroelectric Field-Effect Transistor (FeFET) technology, which incorporates a precise characterization of non-idealities. This modeling enables the generation of an HDC-tailored model that faithfully represents the hardware architecture. Despite the non-idealities inherent in emerging CiM technologies, our platform demonstrates performance on par with traditional von Neumann architectures for substantial combinations of FeFET device parameters. Our solution overcomes FeFET CiM the increased non-idealities from down-scaled 3 nm, operating effectively under all possible configurations when 50 graph edges are considered. Scenarios with less than 4-bit precision per FeFET device cannot handle graphs with more than 200 edges, whereas the 4-bit case can achieve a 90.3% graph reconstruction rate on the worst-case scenario of 80% of noise.

P.3: Plasmonic Resonances of Ge Nanoparticles in ZnO Matrix

Michael Shur
Rensselaer Polytechnic Institute, Troy, NY

Alexander L. Efros
Naval Research Laboratory, Washington, DC

The ZnO-Ge nanodot materials system is a unique combination of wide band gap and narrow band gap materials enabling photoresponse in a wide wavelength range. The polarization of Ge nanodots in the wurtzite ZnO matrix leads to the appearance of electron and hole droplets oscillating with plasmonic resonant frequencies in the terahertz (THz) or far-IR range. The resulting THz or far-IR response greatly extends the wavelength bandwidth of the ZnO-Ge optoelectronic devices enabling unique applications in photodetectors, sensors, THz detectors and emitters, and optical to THz conversion for fiber-6G communication links. ZnO matrix will respond to visible and near UV, which could be further extended to UV using the FIN lasing heterostructures.

P.4: Creating a Guiding State for the Cascaded Variational Quantum Eigensolver Using Highly Discretized Adiabatic State Preparation

John P. T. Stenger, Daniel Gunlycke, C. Stephen Hellberg
U.S. Naval Research Laboratory, Washington, DC

Elizabeth Lee
U.S. Naval Academy, Annapolis, MD

In this work, we explore the effectiveness of using highly discretized adiabatic state preparation to produce the guiding state for use in the cascaded variational quantum eigensolver (CVQE) algorithm. The CVQE algorithm is unique in that it requires only a single run of the quantum computer, after which the optimization is performed classically. Because the quantum computer is only run once, we need to ensure that a guiding state is generated that has a non-exponentially small overlap with the ground state. It is known that a full adiabatic state preparation can find the ground state exactly. However, the full adiabatic state preparation is too costly for present day quantum computers. Therefore, we reduce the cost of the state preparation by allowing for high discretization.

P.5: Scalable Compute Platform for Sensor Processing

Ian Land
Synopsys, Inc., Sunnyvale, CA

Michael Parker
Raytheon Technologies, El Segundo, CA

DoD applications must continue to push the state-of-the-art (SOTA) SWaP while advancing system performance for sensor processing. A scalable Vector Processor (VP) based compute platform can be created to deliver ASIC-like performance/power while incorporating FPGA-like hardware flexibility. This paper presents a study of key processors and assesses the strengths and challenges where a vector-engine based platform can deliver capabilities beyond the traditional methods that leverage FPGAs, while adding in AI acceleration and considering multiple sensors, sensor fusion, and strategic applications.

P.6: Closed-Form Continuous-Time Neural Network Circuit Models for Transient Simulation

Byron Byars, Glen Garner, Zach Coleman, Nikhil Kriplani
Vadum, Inc., Raleigh, NC

Derek Hockenberry, Rhett Davis
North Carolina State University, Raleigh, NC

Surrogate modeling is the process of creating a lightweight and rapid approximation of a compute-expensive system such as physics-based models of nonlinear RF circuit components. While high-dynamic range transient analysis of circuits represents the most accurate approach to simulating nonlinear phenomena in RF circuits, the simulations tend to be time consuming. In this work, closed-form continuous-time neural networks are used to create stable and general-purpose surrogate models of RF devices. The surrogate modeling process will enable multiple rapid executions of a circuit aided by machine-learning approaches to rigorously characterize modern, complex RF circuit performance more rapidly and accurately than current state-of-the-art. Commercial benefits are reduction in the number of costly design-simulate-fabricate cycles prevalent in the Electronic Design Automation (EDA) industry. Military Electronic Warfare (EW) applications include the potential for inducing disruptive RF phenomena in threats by discovering threat-specific Low-Probability of Intercept (LPI) input waveforms.

P.7: Watt-level W-band N-polar GaN Transistors

Matthew Guidry, Emre Akso, Christopher Clymore, Henry Collins, Wenjian Liu, Brian Romanczyk, Weiyi Li, Nirupam Hatui, Christian Wurm, Stacia Keller, Umesh K. Mishra
University of California, Santa Barbara, CA

N-polar GaN deep recess MISHEMT devices have previously shown excellent mm-wave CW transmit power density at 94 GHz. Now this performance has been validated in large-periphery power device cells, providing 1 Watt of output power from a single device cell at 94 GHz. This was made possible by two improvements. First, the total device gate periphery was scaled up to 150 μm using four parallel gate fingers and a source airbridge to minimize inductive and resistance parasitics and maintain useful device gain. Second, this larger periphery device cell required an improved measurement system, so a 94 GHz active tuning load pull system was validated and then used to measure the large signal performance of this device at 94 GHz.

P.8: Fieldable Integrated Photonics Systems Across the Spectrum

Cheryl Sorace-Agaskar, Colin Bruzewicz, Patrick Callahan, John Chiaverini, Christopher Heidelberger, Dave Kharas, William Loh, Thomas Mahony, Ryan Maxon, Robert McConnell, Alexander Medeiros, Alkesh Sumant, Meghan Schuldt, Reuel Swint, Paul Juodawlkis
MIT Lincoln Laboratory, Lexington, MA

Rachel Morgan, Kerri Cahoy
Massachusetts Institute of Technology, Cambridge, MA

We review recent work on emerging Photonic Integrated Circuit (PIC) technology for broad spectral coverage in fieldable optical systems and microsystems. We describe recent demonstrations at non-traditional wavelength including the visible and the mid-infrared using MIT Lincoln Laboratory's integrated photonic platforms. We also discuss environmental testing results for packaged PICs operating in the telecommunications band. Applications include quantum computing and sensing, atmospheric gas detection, chemical and biological sensing and microwave photonics.

P.9: Comparing Analog CMOS Hopfield and Ising Networks on NP-hard Problems – Hopfield vs Ising on the SoC FPAA

Pranav O. Mathews, Jennifer O. Hasler
Georgia Institute of Technology, Atlanta, GA

This paper compares physical Hopfield and Ising networks in 350 nm CMOS on solving NP-hard problems. The discussion reviews the equivalence of both networks and their implementation on a large-scale Field Programmable Analog Array that allows for an equal comparison on identical silicon. The two networks are compared when solving identical NP-hard problems on convergence times, energy efficiency, and ease of use. Hopfield networks outperformed the Ising networks in convergence time, energy, and power, and were also easier to use overall.

P.10: Scalable Analog Standard Cells for Mixed-Signal Processing and Computing

Jennifer Hasler
Georgia Institute of Technology, Atlanta, GA

This work presents a developed and experimentally measured programmable analog standard cell library for mixed-signal computation and its resulting synthesis. This effort presents the methodology and resulting impact in developing these analog standard cell library, as well as the methodology integrating these cells into synthesis tools.

P.11: Compact Linear Time to Digital Converter Using Pulse Shrinking Rings

Patricia Tutuani, Randall Geiger
Iowa State University, Ames, IA

A compact high-resolution Time to Digital Converter (TDC) is introduced that combines a pulse shrinking ring comprised of an even number of inverting delay elements with a pulse-arbiter delay line. By leveraging the linearity provided by the pulse shrinking ring and the resolution offered by the pulse-arbiter delay line, this approach provides both high resolution and good accuracy in the time-to-digital conversion process.

EO/IR Technologies, Components, and Systems Posters

P.12: Broadband Visible-SWIR Imaging with Germanium Detectors

Christopher Leitz, Kevan Donlon, Ilya Prigozhin, Daniel Schuette, Douglas Young, Renee Lambert, Cameron Walton, Noah Pestana
MIT Lincoln Laboratory, Lexington, MA

Germanium exhibits high sensitivity to both short-wave infrared (SWIR) and visible light, making this material a candidate for imaging applications in these wavebands. Recent advances in device processing now enable high-quality imaging devices to be realized in this material. Moreover, since large-diameter germanium wafers are commercially available, these imagers can be fabricated in the existing highly automated tool set used to fabricate silicon imaging devices, in many cases leveraging mature fabrication processes with only minor modifications. In this article, we describe development of germanium charge-coupled device (CCD) and hybrid active-pixel sensor (APS)-style imagers with the long-term goal of realizing megapixel-class germanium detectors with read noise of a few electrons or less and excellent sensitivity across both the visible and SWIR wavebands.

P.13: Enhanced UV-Visible Rejection in Metal/$BaTiO_3$/β-Ga_2O_3 Solar-Blind Photodetector

Nathan Wriedt, Lingyu Meng, Dong Su Yu, Joe McGlone, Kyle Liddy, Ashok Dheenan, Sushovan Dhara, Hongping Zhao, Siddharth Rajan
Ohio State University, Columbus, OH

Oleg Maksimov, Richard Blakeley
Radiation Monitoring Devices, Watertown, MA

We report on an investigation of metal/$BaTiO_3$/β-Ga_2O_3 solar-blind photodetectors. β-Ga_2O_3 is a promising material for solar-blind photodetectors due to its large bandgap and the availability of low defect-density melt-grown substrates. In this work, we introduce structures that employ high-permittivity heterojunctions to overcome the lack of p-type doping. We show that integrating the high-k dielectric $BaTiO_3$ leads to improved dark current, excellent sensitivity, and a UV-visible rejection ratio that is improved by a factor of >1000× when compared with a Schottky photodetector.

High Performance Digital and Mixed-signal Technologies Posters

P.14: Facilitating the Design of Complete System-on-Chip through High-Level Synthesis

Santosh Shetty, Benjamin Carrion Schaefer
University of Texas at Dallas, Richardson, TX

High-Level Synthesis (HLS) dramatically facilitates the design and verification of individual components. These components are typically the dedicated hardware accelerators used within larger systems, e.g. image processing, DSP or encryption cores. Unfortunately, HLS is a single process (component) synthesis method. This implies that the integration of these accelerators are often done at the RT-Level, which implies that the system-level verification and co-design needs to be done at lower levels of abstraction. This work presents an approach that enables a path to generate complete SoCs at the behavioral level.

P.15: Benefits of HLS for DoD ASIC Development

Edwin Lee, Michael Parker, Monir Zaman
Raytheon Technologies, El Segundo, CA

Kirk Ober
Cadence Design Systems, Inc., San Jose, CA

Once conceptualized as futuristic, HLS (High Level Synthesis) tools are now mainstream for ASIC and FPGA design in development of commercial applications, relegating hand-coded RTL (Register Transfer Language) methods such as Verilog and VHDL to the past. Our paper details our experience using HLS to design an ASIC with a large scalability and high complexity data path design, comparing this with efforts to replicate the same design using Verilog and VHDL. We will provide area, power and development time metrics of both flows, supporting our conclusion that HLS tools surpass RTL hand coding in virtually all cases. The perception that HLS tools are too risky to adopt because of their novelty and abstraction of design control is overcome by dramatic improvements in development efficiency, and this gap will grow will anticipated acceleration using generative AI technologies in tandem with HLS.

P.16: Digital Twin Models for Design Optimization of Ultra-Wideband Transceiver Systems

Arnaldo J. Sans, John M. Willis, John L. Volakis, Satheesh B. Venkatakrishnan
Florida International University, Miami, FL

Wilfredo Rivas-Torres
Keysight Technologies, Inc., Santa Rosa, CA

The rapid evolution of wireless millimeter-wave (mm-Wave) links has provided an impetus in the developing low power of ultra-wideband (UWB) transceiver systems. Notably, UWB wireless links enable interference immunity using spread spectrum modulation technique. Several reasons make spread spectrum techniques attractive as relates to noise, direct signal interference and signal fading (multipath fading). Designing and optimizing such systems pose formidable challenges. This paper proposes a system design methodology using the digital twin circuit concept. The model accurately reflects the realistic design and therefore predicts the performance of the UWB RF transceivers.

P.17: On the Journey to True 3DHI Microsystems: Fusing Functions and Materials

Kenneth Larsen
Synopsys, Mountain View, OR

P.18: Experimental Demonstration of Stochastic Bayesian Inference Using Muller C-Elements

Alexander Edwards, Ebenezer Usih, Peng Zhou, Brighton Hill, Steve Martindell, Tianxi Qi, Disha Biswas, Xuan Hu, Shreya Mysore Panduranga, Joseph Friedman
University of Texas at Dallas, Richardson, TX

Muller C-Elements (CEs) perform naive Bayesian inference within the stochastic computing paradigm, enabling energy-efficient data fusion. We report the first fabricated stochastic Bayesian inference engine implemented with CEs. Our measurements of four distinct CE structures experimentally demonstrate tradeoffs among accuracy, efficiency, robustness, and speed. Our chip achieves better PDP than other proposed stochastic Bayesian engines with CEs, and is the first such chip to be fabricated.

P.19: The Advantages of Dual Use Intellectual Property in Government Chip Design Projects – How Marvell Government Solutions used Intellectual Property developed for Commercial Standard Products to rescue a chip design project whose Analog and Mixed Signal block was unable to meet specifications

Aidan Kelly, Laura Chadwick
Marvell Government Solutions, Burlington, VT

Marvell Government Solutions has access to a broad portfolio of Intellectual Property used in Marvell's commercial semiconductor solutions. By leveraging silicon proven designs, Marvell Government Solutions was able to identify a proven Analog and Mixed Signal block, propose low risk changes to integrate that block into a government design, offering a path to improved noise performance and power dissipation. This paper outlines a path to reusing commercially proven designs and proving that dual use of system blocks is possible for government and commercial chip designs.

P.20: Reducing Power Consumption of Next Generation Ultra Wideband Software Defined Radios

John Majewski
Analog Devices, Inc., Chelmsford, MA

W. Michael Jones
Analog Devices, Inc., Durham, NC

Advances in direct RF sampling converters necessitate new architectures in baseband processors as channel count and converter sample rates have outpaced baseband processor capabilities. This paper analyzes the hardware resources and power consumption of common digital signal processing blocks implemented in FPGA-based SDR's, and proposes an architecture to reduce power consumption while maintaining broad RF spectrum situational awareness.

P.21: Methodology for Verification and Validation Shift Left

Paul Morrison
Siemens EDA, Longmont, CO

Andy Meier
Siemens EDA, Marlborough, MA

System-level testing has increasingly become a larger percentage of the overall time required to complete a product and have it ready for use by customers. As designs get larger and more complex, standard verification and validation solutions are no longer sufficient. Additional solutions have filled this gap, but do not provide a seamless transition when going from one to another. This paper presents a testing approach that allows transitions from one to another with minimal changes, allowing hardware and software testing and debug of a full system thoroughly and quickly to shift left the product availability. The results of this approach will be reported.

Packaging, Integration, Thermal and Control Technologies Posters

P.22: Temperature Control Through Dynamic Approximations

Siyuan Xu, Benjamin Carrion Schaefer
University of Texas at Dallas, Richardson, TX

Many applications exhibit significant tolerance to inaccuracies. These can be exploited to build faster circuits with smaller area and lower power. In this work we leverage this property to dynamically control the temperature of a circuit by trading off temperature with output error. To achieve this we propose to isolate and encapsulate different portions of the circuits and turn these approximations on and off at runtime. Different approximation primitives are used for different parts of the circuit based on their potential for approximation. These include approximating parts of a circuits by a constant or by another signal with high correlation. A controller then dynamically enables or disables these approximations at runtime based on the temperature in the circuit. This allows to trade-off dynamically, at runtime, the output error vs. the temperature. Moreover, we show that knowing where the approximated circuits are placed allows to specifically target Hotspot build-ups. We have prototyped the system on an FPGA board and show the effectiveness of the proposed framework.

P.23: Frequency Domain Thermoreflectance for Bond Evaluation in Heterogeneously Integrated Microelectronics

Wyatt Hodges, Amun Jarzembski, Anthony McDonald, Benjamin Treweek, Matt Jordan, Matt Bahr, Tim Walsh, Luke Yates, Greg Pickrell
Sandia National Laboratories, Albuquerque, NM

Heterogeneously integrated (HI) electronic systems are needed for high-consequence applications. One barrier to integrating HI systems is lack of understanding of failure due to thermomechanical stresses developed during manufacturing or use. In order to examine thermomechanical failures in HI systems we utilize Frequency Domain Thermoreflectance (FDTR) to examine bond quality of structures in indium-interconnected silicon. FDTR is shown to be able to image metal interconnects through 50 μm of silicon without cross sectioning the sample. We additionally show the ability to finite element models to give insight about FDTR measurements in geometrically complex samples.

P.24: Rapid Subsurface Analysis of Frequency Domain Thermoreflectance Images with K-Means Clustering

Amun Jarzembski, Zachary Piontkowski, Anthony McDonald, Wyatt Hodges, Matt Bahr, William Delmas, Greg Pickrell, Luke Yates
Sandia National Laboratories, Albuquerque, NM

Non-destructive characterization of subsurface features in heterogeneously integrated (HI) microelectronics is needed for their robust utility. Frequency domain thermoreflectance (FDTR) provides a unique opportunity to characterize the bond/interconnect integrity in HI microsystems by leveraging thermal penetration to image subsurface heat pathways. Here, we show how rapid analysis of FDTR hyperspectral images with K-Means clustering enables quantification of bond quality in a GaN-diamond microsystem.

P.25: Metal Core Substrate for Advanced Packaging

Shane McMahon, Graeme Housser
Lux Semiconductors, Albany, NY

Lux Semiconductors is developing a new system-level advanced packaging technology, System-on-Foil, to address the shortcomings of current state-of-the-art packaging solutions. The System-on-Foil architecture contains a patterned metal core, able to carry high speed signals between redistribution layers on the top and backside. Copper transmission lines are patterned in silicon tools at interposer densities, enabling high bandwidth, low latency routing for chiplet-based heterogeneous integration. A thick dielectric layer stack allows for low loss high speed transmission lines, which can be routed through the metal core in highly tuned coaxial lines with near zero crosstalk. The metal core also provides high thermal conductivity, a CTE near silicon, and strength for durability even in ultra-thin form factors. Collectively, the unique capabilities of System-on-Foil will allow this novel platform to service DoD State-of-the-art Heterogeneous Integrated Packaging (SHIP) application targets, including Extremely High Performance, Ultra Low Power, and Radiation Hard – Safety Critical.

P.26: Atomistic Thermal Model of Nanoscale Transistor

Sanghamitra Neogi, Artem Pimachev, Ashley Pera
University of Colorado Boulder, Boulder, CO

We develop a phonon-physics-based, parameter-free computational framework for thermal modeling of complex microelectronic structures. Atomistic modeling can provide highly accurate prediction of thermal properties of finite systems. For example, molecular dynamics simulations enable us to model thermal properties in steady-state or transient thermal operating conditions. However, the simulations usually require days to weeks for even simple structures. To overcome this challenge, our framework combines phonon-physics insights and emerging machine-learning techniques, to speed up the atomistic modeling. Our thermal model directly predicts interior tempera-

tures of the structures under steady-state and transient heating conditions, without additional calibration steps. We demonstrate the performance of the framework on a class of structures ranging from isolated nanometer (nm)-scale transistors to array of nanoscale transistors. The model will provide highly valuable insights to the device engineers to rapidly achieve thermally optimized transistor designs and cut down the time and resources otherwise spent on calibration procedures.

P.27: Active Flexible Connector for High Bandwidth Signaling in System-on-Wafer Applications

Randall Irwin, Subramanian S. Iyer
UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS), Los Angeles, CA

FlexCon, a high bandwidth connector cable platform, is a key enabling technology for systems-on-wafer (SoWs), which are anticipated to meet the growing demand for memory and compute in AI and machine learning applications. Here, we explore the effect of a low-loss Parylene-N dielectric and an integrated linear redriver on the signaling performance of FlexCon. These greatly extend the reach of FlexCon channels while maintaining excellent signal integrity. The reliability of FlexCon is investigated under cyclic bending and temperature and humidity testing.

P.28: Precise On-Chip Temperature Control for Production Testing: The Constant-Power Microheater

Emmanuel Amankrah, Pallavi Ebenezer, Kwabena Banahene, Bryce Gadogbe, Degang Chen, Randall Geiger
Iowa State University, Ames, IA

The concept of using constant-power on-chip microheaters for test cost reduction of integrated circuits that contain precision temperature-critical blocks is introduced. The constant power microheaters offer precise and repeatable temperature increases and can be used to reduce production testing costs by providing multi-temperature trim/calibration performance with a single test insertion in a standard ambient temperature production test flow. Experimental results of a via heater designed in a 0.18 μm CMOS process that show the microheater provides an accurate temperature increment and close agreement with simulation results are discussed.

Photonic Technologies, Components, and Systems Posters

P.29: A Low-Noise, Widely Tunable C-Band Hybrid External Cavity Laser

Ivan Shubin, Liangshun Han, Bill P.-P. Kuo, Jack Holloway
Raytheon Advanced Photonics Group, San Diego, CA

P.30: PhotoFourier: Silicon Photonics Joint Transfer Correlator for Convolution Neural Network

Nicola Peserico, Hangbo Yang, Russell L. T. Schwartz, Hamed Dalir, Volker J. Sorger
University of Florida, Gainesville, FL

Shurui Li, Puneet Gupta
University of California, Los Angeles, CA

Convolution Neural Networks are one of the pillar of the Machine Learning revolution over the last years. However, convolution operation is associated with a high computational cost. Here, we present a compact and high-speed solution to perform convolution leveraging optics on a chip, with the potential to reach over 350 TOPS/W.

Power Electronics and Emerging Power Technologies Posters

P.31: Accurate and Fast Prediction of Thermal Behavior in GaN High Electron Mobility Transistor Circuits

Saidur Bakaul, Sudeepta Mondal, Soumalya Sarkar
Raytheon Technologies Research Center, Hartford, CT

Mehdi Anwar
University of Connecticut, Storrs, CT

Herein, we emphasize a critical gap in existing simulators that model high electron mobility (HEMT) circuits' thermal behavior — interdependencies among electrical, mechanical, and thermal parameters are not considered in state-of-the-art software. This causes inaccurate prediction of local temperatures. We propose to develop a full thermodynamic model to improve thermal modeling accuracy and implement machine learning algorithms to accelerate converging of such time-consuming simulations.

P.32: Characterization of Vertical Gallium Nitride Photoconductive Semiconductor Switches

Geoffrey Foster
Jacobs, Inc., Washington, DC

Andrew Koehler, Karl Hobart, Travis Anderson
Naval Research Lab, Washington, DC

Samuel Atwinmah, Sadab Mahmud, Raghav Khanna
University of Toledo, Toledo, OH

Jacob Leach
Kyma Technologies, Inc., Raleigh, NC

P.33: Radiation Hard High Voltage Power Supply in Package using Heterogeneous Integration

Collin Burt, Rafmag Cabrera, Albert Colon, Scott Habermehl, Steven Larson, Judi Lavin, Jaime McClain, Jason C. Neely, Greg Pickrell, Andrew Ian Young
Sandia National Laboratories (SNL), Albuquerque, NM

P.34: Design of Multi-kV $BaTiO_3$/Ga_2O_3 Transistors with Graded Thickness $BaTiO_3$ Layers and Near Ideal Electric Field Profiles

Ashok V. Dheenan, Sushovan Dhara, Chandan Joishi, Siddharth Rajan
Ohio State University, Columbus, OH

Beta-Ga_2O_3 is an ultrawide bandgap semiconductor with attractive properties for high power electronics including an high breakdown electric field and native melt-grown substrates. High-k $BaTiO_3$ has recently been integrated with Beta-Ga_2O_3 and shown to lead to more uniform electric field profiles and increased breakdown voltage in lateral devices. In this study, we use TCAD simulations to show that a lateral grading of the $BaTiO_3$ thickness in the gate-drain region can further increase average breakdown fields for multi-kV Beta-Ga_2O_3 power transistors.

Radiation Hardened Technologies, Designs, and Systems Posters

P.35: A RISC-V Migration, the Future of Space Computing

Richard Ferguson, Dave Moser, David Matthes
BAE Systems, Manassas, VA

Dany Nativel
SiFive, Santa Clara, CA

BAE Systems has been a trusted component supplier for the radiation-hardened space community for multiple generations of processor components. The sun is setting on PowerPCTM architectures and a transition is needed to a modern Instruction Set Architecture (ISA). RISC-V® based designs are gaining momentum in the space community and this paper will discuss our transition to RISC-V processor components to meet the needs of the future.

P.36: Leveraging Automotive Functional Safety Design Techniques for RHBD SoCs

Jeff Wetch, David Kingston
Synopsys, Inc., Sunnyvale, CA

The automotive industry has introduced many functional safety constructs into their SoC designs for many years that enhance the fault tolerance and safety of their electronics systems. These include fault tolerant state machines, triple mode redundant storage elements, error correction for memories and many others. Many of these same constructs can be used in radiation hardened SoCs to mitigate the effects of heavy ions and particle strikes on the die. Single event effects (SEUs) in integrated circuits can be mitigated by careful layout of the various standard cells in a library used for synthesizing SoCs and by taking advantage of the pre-defined functional safety (FuSa) constructs already available to automotive SoC designers. This paper will discuss the various techniques available to engineers for insertion of flip-flop storage elements based on the soft error rate (SER) of individual flip-flop library cells.

P.37: Simulated Space Radiation Doses in Cislunar Space

Ishaan Rao, Sayan Roy, Peter Bermel
Purdue University, West Lafayette, IN

The radiation environment in Earth orbit is harmful to satellite electronics. To maximize satellite durability in the radiation environment, an accurate estimate of the radiation dose received in any given orbit is required. This paper investigates the radiation environment in cislunar space to determine the expected radiation dose for common orbits. Having more accurate radiation dose information allows satellite designs to optimize their intended orbits, balancing radiation shielding with mass requirements. Having a detailed understanding of the distribution of radiation particles also allows for electronic equipment to be designed for durability against particular types of radiation.

P.38: Single Event Transient Pulse Width Characterization and Analysis of Basic Skywater 130 nm Logic Gates

Janani Aravind, Daniel B. Limbrick
North Carolina Agricultural and Technical State University, Greensboro, NC

This research aims to analyze Single Event Transient (SET) pulse durations in 1-input and 2-input logic gates with low drive strength, utilizing the Skywater 130 nm (Sky130) technology library and SPICE simulations, while also conducting a comparative evaluation against data acquired from the IHP 130 nm (IHP130) technology library to discern variations in how these logic gates respond to SET events. By exploring these differences, the study seeks to enhance the understanding of the susceptibility and resilience of low drive strength logic gates to SET incidents, offering valuable insights for optimizing electronic circuit designs in applications where radiation-induced transients may be problematic, such as aerospace, space exploration, or critical infrastructure.

P.39: Radiation Hardened Processors and 90 nm Products

**Jim Hobbs, Robert Rabe, James Patella,
Romney Katti, Dave Nelson**
Honeywell, Plymouth, MN

P.40: A Potential Approach to Radiation Modeling on Large Systems Composed of Multiple Chips or Integrated Circuits

Thomas Wolf, Kent Smith
Silicon Technologies, Inc., Midvale, UT

Large state of the art electronics systems in radiation environments can use a variety of technologies, packaging, shielding, and other parameters that can affect the response of the system to radiation. These complex systems may contain a combination of analog and mixed signal microelectronic including sensors, wireless communications, video, audio, CPUS, Memories, actuators, clocks, and other critical circuits. A variety of electronics could be built with standard CMOS, GaNa, FinFet, and other processes and then combined into a single high level system.

P.41: Giving Mars Rover the Gift of Planetary Adaptability

Paul Chopelas, Kristine Schroeder
Avalanche Technology, Fremont, CA

For improved prospects of colonizing other planets in a timeframe of relevance, dramatic improvements to capability and pace of innovation are required for space-based systems, from orbiting satellites to mobile rovers. As the eyes, ears, and ambulatory emissaries for some of the most hostile reaches of the universe, rovers need to be untethered from latency-riddled remote control, requiring high levels of intelligence, adaptability, survivability, and autonomy to become resilient in changing conditions. Current systems are limited by the availability of sufficiently radiation resilient advanced semiconductors, leaving them less able to respond to changing conditions. Recently, several semiconductor innovations have been introduced, including advanced adaptive SoCs and high density, radiation resilient non-volatile memory, which together address capability gaps and enable an accelerated pace of innovation going forward. This paper will examine historical limitations and these novel device innovations which could provide Mars Rover with planetary adaptability and increasing levels of autonomy.

RF Technologies, Components, and Systems Posters

P.42: Doubling ADC Sampling Bandwidth with Direct Quadrature Sampling

Peter Delos, Brian Reggiannini, Connor Bryant
Analog Devices, Inc., Wilmington, MA

This paper presents an approach to double the effective ADC sample rate using direct quadrature sampling rather than interleaving. An example will be illustrated to create an effective 40GSPS ADC monitoring an entire 2–18 GHz input bandwidth. First, direct quadrature sampling is described relativeto the more common Zero-IF (ZIF) architectures. Quadrature errors are acknowledged along with embedded digital processing needed for quadrature error correction (QEC). MATLAB models published for the data converter are used as a basis for simulation. The simulation approach allows including S-Parameters for the RF front end, sampling of ADC data, embedded DSP processing and final processing of data converter IQ outputs. Simulation results are presented. The approach is described for a specific IC yet extendable generally to any wideband sampling system.

P.43: Wideband Programmable Frequency Divider in an Advanced 45 nm SiGe BiCMOS Process

Samantha McDonnell, Lauren Pelan, William Gouty, Trevor Dean, Tony Quach, Stephen Hary
Air Force Research Laboratory, Wright-Patterson AFB, OH

Waleed Khalil
Ohio State University, Columbus, OH

David Dolt, Samuel Palermo
Texas A&M University, College Station, TX

P.44: Direct Observation of Microwave-Frequency Reflection Gain in GaN-Based IMPATT Diodes

Z. Zhu, P. Fay
University of Notre Dame, Notre Dame, IN

A. Xie
Qorvo, Inc., Richardson, TX

High-efficiency, high-power microwave and millimeter-wave sources are critical components for many communications and sensing systems. Impact ionization avalanche transit-time (IMPATT) diodes leverage the negative differential resistance associated with avalanche breakdown to make very efficient high-frequency oscillators into the millimeter-wave regime. While Si and GaAs-based IMPATTs are well established, the use of GaN and related III-N materials offers an opportunity for significantly improved power-frequency performance, with projected power-frequency products approximately 500× higher than those possible with Si. This promises to enable greatly increased output power levels at high DC to RF conversion efficiency. We report here the first direct observation of microwave-frequency reflection gain in GaN-based IMPATT diodes. Good agreement between theory and experiment is obtained for the avalanche frequency's dependence on bias, and projections of millimeter-wave performance are made from the measured microwave performance.

P.45: Development and Qualification of an Improved Bulk Acoustic Wave Resonator Technology for Open Foundry

Romain Gerbe, Daniel Hou, Yuefei Yang, David Wang, Andy Chen, Eric Schneider
Global Communication Semiconductors, LLC (GCS), Torrance, CA

We are reporting our effort to develop a competitive structure and process for Bulk Acoustic Wave resonators for an open-foundry service, where the designers have the flexibility to select the frequency and bandwidth of their acoustic filters. The objectives of the structure are to deliver high-performance and reliable devices for any design required by the designers. After developing Finite Element Models of the resonators and designing competitive structures, devices with different frequencies and piezoelectric materials (AlN/ScAlN) have been fabricated and their quality factors have been characterized. The reliability of the filters has also been assessed through power handling tests.

P.46: Single Chip Direct RF Waveform Classification Using Intel FPGA AI Suite

Hong Shan Neoh, Pierre Duhamel, William Pye, Jonathan Wulf, Greg Nash
Intel Corporation, San Jose, CA

Dan Pritsker, Suk Bum Lee
Intel Corporation, San Diego, CA

Modern FPGAs have been released with integrated direct RF data-converters, CPU and FPGA fabric. On an Intel® Stratix-10 AX Direct RF SOC FPGA, we develop and test a system that has RF to classified waveform using an AI inference engine in a single package. This allows for the lowest latencies while still achieving 95% accuracy on the test set. We present data from the device, the toolset used, details of the network, and results.

P.47: Signal and Power Transfer in a Waveguide Confined Network

Gurkan Gok, Joseph Zacchio, Dustin Caldwell, Thomas Martin, Joseph Mantese
Raytheon Technologies Research Center, East Hartford, CT

P.48: HF Antennas Based on Magnetodielectric Materials

Haoling Li, Bin Luo, Nian X. Sun
Northeastern University, Boston, MA

Xiaoling Shi, Mark Sun, Hwaider Lin
Winchester Technologies, LLC, Burlington, MA

Novel magnetic dipole-based magnetodielectric antennas exhibit advantageous properties of ground plane immunity, ultracompact size, reduced profile and signature, enhanced radiation, and potential to approach Chu's Limit, showing great opportunity in military vehicles in the HF band. We demonstrated a compact HF magnetodielectric antenna based on commercially available NiZn ferrites. The comparison between the high hesitivity magnetodielectric antenna and traditional antennas revealed a prospective pathway for HF military antenna with significant miniaturization, enhanced radiation, and ground plane immunity.

P.49: Noise Canceller ADC with FPGA in the Loop Performance Assessment

Ethan Rando, Saiyu Ren, Ray Siferd
Wright State University, Dayton, OH

P.50: Ka-Band 12W Asymmetric Doherty PA GaN MMIC

Gayle Collins, John Wood
Obsidian Microwave, LLC, Raleigh, NC

P.51: Aerosol Jet Printed Multi-line TRL Structures for Millimeter-Wave Calibration

Matthew Hodek, Nicholas C. Miller
Michigan State University, East Lansing, MI

P.82: The Design of Wideband High Linearity Low Noise Amplifiers in 45 nm SiGe BiCMOS

David Dolt, David Reents, Samuel Palermo
Texas A&M University, College Station, TX

Will Gouty, Tony Quach
Air Force Research Laboratory, WPAFB, OH

Trusted, Assured, and Cyber-secure Microelectronics Posters

P.52: Hyperdimensional Distributed Learning for Heterogeneous Sensor Networks

Mohsen Imani
University of California Irvine, Irvine, CA

Hugo Latapie
CISCO Systems, San Jose, CA

In this paper, we propose EdgeHD, a hierarchy aware learning solution that performs online training and inference in a highly distributed, cost-effective way. We use brain-inspired hyperdimensional (HD) computing as the key enabler. HD computing performs the computation tasks on a high-dimensional space to emulate functionalities of the human memory, such as inter-data relationship reasoning and information aggregation. EdgeHD exploits HD

computing to effectively learn the classification models on individual devices and combine the models through the hierarchical IoT nodes without high communication costs. We also propose a hardware design that accelerates EdgeHD on low-power FPGA platforms. We evaluated EdgeHD for a wide range of real-world classification applications. The evaluation shows that EdgeHD provides highly efficient computation with reduced communication. For example, EdgeHD achieves on average 3.4x– and 11.7x– (1.9x– and 7.8x–) speedup and energy efficiency improvement during the training (inference) as compared to the centralized learning approach. It reduces the communication costs by 85% for the training and 78% for the inference.

P.53: State-of-the-Art Commercial Anti-Counterfeiting

Scott C. Best, Matthew Orzen
CRI, Inc. (a subsidiary of Rambus, Inc.), San Jose, CA

Counterfeit microelectronic detection is accomplished by answering exactly two questions for any particular component: is the component authentic? And does it belong here? This paper presents mass-production, commercial technology that addresses the first question “is the component authentic?” for both FPGAs and custom microelectronic ICs (e.g., ASICs and SoCs) that include an authentication function (i.e., an “authentication IC”. As part of Rambus’ anti-counterfeiting product line, the technology described herein has shipped in more than 650 million chips over the last ten years. The second question “does the component belong here?” is primarily what is asked of commercial secure supply-chain solutions which we present separately. Topics covered in this paper will include a description of the nominal attacks a system operator can expect on their ICs, as well as state-of-the-art countermeasures which mitigate these attacks. Attacks will be gathered into three common categories: non-invasive, semi-invasive, and fully-invasive.

P.54: VARI-CHECK: Authentication of COTS Devices using ML-Based Variability Characterization

Christopher Vega, Patanjali SLPSK, Ravalika Karnati, Swarup Bhunia
University of Florida, Gainesville, FL

Counterfeit devices are a growing threat to trust in electronic devices, involving the production and distribution of fake components or reselling out-of-spec ones. These pose risks like compromised functionality, security vulnerabilities, and economic losses when purchasing Commercial Off-The-Shelf (COTS) devices like FPGA and microcontrollers. To address this, we introduce VARI-CHECK, a low-overhead method for authenticating COTS devices. VARI-CHECK leverages inherent fabrication process variations to create digital signatures for device authentication. We validate this approach through experiments on FPGA devices, training a machine learning model to identify non-original devices. We test it on 100 oscillating/bistable circuit elements across 40 FPGA devices, achieving 80.4% success with Isolation Forest and 81.25% with One Class SVM.

P.55: Blockchain-enabled Whitelisting for Securing 3D ICs

Ujjwal Guin
Auburn University, Auburn, AL

Bhaskar Krisnamachari
University of Southern California, Los Angeles, CA

Due to the lack of trust among the entities in the semiconductor supply chain, ensuring security for 3D ICs becomes extremely challenging. The chiplets that are fabricated at an untrusted location can be tampered with, resulting in the insertion of malicious circuits that may leak secret information to an adversary. This paper presents a conceptual approach that limits the communication capability of an untrusted chiplet using a whitelisting approach inspired by security measures deployed in traditional networks. We also propose to use a logger to capture any communication rule violation that occurs during die-to-die communications across different chiplets. The logger state can be further uploaded to an immutable blockchain ledger for forensics purposes if an attack is identified.

P.56: Dendritic Identifiers: A Novel Approach to Transparency, Trust, and Assurance in Microelectronic Supply Chains

Michael N. Kozicki
Arizona State University, Tempe, AZ
and
Densec ID, LLC, Phoenix, AZ

Transparency, trust, and assurance in microelectronics manufacturing require a new approach to the digital identity of individual parts, regardless of size or selling price. The missing element is a digital trigger that fits the cost, security, and compatibility requirements of the supply chain, while matching the performance of the latest cryptographic databases. We present our approach to this issue in the form of an inexpensive “fingerprint” for components – the Dendritic Identifier. This physical element is naturally unique and difficult to clone. It can also be applied directly to parts and read using existing camera systems in-line or in the field.

P.57: Sliding Across the Power Side Channel

Kevin Pintong, Douglas Summerville
Binghamton University, Binghamton, NY

Side channel analysis can be used to detect anomalous behavior, but the cost of performing it in an automated way is currently too high to implement in a small and low-cost form factor. In this work we show that that it is possible to identify specific algorithms running on a target processor in a lightweight manner. For instance, we show that we can distinguish between various algorithms even when the individual instructions cannot be identified with high certainty. We show that the sliding window method is effective for detecting an algorithm when tested on a trace with multiple algorithms and provide associated metrics such as false positive rates. We also explore parameters that affect the detection performance such as sampling rate, method, and effects of adjacent instructions.

P.58: A Full Hardware Implementation of CRYSTALS with Implementation Attack Resistance

Abubakr Abdulgadir, Luke Beckwith, Rami Elkhatib, Reza Azarderakhsh
PQSecure Technologies LLC, Boca Raton, FL

Current cryptographic standards can be broken by a sufficiently large quantum computer. A new set of algorithms that are believed to be secure against quantum computing attacks have been evaluated and selected by NIST to replace our current public key encryption standards. The primary algorithms are CRYSTALS-Kyber for key exchange and CRYSTALS-Dilithium for digital signatures. While these algorithms are secure against quantum computing attacks, their implementations are still vulnerable to implementation-based attacks such a power analysis. This work present a protected hardware implementation of CRYSTALS-Kyber and CRYSTALS-Dilithium which is protected against power side-channel attacks. This design is the first reported protected hardware implementation of Dilithium and the first protected combined hardware implementation supporting both Kyber and Dilithium.

P.59: Highly Secure Central Repository Framework for Complex RTL SoCs

Khushboo Mittal, Naincy Katyal, Nitin Garg
Synopsys India Pvt. Ltd., Noida, India

Dale Donchin
Synopsys, Inc., Marlborough, MA

Modern system-on-chips (SoCs) have increased vulnerabilities because of growing global supply chains, making it more challenging for design foundries to securely rely on IP designs from around the world. Further, making the appropriate IP choices and IP configuration decisions satisfying SoC constraints requires high-level SoC design expertise. IPs can originate from several manufacturers, and each IP can have hundreds of settings without any knowledge of Power, Area, Speed, or Security (PASS). It is crucial to

develop a strategy for addressing design complexity and secure RTL IP selection simultaneously due to short time to market and increasing design difficulties. To address these issues, this paper proposes a secure central repository (repo) framework where authorization is granted through a security asset container mechanism. It further provides a systematic method for authorized IP authors to store IP metadata, such as PASS, IP version, and legitimate RTL sources, in a secure manner.

P.60: The T-PROP Project: Assessing Hardware Confidentiality and Resiliency with RTL Simulation

Arturo Salz
Synopsys, Inc., Sunnyvale, CA

Saurin Shroff
Synopsys, Inc., Marlborough, MA

P.61: Zero-Latency In-Line Encryption

Ryan Prince, Brent Hollosi, Lake Bu
Draper Labs, Cambridge, MA

P.62: Hardware Trojan Horse Detection via Analog Emission Analysis

Tristan J. Hudson, Barry B. Vincent
Booz Allen Hamilton, Beavercreek, OH

Carlos R. Aguayo Gonzalez
PFP Cybersecurity, Vienna, VA

Ashok V. Madanahalli
LOCH Technologies, Emeryville, CA

Kevin J. McCamey
Air Force Research Laboratory, Wright-Patterson AFB, OH

P.63: Verification of Third Party Hard IP by Scalable Graph Search

Luke Gilles, Derek Doran, Jeff Hughes
Tenet 3, LLC, Dayton, OH

Brian Dupaix
AFRL, Dayton, OH

P.64: Using Open-source Hardware for Third-Party Intellectual Property Assessment

Kyle Ahearn, Mark Labbato, Russell Emmert, Saverio Fazzari, Scott Fischer, Barry Vincent
Booz Allen Hamilton, Beavercreek, OH

Brendon Chetwynd
MIT Lincoln Laboratory, Lexington, MA

To quicken the device development process and enable designers to focus more on system design than individual components, the use 3rd party intellectual property (3PIP) has been widely adopted. However, this brings the increased security risk that a piece of 3PIP being placed into a system has hidden malicious functions. The 3PIP may have been verified separately using various verification techniques, but the risk still exists once implemented into a system. To enable a cost effective and rapid development process, Open-source hardware can be leveraged to assess a piece of 3PIP in a system to ensure its functionality and safety. In this paper, an application specific integrated circuit (ASIC) design using the Common Evaluation Platform (CEP) is proposed to assess a piece of 3PIP functionality and safety at the block and system levels.

P.65: The Role of EDA in FPGA Assurance Best Practices

Margaret Winslow, Jonathan Graf, Whitney Batchelor, Scott Harper, Kevin Paar, Ali Asgar Sohanghpurwala
Graf Research Corporation, Blacksburg, VA

Developing assured microelectronics requires coordination throughout the lifecycle of the device to ensure that necessary assurance policy, guidance, and/or best practices are met. Assurance practices for the development of Field Programmable Gate Arrays (FPGAs) can be categorized such that programs can delegate assurance tasks across personnel within a program. A significant portion of assurance practices remain dependent on the actions of the development team, however. This paper explores which of the assurance practices that fall to the development team are automatable using Electronic Design Automation (EDA) tools and which involve more manual interventions and practices, highlighting specific tools of interest to the FPGA assurance community.

P.66: Functional Model Recovery from Transistor Networks for Unknown Cell Identification

Noah Taylor, Tim McDonley, Josh Delozier, Katie Liszewski, Adam Kimura
Battelle Memorial Institute, Columbus, OH

Richard Ott, Matt Sale
Air Force Research Lab, Dayton, OH

In this paper, a new method for recovering combinational and sequential descriptions of small digital networks of transistors is presented. An example circuit is presented, and its description compared to the originally designed Verilog.

P.67: Hardware Accelerated Complete Satisfiability Solvers Exploring Multiple Restart Strategies

Sai Surya Kannan, Christopher Chuvalas, Ranga Vemuri
University of Cincinnati, Cincinnati, OH

Logical decision problems exist throughout many critical applications. These problems can be formulated and solved through Boolean Satisfiability (SAT). These problems often require complete satisfiability methods which guarantee a SAT or UNSAT result upon termination and are challenging to modern CPUs due to their size and complexity. This paper presents an FPGA based complete SAT solver. Our solver utilizes recent complete SAT methods and harnesses the power of a state-of-the-art FPGA accelerator. The solver uses multiple restart strategies and branching and variable selection heuristics, along with the well known capabilities of Conflict Driven Clause Learning (CDCL) to overcome the limitations of CPU bound counterparts in speed and capacity.

P.68: Artificial Intelligence Driven THz Sensing for VLSI Testing and Fault Detection

Muhammad Mahmudul Hasan, Nezih Pala
Florida International University, Miami, FL

John Suarez
Widener University, Chester, PA

Michael Shur
Rensselaer Polytechnic Institute, Troy, NY
and
Electronics of the Future, Inc., Vienna, VA

Hardware security has grown increasingly important, particularly in the VLSI industry. The security and dependability of the entire system are compromised if there are any counterfeit, forged, or defective ICs in the system. The increasing complexity of digital and mixed-signal systems makes devising reliable ways to analyze the reliability and authenticity of ICs more difficult. Using artificial intelligence self-learning models to interpret the THz sensing

response allowed us to develop a novel testing method for the non-destructive and subtle identification of counterfeit, damaged, forged, or defective ICs. A similar approach could be applied to THz sensing for applications ranging from 6G communications to medicine and industrial controls.

P.69: A Temporal Causality Model for SoC-Scale Security Formal Verification at the Hardware-Software Boundary

Zhaoxiang Liu, Xiaolong Guo
Kansas State University, Manhattan, KS

Orlando Arias
University of Massachusetts Lowell, Lowell, MA

Dean Sullivan
University of New Hampshire, Durham, NH

Raj Dutta
Silicon Assurance, Gainesville, FL

We propose MicroScope, a new framework that addresses growing security issues in System-on-Chip (SoC) designs due to their complexity and involvement of third-party vendors. Traditional methods are inadequate for identifying software-exploited hardware vulnerabilities, and existing solutions for hardware-software co-verification often fall short. The framework has been proven effective through extensive testing on SoC benchmarks and it has outperformed existing methods and commercial tools in comparative analyses.

P.70: Trace-Based Runtime Specification Mining for Pre- and Post-Silicon Verification

Tommy Tracy II, Yasas Seneviratne, Kevin Skadron
University of Virginia, Charlottesville, VA

The increasing complexity of modern Integrated Circuit (IC) designs as well as the continued vulnerability of IC manufacturing to adversarial attacks at various stages of design and manufacturing motivates verification at every stage. Runtime monitors can be used in the cases that static verification is inadequate, but generating specifications to be monitored remains a significant challenge. We propose a general approach to automatically generating runtime specifications for our runtime monitoring framework from signal traces generated by simulating a design under test. As a pilot study, we collected traces while simulating an open-source RISC-V and then extracted signal ordering relationships between architectural signals in the form of Linear Temporal Logic (LTL) specifications. To evaluate the extracted specifications, we compared to an existing approach, and found that we reached 75% coverage from a simple simulated workload. We then synthesized hardware monitors from the specifications and integrated them with the CVA6 core.

P.71: Towards System Level Hardware Assurance at Industrial Scale

Alan Ahlberg Elliot
Kansas City National Security Campus by Honeywell FMT on behalf of NNSA and DOE, Kansas City, MO

There is an increasing need for hardware assurance testing procedures that can be applied to commercial off the shelf assemblies without a golden reference and with a high throughput. We propose a framework for an inspection process that uses “quantified assurance” to build a threat model for an unknown assembly and to design a testing schedule that matches an appetite for risk with a finite budget. We focus on advanced adversarial threats and de-emphasize counterfeit for profiteering. Industrial scale optical and x-ray microscopes perform rapid inspections with high resolution. Clustering algorithms are used to detect anomalies. We are developing object detection and character recognition models to help reduce the time required to generate a bill of materials of unknown assemblies. We also present a preview of our dataset of annotated and spatially-correlated optical and xray images. Finally, we discuss the specific challenges we face ramping our inspection process to production.

P.72: Towards Assurance of Microelectronics Third Party IP. Looking a Gift (Trojan) Horse in the Mouth.

Dale Donchin, Shylaja Sen, Mike Borza, Robert Freeman, Alessandra Nardi, John Sorebo, Zongyao Wen
Synopsys, Inc., Sunnyvale, CA

Third party intellectual property (IP) designs, often called "cores", are widely used in all segments of the microelectronic integrated circuit industry. While used to provide functionality in the integrated circuit design, these third-party IP (3PIP) cores can also be a source of malicious or vulnerable code and circuitry. This paper will look at the potential risk areas in the design and a staged process to apply tools and methods that significantly reduce the risk of malicious implants or vulnerabilities.

P.73: Towards Lightning Fast Threat Detection with Near Data Processing

Tommy Tracy II, Sheharyar Khalid, Wajih Ul Hassan, Kevin Skadron
University of Virginia, Charlottesville, VA

Hosts throughout an organization continuously generate system logs and direct them to centralized Security Information Management (SIEM) systems, such as Elasticsearch and Splunk, to facilitate threat detection and incident response. However, the vast volume of these logs, paired with complex threat detection rules, has slowed down the threat rule matching process within these SIEM systems. This inefficiency introduces a delay in threat detection, inadvertently prolonging the attacker's dwell time, and thus granting attackers greater opportunities for persistence. We propose a novel approach to achieve real-time threat rule matching against the enormous volume of logs by offloading event detection to an FPGA. This method not only reduces computational load on the server's CPU but also improves power efficiency. These enhancements come from minimizing repetitive queries on historical data and leveraging efficient hardware engines for pattern matching.

P.74: Towards an Apophatic Definition of Microelectronics Quantifiable Assurance

Jonathan Graf, Scott Harper, Whitney Batchelor, Margaret Winslow
Graf Research Corporation, Blacksburg, VA

Recent reports have called into question the sufficiency of the quantification aspect of DoD Microelectronics Quantifiable Assurance (MQA) efforts. Much of the difficulty they cite in quantification emerges from the fact that the set of what must be proven to be completely assured is infinite and unknowable. We contend that instead of defining that set based on what assurance is, we should be defining it apophatically. That is, we should be defining assurance based on the properties of things that must be absent in order for something to be assured. That set is both quantifiable and extensible. The use of this definition accomplishes more than just precise semantics. Rather, an apophatic definition of assurance establishes a foundation for quantifying assurance via establishment of ontologies of countable aspects. These ontologies specify properties and relationships that can be measured to enable the MQA community to quantify the degree to which objectives have been accomplished. Furthermore, these ontologies are extensible such that as the boundaries of assurance principles expand, the apophatic definition of assurance quantifiably improves with them.

P.75: Guarding the Gatekeepers: Ensuring the Security of Computation Hardware in Cloud Infrastructure

Kejun Chen, Xiaolong Guo
Kansas State University, Manhattan, KS

Xuan Zhang
Northeastern University, Boston, MA

Xianglong Feng
Miami University, Oxford, OH

Physical computation devices, including CPUs, FPGAs, and GPUs, are integral to cloud computing but face unique security challenges. While cloud infrastructures are pivotal for service delivery, they are susceptible to threats. This paper introduces a novel hardware security framework to bolster cloud infrastructure resilience. Utilizing side-channel measurements from the power distribution network (PDN), the framework detects anomalies in computational devices. Leveraging Ring Oscillators and Time-to-Digital Converters, we design PDN sensors, further enhancing security with a co-processor for real-time checks based on Neural Network analysis.

P.76: Formal Verification for Building Secure Hardware Systems

Naiyong Jin, Sudipta Kundu, Sean Safarpour, Manish Pandey
Synopsys, Inc., Sunnyvale, CA

Secure hardware is critical for applications such as automobile ADAS, medical control systems and public infrastructure for power and water. Such systems require secure designs, where there are no unexpected or unauthorized ways to read or modify data such as private keys, encryption keys of privileged memory regions that are considered secure. Typical verification approaches based on code review and simulation are not sufficient to ensure unauthorized reads or accesses do not occur under all conditions. This requires formal verification. VC Formal Security Verifier (FSV) is the industry's highest capacity automated formal verification solution to address this problem. FSV security specification creates properties to check information flow between secure and insecure design zones and disallows secure to unsecure data transfers. FSV parallelizes the formal verification of these properties for efficient security verification and has successfully verified the security of several state-of-the-art industrial RTL designs.

P.77: Genetic Algorithm for Functionally-Equivalent and Structurally-Divergent Benchmark Generation

David S. Koblah, Rabin Acharya, Domenic Forte
University of Florida, Gainesville, FL

This work uses information theory within the context of circuit design optimization and benchmark generation. Previous work has used genetic algorithms and Prolog-based binary trees to minimize conditional entropy in circuit designs. We build on this by employing genetic programming to optimize structural aspects and reduce decision diagram sizing. Unlike the prior approach, which used binary multiplexers, our work adopts Binary Decision Diagrams (BDDs) for benchmark representation. The fitness function, based on mutual and normalized mutual information, guides the optimization process. Additionally, the framework can generate synthetic benchmarks for gate-level design experiments, offering large datasets for use in research applications, including artificial intelligence and hardware security. This work provides a benchmark generation tool with comprehensive results, including running time, generation count, divergence range, and sizing differences. The experiments also explore additional optimization objectives where applicable.

P.78: Multi-layer PCB Via and Trace Tracking Tool using Semi-Supervised Semantic Annotator (S3A)

John True, Thamid Ahmed, Nathan Jessurun, Navid Asadi
University of Florida, Gainesville, FL

In our work, we introduce a simple approach for enhancing the security assurance of Printed Circuit Boards (PCBs) through combining open-source software with X-ray Computed Tomography (CT). By using Python in combination with the Semi Supervised Semantic Annotator or S3A, we meticulously align vias and traces across multiple layers, removing noise and enhancing clarity. Our research fills a critical gap for physical inspection by offering an open-source tool for visualizing circuitry difference across designs. Our technique manipulates overlapping pixel values to ensure accurate via and trace connectivity. This significantly improves analysis of the PCB when compared to analyzing the raw data in other formats. This methodology provides a robust and precise tool for evaluating the interconnectivity and security of multi-layer PCBs without the need for commercial software.

P.79: Dynamic Mitigation of Multiple and Persistent Voltage Attacks on Multi-tenant FPGA

Sandeep Sunkavilli, Mashrafi Alam Kajol, Qiaoyan Yu
University of New Hampshire, Durham, NH

Field-Programmable Gate Arrays (FPGAs) have become popular in multi-tenancy and cloud servers while exposing them to fault attacks. Existing countermeasures perform combinatory loop checks or deploy numerous on-chip sensors to mitigate voltage-drop attacks. We observe that existing mitigation techniques can mitigate attacks on a single tenant with a success rate of 75% and only 43% when mitigating attacks on multiple tenants or persistent attacks. Therefore, we propose a dynamic mitigation technique to update the current multi-tenant FPGA deployment flow by adding a function extract module and an adaptive DRC module. The redundant logic and its frequency have been extracted from the identified malicious bitstream in the function extract module and used to update the adaptive DRC module. The updated DRC is checked against all the new user requests and mitigates multiple voltage attacks before deploying them onto the fabric.

P.80: Pre-Silicon Hardware Trojan Horse Analysis

Austin Vorst, Alicia Washington
Booz Allen Hamilton, Beavercreek, OH

Adam Sherer
Cadence Design Systems Inc., Burlington, MA

Matt Sale
AFRL/RYDT, Wright-Patterson AFB, OH

P.81: RIPPER: Low-Overhead Fine-Grain Redaction Tool Flow for Hardware IP Protection

Aritra Dasgupta, Jackson Fugate, Greg Stitt, Swarup Bhunia
University of Florida, Gainesville, FL

Nij Dorairaj, David Kehlet
Intel Corporation, San Jose, CA

LUNCH **(12:00–1:30)**
Exhibit Hall

STEM THE "LEAKY PIPELINE" II PANEL

Thursday, March 21 / 8:30 – 10:10 am / Room 10/11

THE T&AM MPW PROGRAM PANEL DISCUSSION

Thursday, March 21 / 10:30 am – 12:10 pm / Room 10/11

LUNCH **(12:00–1:30)**
Exhibit Hall

ANALOG DESIGN AND EMULATION

Thursday, March 21 / 1:30 – 3:10 pm / Ballroom A

Chair: **Seyi Ayorinde**
Army Research Laboratory, Los Angeles, CA

Co-Chair: **Wes Hansford**
Boeing, Huntington Beach, CA

37.1: System-Level Mixed-Signal Emulation Digital Twin (1:30)

Nimay Shah
Analog Devices, Inc., Wilmington, MA

Luke Duncan
Niobium Microsystems, Columbus, OH

Jamin McCue
Air Force Research Laboratory, Wright-Patterson AFB, OH

Raj Mitra, Adam Sherer
Cadence Design Systems, Inc., Burlington, MA

37.2: A Cross-layer Framework for Design Space and Variation Analysis of Non-Volatile Ferroelectric Capacitor-Based Compute-in-Memory Accelerators (1:50)

James Read, Yuan-Chun Luo, Anni Lu, Shimeng Yu
Georgia Institute of Technology, Atlanta, GA

In this work, we present our system-wide framework for evaluating analog compute-in-memory (CIM) accelerators for deep neural networks (DNNs) using non-volatile capacitors. Typically, resistive random-access memory is used as the device of choice in these accelerators. These memories, however, face several limitations preventing them from meeting the high scalability demands of large-scale DNNs prevalent in the field of machine learning. Non-volatile, ferroelectric capacitors are one such solution to these limitations and as such merit a system-wide evaluation. Our framework incorporates device level measurements with array-level SPICE simulations and system-level functional simulations. Additionally, the framework assesses the system's power, performance, and area. Findings suggest that the capacitive CIM system is robust against D2D variation and noise, outperforming its resistive counterpart by 6.95× and 14.1× for the optimal design in the figure of merit (TOPS/W × TOPS/mm^2) for ResNet-50 and SwinV2-T respectively.

37.3: A 4 Transmit Receive, 4 GHz IBW, 0.1–20 GHz 3UVPX Tuner, Digitizer and Processor SoM (2:10)

W. Michael Jones, Bryce Readyhough
Analog Devices, Inc., Durham, NC

John Majewski
Analog Devices, Inc., Chelmsford, MA

A four-channel transmit, four-channel receive 3UVPX tuner plus digitizer platform all contained within a single 1-inch pitch chassis is developed leveraging a multichannel high-speed digitizer integrated circuit (IC). The system enables wideband digitization up to 5GSPS data rates per channel covering a frequency tuning range between 0.1–20 GHz and is comprised of both a Digitizer Base Card and a Tuner Personality Card. The digital offload options include on-board memory as well as both copper and optical Ethernet interfaces enabled by a FPGA/SoC combination collocated with a multichannel digitizer IC on the Digitizer Base Card. The front-end networks which leverage new system-in-package (SiP) technology for the Tuner Personality Card is also covered. Additionally, this paper describes plans to enable key digitizer IC hardened digital signal processing (DSP) features often required for electronic warfare applications, such as low latency loopback, fast-frequency-hopping, on-chip FFT sniffing and dynamic decimation/interpolation reconfiguration.

37.4: Digitally Programmable Current Mirrors Utilizing Cascode Transistors (2:30)

Kwabena Oppong Banahene, Randall Geiger
Iowa State University, Ames, IA

An innovative solution to the growing transistor size problem is the introduction of a new digitally programmable current mirror. The design uses current mirror transistors to segment the programmable current mirror and the cascode transistor, creating a sub-array for binary weighting within the segment. The simulation results demonstrate that this new structure provides linear control.

37.5: Custom Microelectronics Development for Modernization of Legacy DoD Systems (2:50)

Jeff Durrum
Booz Allen Hamilton, Beavercreek, OH

Saverio Fazzari
Booz Allen Hamilton, Arlington, VA

Adam Sherer
Cadence Design Systems, Burlington, MA

State of the art microelectronics are the cornerstone to mission critical DoD systems. Due to a variety of unavoidable reasons, the DoD must sustain increasingly obsolete microelectronics components across extended mission lifecycles. Aging and difficult to source parts introduce risk and incur billions in sustainment costs. Additionally, A reliable development flow has been demonstrated to provide modernized microelectronics parts in state of the art fabrication nodes. These reliable replacement parts are a source of trusted and assured microelectronics to provide a complete form fit and function solution, all the way from design specification through fabrication, packaging, board, and final implementation.

BREAK (3:10–3:30)
Ballroom Foyer

WIDEBAND ADAPTIVE RF PROTECTION (WARP) I

Thursday, March 21 / 1:30 – 3:10 pm / Ballroom B

Chair: **David Abe**
DARPA MTO, Arlington, VA

Co-Chair: **Steven Gross**
DARPA MTO SETA, Arlington, VA

38.1: Wide Band, Frequency Adaptive Filter with Embedded Threshold Detection **(1:30)**

Michael Meholensky, Eric Peterson, Zach Haralson
Collins Aerospace, Cedar Rapids, IA

Charles Campbell
Qorvo, Richardson, TX

38.2: Reconfigurable Filter MMICs Covering 2–18 GHz **(1:50)**

Charles F. Campbell, Deep C. Dumka, Jeffrey Miller
Qorvo, Richardson, TX

This paper describes the design, simulation and experimental results for three Gallium Arsenide electronically reconfigurable filter bank MMICs suitable for RF filtering and frequency selective interference rejection. Simulated results are shown for a 2.0–4.0 GHz 4-channel MMIC and an 8.5–18 GHz 6 channel design. Measured results are presented for a 6-channel 4.0 8.5 GHz MMIC. Experimental results for the low loss IN-Band state demonstrates 4.0 dB average insertion loss and 30 dBm typical input IP3. Experimental results for Out-of-Band rejection states indicates greater than 37 dB of loss and 50 dBm typical input IP3.

38.3: Reconfigurable Microwave Filters for Interference Mitigation in Next Generation Wireless Systems **(2:10)**

Eric E. Hoppenjans
Indiana Microelectronics, LLC, West Lafayette, IN

38.4: A Wideband Analog FIR Filter with Planar Silicon Carbide Delay-Line **(2:30)**

Eric Wagner, Mason Fordham, Todd Cooper, Mathew Biedka, Zhongzhong Dong, Joe Nedy, Brandon Paterson, Aaron Oki, Tim LaRocca
Northrop Grumman Space Systems, Redondo Beach, CA

38.5: Frequency Tunable Notch Filters Realized in Thin Film Yttrium Iron Garnet with Zero Power Magnetic Bias Circuit **(2:50)**

Xingyu Du, Shun Yao, Yixiao Ding, Zhehao Yu, Alexander J. Geers, Firooz Aflatouni, Mark Allen, Roy H. Olsson III
University of Pennsylvania, Philadelphia, PA

This paper reports on the realization of miniature, frequency tunable, high quality factor (Q), notch filters that consume zero static power. The high-Q notches are based on magnetostatic surface wave (MSSW) resonators. To obtain low insertion loss, the parasitic inductance of the MSSW resonator transducers are absorbed into an on-chip LC transmission line. Using this approach, a 19-stage frequency tunable notch filter with a notch depth exceeding 48 dB is achieved while simultaneously allowing for a passband insertion loss <1.5 dB over the entire 3.4–11.1 GHz tuning range. The frequency of the notch is tuned using a previously reported magnetic bias circuit that occupies only 1.68 cc of volume, achieves a magnetic field tuning range from 284–3180 Gauss, and consumes zero static power.

BREAK **(3:10–3:30)**
Ballroom Foyer

QUANTUM TECHNOLOGY

Thursday, March 21 / 1:30 – 3:10 pm / Ballroom C4

Chair: **Gerald Borsuk**
Naval Research Laboratory, Washington, DC

Co-Chair: **Michael Lovellette**
The Aerospace Corporation, Chantilly, VA

39.1: Quantum Computing at the Utility Scale and Beyond (1:30)

Jay M. Gambetta, Antonio D. Córcoles, Paul D. Nation
T.J. Watson Laboratory, Yorktown Heights, NY

With the recent demonstration executing quantum circuits outside the reach of classical exact computing methods, it is evident that the field is quickly approaching utility scale; where quantum computers could serve as a scientific tool to explore a new scale of problems that classical methods may not be able to solve. This scale combined with advances in algorithms is fundamental to enable quantum advantage; the point where quantum computers can faithfully run one of more tasks providing business or scientific value with more accuracy, efficiently, or cost-effectiveness than with classical computation alone. Given this rapid progress, we review the technical achievements that have enabled these advances, and offer insight into the next milestones that unlock the potential of quantum computing to address computation at scales relevant for industrial applications.

39.2: Advances in Trapped-Ion Quantum Computers and Co-Development of Practical Applications (1:50)

Masako Yamada
IonQ, Inc., College Park, MD

As quantum computers rapidly move toward larger and higher-quality systems, the capability of quantum applications also grows in parallel. We provide an overview of state-of-the-art IonQ trapped-ion quantum computing hardware, as well as an overview of practical use cases that we have developed for a range of clients. Additionally, we propose how these technologies could potentially be adapted and applied toward government interests.

39.3: Magnetic Random Access Memory (MRAM) for Embedded Quantum Computing Hardware **(2:10)**

Onri J. Benally, Deyuan Lyu, Brandon Zink, Y. Lv, K. Andre Mkhoyan, J. P. Wang
University of Minnesota, Minneapolis, MN

P. Khanal, W. Wang
University of Arizona, Tucson, AZ

Jenae E. Shoup, Brian Hoskins, Daniel B. Gopman
National Institute of Standards and Technology, Gaithersburg, MD

For both the current era of noisy intermediate-scale quantum and future fault tolerant quantum computing eras, memory is a buffer for the interaction of classical and quantum domains. To make quantum computers scalable and practical requires the exploration of compatible hardware such as robust random-access memory. It has been shown that memory can store reusable pulse sequences for controlling physical qubits, making it possible for larger qubit counts of increasing fidelity with each implementation. This paves the way for the application of quantum error correction codes for advanced quantum computers. Findings from our lab have demonstrated that spin-transfer torque magnetic tunnel junction memory cells can operate at the sub-nanosecond time scale in temperatures down to 2K. With that, we've also shown a successful implementation of energy efficient spin-orbit torque magnetic tunnel junction memory cells that can switch by voltage control exchange coupling effects. We propose, based on the above motivations, a spin-orbit torque cryogenic magnetic random-access memory architecture for quantum computing hardware.

39.4: Correction of Time-Varying Errors in Atom Interferometry **(2:30)**

Adam T. Black, Jonathan M. Kwolek
U.S. Naval Research Laboratory, Washington, DC

Inertial sensors based on atom interferometry have been shown to exhibit high sensitivity and accuracy in controlled laboratory environments. However, these sensors are susceptible to systematic errors related to energy shifts in the internal atomic states induced by magnetic fields or laser fluctuations. Well-known techniques for slow periodic reversal of the sensor's axis of inertial sensitivity are able to mitigate dc level-shift errors by several orders of magnitude. Time-varying level shifts are not successfully addressed by such slow reversal. Here we show, both through modeling and experimentation, that a sensor architecture featuring continuous interrogation of laser-cooled atoms can successfully mitigate time-varying level-shift errors through rapid axis reversal.

39.5: An Analysis of Teleportation Through an Arbitrary State **(2:50)**

Daniel Bonior, Mark Palenik, Tanner Crowder
Naval Research Laboratory, Washington, DC

Teleportation is a quantum mechanical process that transfers the information encoded in a quantum state without the actual system passing through physical space. This protocol relies upon a shared quantum state, which is generally assumed to be maximally entangled, a standard that is often not guaranteed by current experimental capabilities. In this paper, we provide a more concise and informative proof for the full characterization of imperfect entanglement in n-qubit teleportation, as to compared that found in current literature. Using this model, we calculate the average fidelity of teleportation through imperfect entanglement and provide necessary and sufficient conditions for surpassing the average fidelity of distributing a qubit state via classical processes.

BREAK **(3:10–3:30)**
Ballroom Foyer

PROTECTION METHODS AND ASSESSMENTS

Thursday, March 21 / 1:30 – 3:10 pm / Ballroom C1-3

Chair: Vivek Menon
National Reconnaissance Office, Chantilly, VA

Co-Chair: Adam Waite
Battelle Memorial Institute, Beavercreek, OH

40.1: Cryptographic Assurance of a Microelectronic Supply Chain (1:30)

Matthew Orzen, Scott C. Best
CRI (a subsidiary of Rambus, Inc.), San Jose, CA

40.2: Physically Secure Hardware Redaction with Strain-Shielded Nanomagnetic Logic (1:50)

Jared D. Arzate
University of Texas at Dallas, Richardson, TX
and
University of Texas at Austin, Austin, TX

Alexander N. Chin, Yiorgos Makris, Naimul Hassan, Alexander J. Edwards, Joseph S. Friedman
University of Texas at Dallas, Richardson, TX

Recent hardware obfuscation techniques such as logic locking and hardware redaction rely on the security of a programmable obfuscation key stored on-chip. Hardware redaction shows more resilience to algorithmic Boolean satisfiability (SAT)-based attacks due to finer-grained obfuscation, however, it was recently demonstrated that logic obfuscation schemes implemented in CMOS remain vulnerable to physical attacks based on electrical side-channel analysis or imaging of electrical behavior. These physical vulnerabilities can be eliminated by using non-electrical technologies such as nanomagnetic logic (NML) for logic obfuscation, and given the physical security of strain-protected NML, we propose a new hardware redaction scheme based on an embedded field-programmable gate array constructed entirely in NML to replace sensitive IP within a larger CMOS circuit. This is therefore the first hardware redaction scheme that is secure against all known physical and algorithmic attacks.

40.3: Enabling Rapid Deployment of COTS-based High-Security Products through Security Autonomy (2:10)

Matthew Areno
Intel Corporation, Austin, TX

Raghu Yeluri
Intel Corporation, Hillsboro, OR

Security Autonomy is an industry paradigm that enabled equipment owners to customize security settings and features specific to their unique deployment scenario and threat model. It is a key requirement for any processing solution attempting to enable rapid product deployment across a wide range of requirements, including high security. The paper presents a first of its kind approach to enabling security autonomy in commodity products to facilitate such needs. It also presents a new solution meant to enable network-level management and control of this technology in public and private cloud instances.

40.4: Creating a Scalable Security Assurance Workflow for Third-Party IP **(2:30)**

Jason Oberg, Aloke Das
Cycuity, Inc., San Jose, CA

Ryan Walker, Kyle Ahearn, Mark Labbato
Booz Allen Hamilton, Beavercreek, OH

Todd James, Matthew Sale
Air Force Research Laboratory, Wright-Patterson AFB, OH

40.5: Spectral Fingerprinting and Security Vulnerability Analysis of Pluggable Optical Transceivers **(2:50)**

**Leonardo G. Mesquita, John R. Holaday,
Ryan J. Herrington, LeAnn M. Hamilton,
Vincent M. Vangelista, Stephen W. Howell**
Naval Surface Warfare Center – Crane Division, Crane, IN

BREAK **(3:10–3:30)**
Ballroom Foyer

SOLID STATE TECHNOLOGY FOR PULSED POWER SOURCES

Thursday, March 21 / 1:30 – 3:10 pm / Room 6/7

Chair: **Joseph Croman**
Naval Research Laboratory, Washington, DC

Co-Chair: **Travis Anderson**
Naval Research Laboratory, Washington, DC

41.1: Development of Highly Manufacturable Drift Step Recovery Diodes for Ultra-Wideband Pulsed Power Applications (1:30)

Andrew Koehler, Michael Mastro, Karl Hobart, Alan Jacobs, Joseph Croman, Travis Anderson
U.S. Naval Research Laboratory, Washington, DC

Christopher Wu, Anthony Troxell
Defense Microelectronics Activity, McClellan, CA

Michael Hontz
Naval Surface Warfare Center Philadelphia, Philadelphia, PA

Geoffrey Foster
Jacobs, Inc., Residing at U.S. Naval Research Laboratory, Washington, DC

Ronald Focia
Envisioneering, Inc., Residing at U.S. Naval Research Laboratory, Washington, DC

Solid-state high-power microwave (HPM) sources based on semiconductor opening switches (SOS), such as drift step recovery diodes (DSRDs) have potential for generating pulses with high peak voltage, narrow pulse widths, and high repetition frequencies. In this work we describe a simulation-guided, highly manufacturable 150 mm silicon DSRD fabrication process, based on aluminum ion implantation, to uniformly and reproducibly produce deep pn junctions. In addition, a wafer-scale stacking approach is developed to increase operating voltage by series stacking DSRDs. Dynamic evaluation test circuits are designed, simulated, and constructed to appropriately bias the DSRDs to characterize their performance.

41.2: SiC Opening and Closing Switches for High Power Pulsed Applications (1:50)

Reza Ghandi
GE Research Center, Niskayuna, NY

Jason Sanders
Transient Plasma Systems, Inc., Torrance, CA

Design considerations for single junction and stacked SiC drift step recovery diode (DSRD) and avalanche sharpening diode (SAS) are discussed, and experimental data are presented. We demonstrate that a stack of SiC DSRDs can generate 10 kV 2 ns pulses, and a complementary SiC SAS diode can further sharpen the pulses to approximately 100ps rise times.

41.3: Solid State Switches for Pulsed Power Applications – An Overview of Lawerence Livermore National Laboratory's Work **(2:10)**

Caitlin A. Chapin, Qinghui Shao, David Smith, Sara E. Harrison, John Monzon, Robert Beard, Brent McHale, Lars F. Voss
Lawernce Livermore National Laboratory, Livermore, CA

Mark Rader
US Arm Space and Missile Defense Command, Huntsville, AL

James Shrock
Air Force Research Laboratory, Kirtland AFB, NM

41.4: Lock on Phenomena in GaN Photoswitches Demonstration and Potential Applications **(2:30)**

Jane Lehr, Nicolas Gonzalez, Brad Maynard
University of New Mexico, Albuquerque, NM

Harry Hjalmarson, Bob Kaplar, Alan Mar, Seth Miller, Emily Schrock, Greg Prickrell
Sandia National Laboratories, Albuquerque, NM

Gallium nitride (GaN) has been considered a prime candidate for the high-gain mode of operation of the PCSS. While multiple researchers have reported linear operation of WBG-based PCSS, the non-linear, high-gain mode of operation has been quite elusive over the last years. Recent experiments conducted at the University of New Mexico show clear evidence of high gain operation in lateral GaN PCSS devices with average electric fields <30 kV/cm and pulsed laser energies of a few tens of microJoules.

41.5: Salient Methods for Drift Step Recovery Diode Manufacturing, Passivation, and Encapsulation **(2:50)**

S. Bellinger
Radiation Detection Technologies, Inc. (RDT), Manhattan, KS and
Semiconductor Power Technologies, Inc. (SPT), Manhattan, KS

A. Usenko, J. Eifler, R. Allen, A. Caruso
University of Missouri-Kansas City, Kansas City, MO

BREAK **(3:10–3:30)**
Ballroom Foyer

PACKAGING TEST AND CHARACTERIZATION

Thursday, March 21 / 3:30 – 4:50 pm / Ballroom A

Chair: **Wes Hansford**
Boeing, Huntington Beach, CA

Co-Chair: **Vashisht Sharma**
Institute for Defense Analyses, Alexandria, VA

42.1: Test and Assembly Pitfalls in the Age of Advanced Packaging (3:30)

Sultan Lilani, Matt Bergeron
Integra Technologies, Milpitas, CA

Today's advanced packaging environment brings unprecedented opportunities to create products that are truly able to be market leaders in an economically sound and swift way. With this great opportunity comes some pitfalls in both Test and Assembly. Integra will discuss specific examples of pitfalls such as test debug, solder hierarchy, material signal integrity issues and how to avoid them.

42.2: A Near-Field Over-the-Air Approach for the Design, Testing, and Evaluation of Chip-Package-PCB-AiP Modules (3:50)

Mo Shakouri, Doug Gray
Microsanj LLC, Fremont, CA

Sidina Wane
eV-Technologies, Caen, France

Ali Shakouri
Purdue University, West Lafayette, IN

Traditional design approaches individually optimize chip, package, printed circuit board, and antenna. Even with high success at each step the overall end-to-end result will fall far short of an optimal solution for the completed module. This presentation describes a holistic Near-Field (NF) Over-The-Air (OTA) testing approach for Chip-Package-PCB-Antenna modules based on the combined field-proven Thermoreflectance imaging technique and a novel Thin-Film coating using Spin-Crossover (SCO) materials. The SCO coating process demonstrates highly reliable thermometric performance with diffraction-limited sub-micron spatial, sub-microsecond temporal, and less than 1-degree centigrade thermal resolution. The resulting performance qualifies the SCO coating process, in terms of fabrication and switching endurance for industrial testing to ensure highly reproducible analysis and measurement results. The proposed near-field sensing solutions are demonstrated by several practical applications using Front-End-Modules (FEMs) with advanced GaN and Fully-Depleted Silicon On Insulator (FD-SOI) technologies co-designed with antenna-in-package (AiP) modules based on heterogeneous System-in-Package and Wafer-Level-Chip-Scale-Packaging (WLCSP) fan-in/fan-out integration assemblies.

42.3: Modular, High Performance RF Microsystems Enabled by Advanced Packaging (4:10)

Matthew B. Jordan, Christopher D. Nordquist, Matthew Bahr, Mieko Hirabayashi, Stefan Lepkowski, Tyler Liebsch, Alexander Ruyack, Jessica McDow, Michael G. Wood
Sandia National Laboratories, Albuquerque, NM

This work demonstrates the use of advanced packaging achieve high data-rate communications between chips as well as integrated RF passive components that reduce size, weight, power, and discrete component counts. Specifically, III-V analog, optoelectronic, and Si CMOS die are combined on a glass interposer utilizing flip chip packaging. Integration challenges, frequency dependent performance tradeoffs with printed circuit board integration, and radiation tolerance have been evaluated and will be discussed.

42.4: Advanced Semiconductor Packaging for Advanced Applications — Landscape Assessment (4:30)

Fernando Roa, Robert McNamara, Vivek Nelanuthala, Richard Gay Jr.
Booz Allen Hamilton, McLean, VA

Darren Crum, Brian Olson
U.S. Department of the Navy, Crane, IN

The intersection of advanced packaging (AP) and artificial intelligence (AI) is a burgeoning field with exciting prospects for growth. The U.S. Department of Defense (DoD) is interested in exploring this field and developing its own capabilities. To that end, the DoD seeks to evaluate the capabilities of various organizations that operate in the AP or AI spaces, within the U.S. domestic defense industrial base (DIB). This paper seeks to provide an overview of those capabilities, as well as to provide insight into research and development activities that show promise to drive the future of AI-enabled edge devices; these activities include DARPA initiatives to develop new AI algorithms and deployment processes, as well as novel computer architectures that could accelerate and streamline these algorithms. This study will also discuss the AP and chiplet-manufacturing activities of the DIB, and evaluate the potential of these activities to promote AI capabilities.

Session 43 (RF Technologies, Components, and Systems)

WIDEBAND ADAPTIVE RF PROTECTION (WARP) II

Thursday, March 21 / 3:30 – 5:10 pm / Ballroom B

Chair: **David Abe**
DARPA MTO, Arlington, VA

Co-Chair: **Iskren Abdomerovic**
Booz Allen Hamilton, Arlington, VA

43.1: Multi-octave Tunable Acoustic Bandpass Filters (3:30)

Matthew Morton, Charles Wang, William Sear, Jason Adams, Clay Long, Adam Peczalski, Matt Rebholz
Raytheon Technologies, Andover, MA

Damla Dimlioglu, Thomas Tapen, Alyosha Molnar, Alyssa Apsel
Cornell University, Ithaca, NY

43.2: Multi-octave Independently-tuned Notch Filters (3:50)

Matthew Morton, Charles Wang, William Sear, Jason Adams, Clay Long, Adam Peczalski, Matt Rebholz
Raytheon Technologies, Andover, MA

Armagan Dascurcu, Hari Vemuri, Harish Krishnaswamy
Columbia University, New York, NY

43.3: Photonic-Acoustic Self Interference Cancellation System on Commercial SOI SiPh Process (4:10)

Mertcan Erdil, Izhar FNU, Roy H. Olsson III, Firooz Aflatouni
University of Pennsylvania, Philadelphia, PA

We report progress on development of an integrated photonic-acoustic system to perform self-interference cancellation in wideband RF transceivers. Preliminary measurement results are reported.

43.4: An RF Self-Interference Canceller with In-Situ Channel-Sensing and Closed-Loop Control (4:30)

Mark D. Hickle
BAE Systems, Inc., Merrimack, NH

Jeffrey Feigin, Matthew Conte, Jonathan Comeau
BAE Systems, Inc., Burlington, MA

Jonathan Beaudeau, Devin Marzullo
Pareto Frontier, Westford, MA

43.5: Modeling and Optimization of Analog Self-Interference Cancellation Spur Reduction (4:50)

Carl W. Morgenstern, Yu Rong, Adarsh Venkataramani, Daniel W. Bliss
Arizona State University (ASU), Tempe, AZ

Scott Hinton, David G. Landon
L3Harris Technologies, Salt Lake City, UT

Alyosha C. Molnar, Alyssa B. Apsel
Cornell University, Ithica, NY

SUPERCONDUCTING AND CRYOGENIC TECHNOLOGY

Thursday, March 21 / 3:30 – 5:10 pm / Ballroom C4

Chair: **Michael Lovellette**
The Aerospace Corporation, Chantilly, VA

Co-Chair: **Barry Treloar**
Strategic Systems Programs, Washington, DC

44.1: Superconducting Electronics at MIT Lincoln Laboratory (3:30)

Justin Mallek, Sergey Tolpygo
Massachusetts Institute of Technology, Lexington, MA

44.2: Thermal Analysis Methodology for Single Flux Quantum ICs (3:50)

Ana Mitrovic, Eby G. Friedman
University of Rochester, Rochester, NY

The maturing of rapid single flux quantum (RSFQ) circuits into a VLSI complexity technology has focused the need for advanced design and analysis capabilities. The temperature dependence of RSFQ circuits has created a need for a thermal analysis methodology, including an accurate thermal model and related partitioning algorithm. Heating of Josephson junctions and niobium interconnects results in reduced margins or functional failure. A methodology for evaluating the thermal properties of RSFQ integrated circuits, targeting large scale systems, is presented here. This methodology is comprised of a thermal model and a multi-stage partitioning algorithm. The algorithm, based on a layout of the IC, partitions the circuit into blocks. A thermal model is applied to the partitioned structure, producing a netlist for thermal simulation. The algorithm is evaluated at several granularities and validated using a numerical solver. An error of less than 0.51% between the model and numerical simulations is achieved.

44.3: Visible-to-IR Superconducting Photon Detectors at MIT Lincoln Laboratory (4:10)

Kevin Ryu, Vladimir Bolkhovsky, Joseph Cimapi
MIT Lincoln Laboratory, Lexington, MA

Benjamin Mazin, Hawkins Clay, Aled Cuda
University of California, Santa Barbara, Santa Barbara, CA

Microwave Kinetic Inductance Detectors (MKIDs) are superconducting detectors that provide single photon counting with negligible dark counts (<1 mHz). They also provide energy resolving capability for every photon and give photon arrival times with microsecond resolution. Moderate array sizes of 20 kilo pixels have been demonstrated and have been fielded on some of the largest telescopes in the world. However, fabrication challenges have limited the yield and performance of the array. MIT Lincoln Laboratory has the Microelectronics Laboratory that is well-suited for microfabrication of large arrays of superconducting detectors. This presentation will review the development of first 20 kilo-pixel MKID array at Lincoln Laboratory and the roadmap for more capable future arrays.

44.4: Deep Neuromorphic Networks with Superconducting Single Flux Quanta (4:30)

Alexander J. Edwards, Joseph S. Friedman
University of Texas at Dallas, Richardson, TX

Gleb Krylov, Eby G. Friedman
University of Rochester, Rochester, NY

The similarities between single flux quantum (SFQ) and neuronal spiking has previously been observed; however, prior proposals for SFQ neural networks often require energy-expensive fluxon conversions, involve heterogeneous technologies, or exclusively focus on device level behavior. In this paper, a design methodology for deep single flux quantum neuromorphic networks is presented. Synaptic and neuronal circuits based on SFQ technology are presented and characterized. Based on these primitives, a deep neuromorphic XOR network is evaluated as a case study, both at the architectural and circuit levels, achieving wide classification margins. The proposed methodology does not employ unconventional superconductive devices or semiconductor transistors. The resulting networks are tunable by an external current, making this proposed system an effective approach for scalable cryogenic neuromorphic computing.

44.5: The Case for COLD / CRYO CMOS & FD-SOI (4:50)

Jamil Kawa, Stephen Whiteley, Robert Freeman
Synopsys, Inc., Sunnyvale, CA

CMOS has been proven to work down to sub 1K and FD-SOI based Gate Arrays that are at the heart of Quantum Computing control blocks. COLD CMOS computing farms operating offer compelling power-performance benefits. And in space-based applications where power budgets are extremely stringent, these optimizations naturally fit. However, there is more to COLD and CRYO CMOS & FD-SOI than better performance at lower power. Issues associated with device re-engineering, optimal combination of power supply voltage reduction and “equilibrium” operating temperature for optimal power savings, and device variability at reduced temperatures must be addressed thoroughly. This talk will address the issues and benefits of CMOS and FD-SOI retargeted for cooled compute environments, quantum controller environments, and space-based applications. We will draw on our efforts in the DARPA sponsored LTLT program as well as Synopsys’ overall research and activities to advance the state of the art in COLD and CRYO.

RADIATION HARDENED BY DESIGN (RHBD)

Thursday, March 21 / 3:30 – 5:10 pm / Ballroom C1-3

Chair: **Lloyd Massengill**
Reliable MicroSystems, Franklin, TN

Co-Chair: **Lew Cohn**
National Reconnaissance Office, Chantilly, VA

45.1: Zipper Layouts for Improved Single-Event Tolerance in Integrated Circuit Designs (3:30)

Michael D. Hu, Oliver E. Forman, Jeffrey S. Kauppila, James M. Trippe, Lloyd W. Massengill, W. Timothy Holman
Vanderbilt University, Nashville, TN

Sean T. Vibbert
Reliable MicroSystems LLC, Franklin, TN

A novel layout technique is described that significantly improves single-event tolerance in stacked-transistor circuit topologies with only minimal area penalty. Layout examples and simulation results are provided to illustrate the improvement in radiation hardness.

45.2: Accelerating Robust Analog State of the Art Design using ADONIS™ (3:50)

Thomas L. Wolf, Kent F. Smith, Jared Bytheway
Silicon Technologies, Inc., Salt Lake City, UT

45.3: Compact 20 GHz RF Low Noise, Radiation Tolerant Amplifier Approach in 22 nm Fully Depleted Silicon-on-Insulator Technology (4:10)

Tom G. McKay
Silicon Technologies Inc., Midvale, UT

One mitigation approach to radiation single event effects (SEE) in radio frequency circuits is to choose circuit architectures which avoid high impedance nodes whose voltage can be disturbed by small charge injections. For example, in a recent study, conventional cross-coupled CMOS high-impedance parallel LC-tank oscillators were shown to be inferior to Colpitts oscillator topologies for SEE. Here we propose a single-ended to differential noise cancelling low noise amplifier topology capable of wide 20 GHz bandwidth in 22 nm FDSOI, avoiding high impedance nodes common in reactive impedance matched designs and therefore less susceptible to SEE. Additionally, this architecture can result in compact designs as it avoids spiral inductors and transformers, reduces size through full system RF and digital co-integration.

45.4: Turn-Key RHBD: Vertically-Integrated Radiation-Aware Design **(4:30)**

D. S. Vibbert, C.T. Jensen, J.S. Kauppila, W.D. Welch, C.J. Conte, C.A. Sanders, M.A. Freestone, L.W. Massengill
Reliable MicroSystems, Franklin, TN

45.5: Dose-Rate Upset Characterization and Transient Analysis of All-Digital Phase-Locked Loops (AD-PLLs) in 14 nm FinFET CMOS **(4:50)**

Alfio Zanchi
Boeing Research & Technology, Tukwila, WA

Parham Hesamaddin
Boeing Research & Technology, Huntington Beach, CA

RESEARCH MATERIALS FOR ADDITIVE MANUFACTURING

Thursday, March 21 / 3:30 – 5:10 pm / Room 6/7

Chair: **Craig Keast**
MIT Lincoln Laboratory, Lexington, MA

Co-Chair: **Daniel Radack**
Institute for Defense Analyses, Alexandria, VA

46.1: Silicate-based Packaging Materials for Heterogenous Integration of Microsystems (3:30)

Ryan T. Benz, Keri Ledford, Avery Rosh-Gorsky, Devon Beck, Al Cabral, Matthew Ricci, Bradley Duncan
MIT Lincoln Laboratory, Lexington, MA

3D heterogeneous integration is at the cutting edge of microelectronics design and fabrication. Currently there are limitations in microelectronics packaging materials that inhibit widespread implementation of the technique, which presents an opportunity to develop new packaging materials. Building on previous work, an improved CMOS-compatible, silicate-based packaging material for 3D heterogeneous integration of microelectronics with a focus on mmWave RF applications was developed. The sodium-free composite material was shown to be compatible with common microelectronics fabrication processes such as positive and negative photolithographic patterning, wet etching, and most chemical cleans. The material could be deposited via spray coating at thicknesses ranging from single-digit microns up to several millimeters and exhibited excellent adhesion to silicon substrates. The novel material will undergo extensive characterization experiments to evaluate its physical properties.

46.2: Additive Manufacturing and Synthesis of 2D Materials for Advanced Device Applications (3:50)

Attila Rektor, Josh Eixenberger, Tony Varghese, Nicholas Mckibben, Naqsh Mansoor, David Estrada
Boise State University, Boise, ID

This work focuses on the design, synthesis, and characterization of nanomaterial-based inks, as well as fabrication of devices utilizing additive manufacturing technologies. Multiple ink systems have been developed, including zinc oxide, niobium, graphene, black phosphorus, bismuth telluride, nickel, gold, platinum, molybdenum, and the titanium carbide ($Ti_3C_2T_x$) MXene. These nanomaterial inks offer AM solutions for the construction of diodes, strain sensors, micro-supercapacitors, surface acoustic wave (SAW) thermometers, thermocouples, energy harvesters, electromagnetic interference (EMI) shielding, dosimeters, and radiation sensors. Synthesis routes for these inks include both top-down and bottom-up methods, which enable fine control of the resulting ink and ultimately device properties. The body of this report focuses on highlighting a number of the previously reported inks and devices, demonstrating their use and notable features.

46.3: Additive Manufacturing of Silicon Nitride (Si_3N_4) Radomes for Hypersonic Vehicles (4:10)

Guang Yang
Kansas State University, Manhattan, KS

Yuhui Xiang, Dong Lin
Oregon State University, Corvallis, OR

Xiaoling Shi, Hui Lu
Winchester Technologies, LLC, Burlington, MA

Mohan Sanghadasa
US Army DEVCOM Aviation & Missile Center, Redstone Arsenal, AL

Yifan He, Haoling Li, Bin Luo, Nian X. Sun
Northeastern University, Boston, MA

In the field of aerospace technology, the demand for materials capable of withstanding the extreme conditions of hypersonic flights is ever-growing. Hypersonic vehicles, surpassing Mach 5 speeds, necessitate advancements in materials science. Silicon nitride (Si_3N_4) stands out as the material of choice for hypersonic Radomes due to its exceptional thermal stability, thermal shock resistance, and mechanical strength. However, traditional manufacturing methods for Si3N4 Radomes pose limitations in terms of time, cost, and design flexibility. Additive Manufacturing, commonly known as 3D Printing, offers an innovative solution. This paper explores the application of Additive Manufacturing to Si_3N_4 Radome production, focusing on a novel technique called 3D Freeze Printing (3DFP), combining Direct Ink Writing (DIW) and Freezing-Casting to create intricate porous ceramic structures. Additionally, this paper delves into the rheological properties of the ink during extrusion and presents the concept of functionally graded Radomes tailored for hypersonic vehicles, open-space ultra-high temperature permittivity testing, etc. This research represents a significant step towards meeting the demanding requirements of hypersonic flights.

46.4: Radiation Tolerant Electronics via Additive Manufacturing (4:30)

Bradley Duncan, Avery Rosh-Gorsky, Austin Coon, Quinn Binney, Ryan Benz, Paul Miller, Isaiah Queen, Salvatore Di Cecca, Pascale Gouker, Melissa Smith
MIT Lincoln Laboratory, Lexington, MA

Devon Beck
Draper Laboratory, Cambridge, MA

The miniaturization of electronic systems for SWaP (Size, Weight, and Power) constrained platforms, such as satellites, promotes the development of the materials that protect these crucial devices. Current methods for preventing radiation induced damage to electronics necessitate making trade-offs between overall system performance and reliability. Alternatively, additive manufacturing offers an approach to directly deposit radiation shielding only on vulnerable components providing a more favorable SWaP posture. We describe a generalized process for formulating and fabricating custom radiation shields. Shielding architectures and compositions are screened using Monte Carlo N-Particle® models to down-select promising designs. The protection of an SRAM (static random-access memory) module from damage due to heavy ion exposure is demonstrated.

46.5: Additive Manufacturing of S-band Antennas with Graphite Composite Conductors and Metallic Inks (4:50)

Luke Lyle, Daniel Erdely, Lachlan Peeke, Thomas Majewski, Joseph Brown, Isaiah Adu, Tyler Ridder, Kristoffer Greenert, David Snyder, Mike Zugger, Callie Zawaski, Mike Yukish, Ethan Kravet, Mohnish Umashankar, Matthew Beckerle, Sven G. Bilén
Pennsylvania State University, University Park, PA

Additive manufacturing (AM) has made great strides in development over the last few decades. Through novel manufacturing technologies to innovative material systems, these technologies have enabled the production of new and exciting products. Success of AM on the commercial scale hinges on its adoption into manufacturing for rapid prototyping of complex geometry parts. The packaging and manufacturing of thin and flexible electronics provides a proving ground for the combination of novel materials and cutting-edge AM hardware to produce assemblies capable of changing how we engage with electronics.

Research presented showcases the Materials and Manufacturing Office at the Penn State Applied Research Lab (ARL) working on developing conductive graphite composite conductors and metallic inks for S-band antenna applications.

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